HD63P01M1
CMOS MCU (Microcomputer Unit)

The HD63P01M1 is an 8-bit single chip Microcomputer Unit (MCU) which has 4096 bytes or 8192 bytes of EPROM on the package. It is pin and function (except ROM) compatible with the HD6301V1. The HD63P01M1 can be used to emulate the HD6301V1 for software development or it can be used in production to allow for easy firmware changes with minimum delay.

■ FEATURES

- Pin Compatible with HD6301V1
- On Chip Function Compatible with HD6301V1
  - · 128 Bytes of RAM
  - · 29 Parallel I/O
  - · 16 Bit Programmable Timer
  - · Serial Communication Interface
- Low Power Consumption Mode
  Sleep Mode, Standby Mode
- Minimum Instruction Cycle Time
  1μs (f = 1MHz), 0.67μs (f = 1.5MHz), 0.5μs (f = 2MHz)
- Bit Manipulation, Bit Test Instruction
- Protection from System Upset
  Address Trap, Op-Code Trap
- Up to 65k Words Address Space
- Applicable to 4k or 8k Bytes of EPROM
  4096 Bytes: HN482732A
  8192 Bytes : HN482764, HN27C64

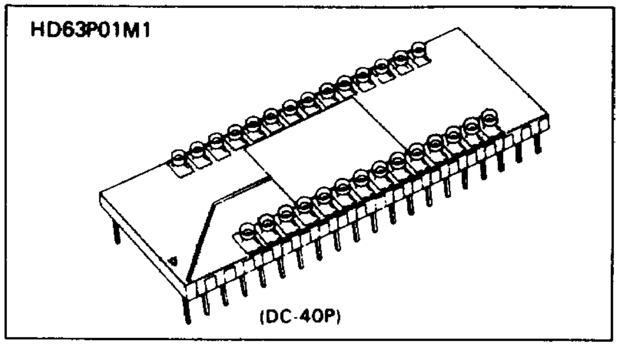
■ TYPE OF PRODUCTS

Type No.	Bus Timing	EPROM Type No.
HD63P01M1	1MHz	HN482732A-30, HN482764-3, HN27C64-30

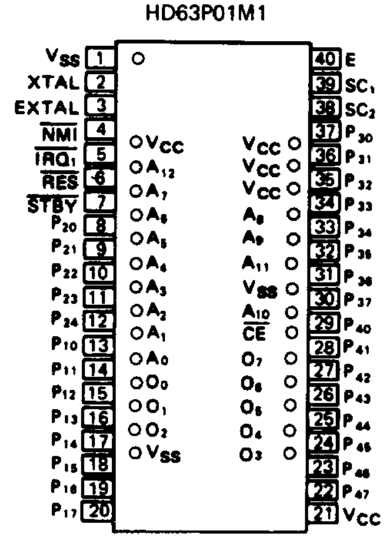
■ PROGRAM DEVELOPMENT SUPPORT TOOLS

- Cross assembler and C compiler software for IBM PCs and compatibles
- In circuit emulator for use with IBM PCs and compatibles

— The specifications for HD63PA01M1 and HD63PB01M1 are preliminary. —



■ PIN ARRANGEMENT



(Top View)

(NOTE) EPROM is not included.

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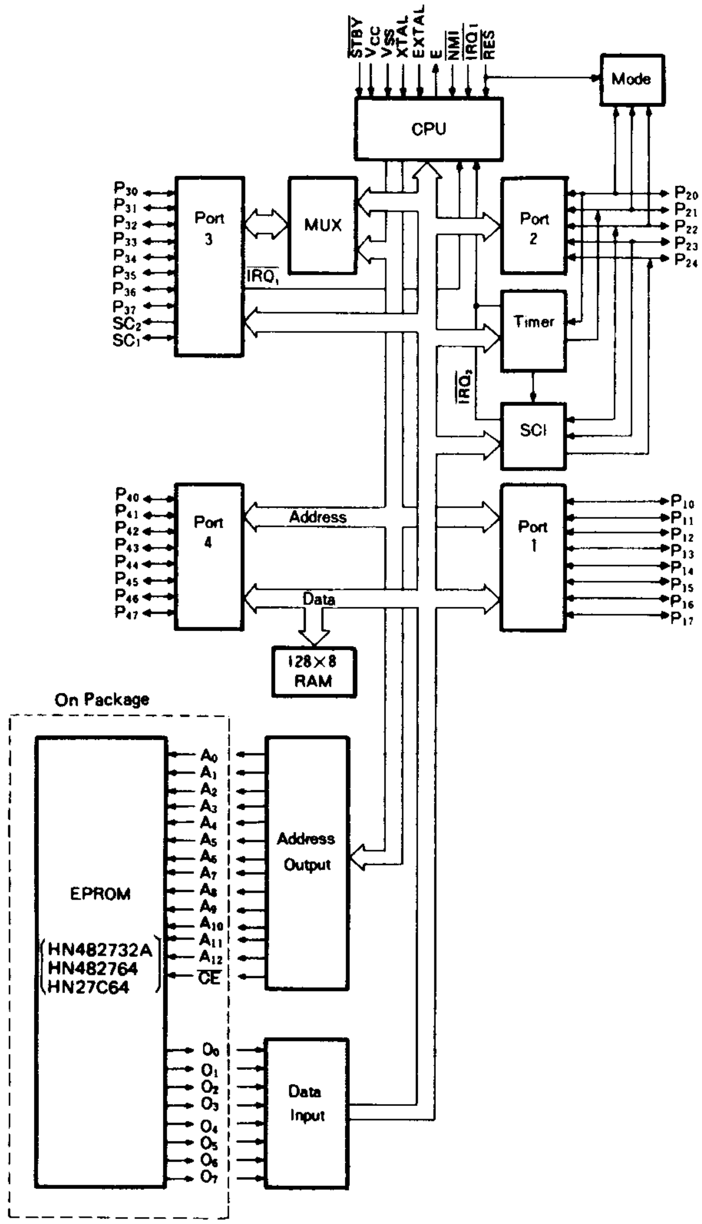
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 ~ +7.0	V
Input Voltage	V_{in}	-0.3 ~ V_{CC}+0.3	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

(NOTE) This product has protection circuits in input terminal from high static electricity voltage and high electric field. But be careful not to apply overvoltage more than maximum ratings to these high input impedance protection circuits. To assure the normal operation, we recommend V_{in}, V_{out} : $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, Ta = 0~+70°C, unless otherwise noted.)

Item		Symbol	Test Condition	min	typ	max	Unit
Input "High" Voltage	$\overline{RES}$, $\overline{STBY}$	V_{IH}		V_{CC}-0.5	–	V_{CC} +0.3	V
	EXTAL			V_{CC}x0.7	–		
	Other Inputs			2.0	–		
Input "Low" Voltage	All Inputs	V_{IL}		-0.3	–	0.8	V
Input Leakage Current	$\overline{NMI}$, $\overline{IRQ_1}$, $\overline{RES}$, $\overline{STBY}$	$\lvert I_{in} \rvert$	V_{in} =0.5~V_{CC}-0.5V	–	–	1.0	μA
Three State (off-state) Leakage Current	P_{10}~P_{17}, P_{20}~P_{24}, P_{30}~P_{37}, P_{40}~P_{47}, $\overline{IS3}$	$\lvert I_{TSI} \rvert$	V_{in} =0.5~V_{CC}-0.5V	–	–	1.0	μA
Output "High" Voltage	All Outputs	V_{OH}	I_{OH} = -200μA	2.4	–	–	V
			I_{OH} = -10μA	V_{CC}-0.7	–	–	V
Output "Low" Voltage	All Outputs	V_{OL}	I_{OL} = 1.6mA	–	–	0.55	V
Input Capacitance	All Inputs	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	–	–	12.5	pF
Standby Current	Non Operation	I_{CC}	V_{IL}($\overline{STBY}$)=0~0.6V V_{IH} ($\overline{RES}$) = V_{CC} - 0.5 ~ V_{CC} V V_{IL}($\overline{RES}$)= 0 ~ 0.6V	–	2.0	15.0	μA
Current Dissipation*		I_{CC}	Operating (f=1MHz**)	–	6.0	10.0	mA
			Sleeping (f=1MHz**)	–	1.0	2.0	
RAM Stand-By Voltage		V_{RAM}		2.0	–	–	V

* V_{IH} min = V_{CC}-1.0V, V_{IL} max = 0.8V, I_{CC} of EPROM is not included.

** Current Dissipation of the operating or sleeping condition is proportional to the operating frequency. So the typ. or max. values about Current Dissipations at f = x MHz operation are decided according to the following formula;

typ. value (f = x MHz) = typ. value (f = 1MHz) x x
max. value (f = x MHz) = max. value (f = 1MHz) x x
(both the sleeping and operating)

- **AC CHARACTERISTICS** (V_{CC} = 5.0V±10%, V_{SS} = 0V, Ta = 0~+70°C, unless otherwise noted.)

BUS TIMING

Item		Symbol	Test Condition	HD63P01M1 min	HD63P01M1 typ	HD63P01M1 max	Unit
Cycle Time		t_{cyc}	Fig. 1, Fig. 2	1	–	10	μs
Address Strobe Pulse Width "High"*		PW_{ASH}		220	–	–	ns
Address Strobe Rise Time		t_{ASr}		–	–	20	ns
Address Strobe Fall Time		t_{ASf}		–	–	20	ns
Address Strobe Delay Time*		t_{ASD}		60	–	–	ns
Enable Rise Time		t_{Er}		–	–	20	ns
Enable Fall Time		t_{Ef}		–	–	20	ns
Enable Pulse Width "High" Level*		PW_{EH}		450	–	–	ns
Enable Pulse Width "Low" Level*		PW_{EL}		450	–	–	ns
Address Strobe to Enable Delay* Time		t_{ASED}		60	–	–	ns
Address Delay Time		t_{AD1}		–	–	250	ns
		t_{AD2}		–	–	250	ns
Address Delay Time for Latch*		t_{ADL}		–	–	250	ns
Data Set-up Time	Write	t_{DSW}		230	–	–	ns
	Read	t_{DSR}		80	–	–	ns
Data Hold Time	Read	t_{HR}		0	–	–	ns
	Write	t_{HW}		20	–	–	ns
Address Set-up Time for Latch*		t_{ASL}		60	–	–	ns
Address Hold Time for Latch		t_{AHL}		30	–	–	ns
Address Hold Time		t_{AH}		20	–	–	ns
$A_0 \sim A_7$ Set-up Time Before E*		t_{ASM}		200	–	–	ns
Peripheral Read Access Time	Non-Multiplexed Bus*	(t_{ACCN})		–	–	650	ns
	Multiplexed Bus*	(t_{ACCM})		–	–	650	ns
Oscillator stabilization Time		t_{RC}	Fig. 10	20	–	–	ms
Processor Control Set-up Time		t_{PCS}	Fig. 11	200	–	–	ns

* These timings change in approximate proportion to t_{cyc}. The figures in this characteristics represent those when t_{cyc} is minimum (= in the highest speed operation).

■ 1.5 MHz AND 2 MHz OPERATION IN SINGLE CHIP MODE OF HD63P01M1

The HD63P01M1, now in mass production, is guaranteed to operate at 1 MHz. If the conditions below are met, it can operate up to 2 MHz.

Note (1) Only single chip mode (mode 7) is available.

Note (2) The access time is limited when the operation frequency is more than 1 MHz. Therefore use an EPROM that satisfies the condition below.
While operating at 1.5 MHz, the access time must be less than or equal to 400 ns.
While operating at 2 MHz, the access time must be less than or equal to 250 ns.

Note (3) Temperature Range: T_a = 0°C - 70°C
Operating Voltage: V_{CC} = 5V ± 10%

Note (4) This data is only for reference, and does not guarantee this characteristic.

■ **PERIPHERAL PORT TIMING (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0 ~ +70°C)**

Item		Symbol	Test Condition	HD63P01M1			Unit
				min	typ	max	
Peripheral Data Set-up Time	Port 1, 2, 3, 4	t_{PDSU}	Fig. 3	200	–	–	ns
Peripheral Data Hold Time	Port 1, 2, 3, 4	t_{PDH}	Fig. 3	200	–	–	ns
Delay Time, Enable Positive Transition to OS3 Negative Transition		t_{OSD1}	Fig. 5	–	–	300	ns
Delay Time, Enable Positive Transition to OS3 Positive Transition		t_{OSD2}	Fig. 5	–	–	300	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid	Port 1, 2, 3, 4	t_{PWD}	Fig. 4	–	–	300	ns
Input Strobe Pulse Width		t_{PWIS}	Fig. 6	200	–	–	ns
Input Data Hold Time	Port 3	t_{IH}	Fig. 6	150	–	–	ns
Input Data Setup Time	Port 3	t_{IS}	Fig. 6	0	–	–	ns

* Except P_{21}

■ **TIMER, SCI TIMING (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0 ~ +70°C)**

Item	Symbol	Test Condition	HD63P01M1			Unit
			min	typ	max	
Timer Input Pulse Width	t_{PWT}		2.0	–	–	t_{cyc}
Delay Time, Enable Positive Transition to Timer Out	t_{TOD}	Fig. 7	–	–	400	ns
SCI Input Clock Cycle	t_{Scyc}		2.0	–	–	t_{cyc}
SCI Input Clock Pulse Width	t_{PWSCK}		0.4	–	0.6	t_{Scyc}

■ **MODE PROGRAMMING (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0 ~ +70°C)**

Item	Symbol	Test Condition	HD63P01M1			Unit
			min	typ	max	
$\overline{RES}$ "Low" Pulse Width	PW_{RSTL}	Fig. 8	3	–	–	t_{cyc}
Mode Programming Set-up Time	t_{MPS}	Fig. 8	2	–	–	t_{cyc}
Mode Programming Hold Time	t_{MPH}	Fig. 8	150	–	–	ns

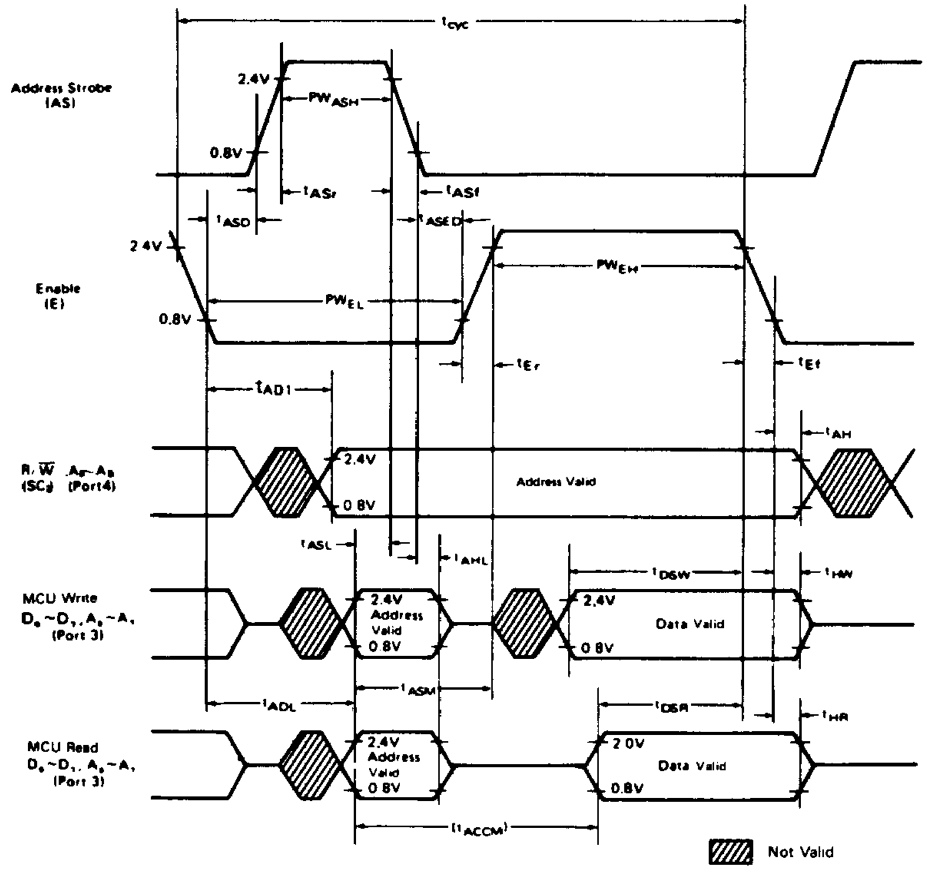


Figure 1 Expanded Multiplexed Bus Timing

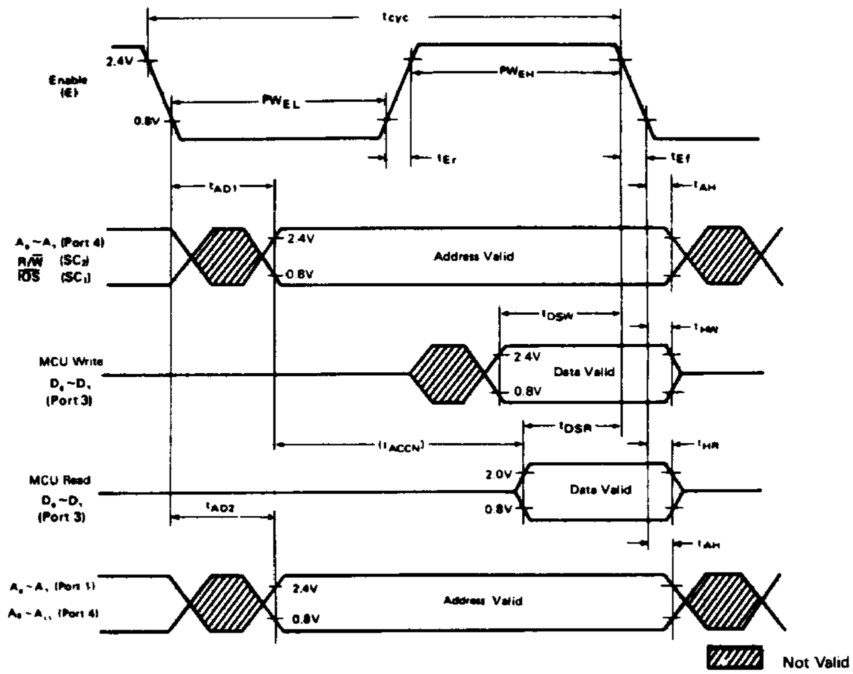
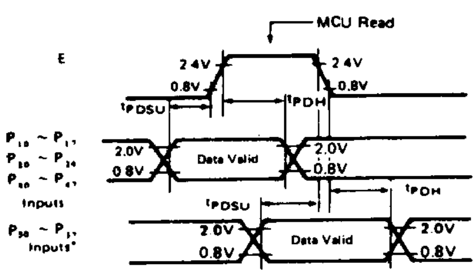
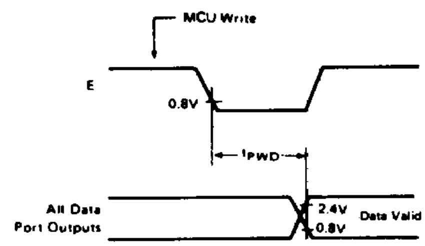


Figure 2 Expanded Non-Multiplexed Bus Timing



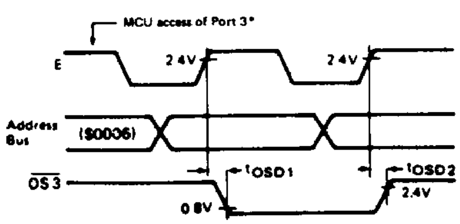
*Port 3 Non-Latched Operation

Figure 3 Port Data Set-up and Hold Times (MCU Read)



Note) Port 2: Except P_{21}

Figure 4 Port Data Delay Times (MCU Write)



*Access matches Output Strobe Select (OSS = 0, a read; OSS = 1, a write)

Figure 5 Port 3 Output Strobe Timing (Single Chip Mode)

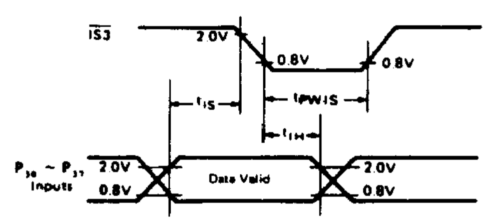


Figure 6 Port 3 Latch Timing (Single Chip Mode)

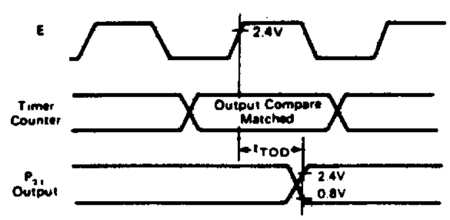


Figure 7 Timer Output Timing

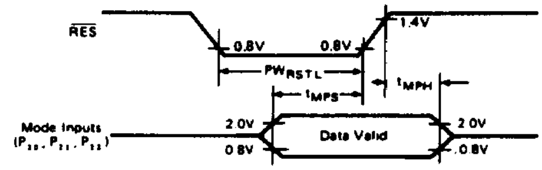
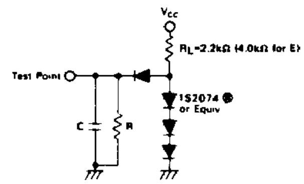


Figure 8 Mode Programming Timing



C = 90pF for $P_{30}-P_{37}$, $P_{40}-P_{47}$, SC_1, SC_2
= 30pF for $P_{10}-P_{17}$, $P_{20}-P_{24}$
= 40pF for E
R = 12kΩ

Figure 9 Bus Timing Test Loads (TTL Load)

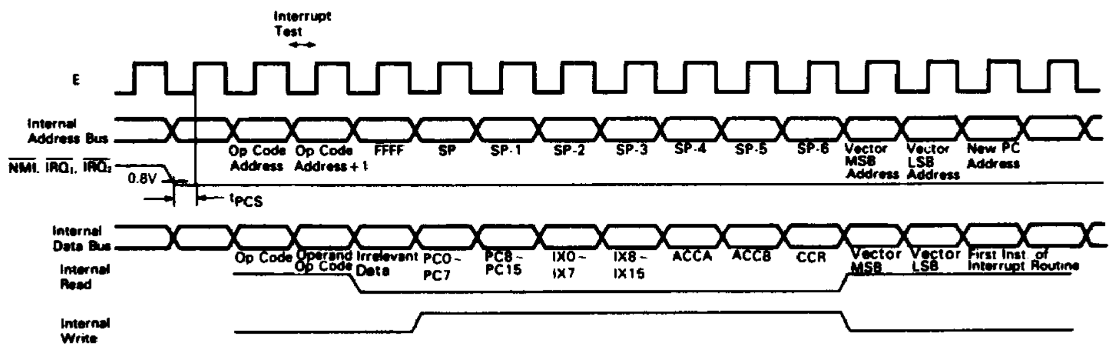


Figure 10 Interrupt Sequence

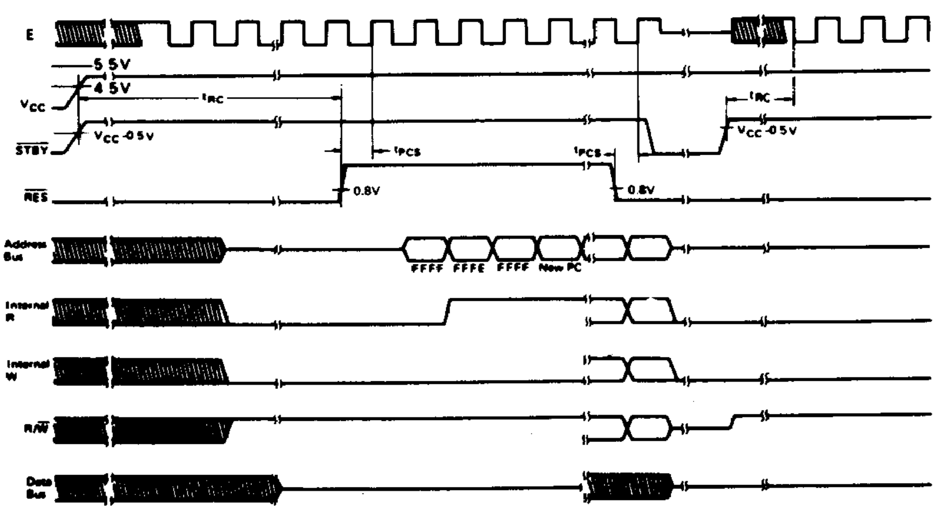


Figure 11 Reset Timing

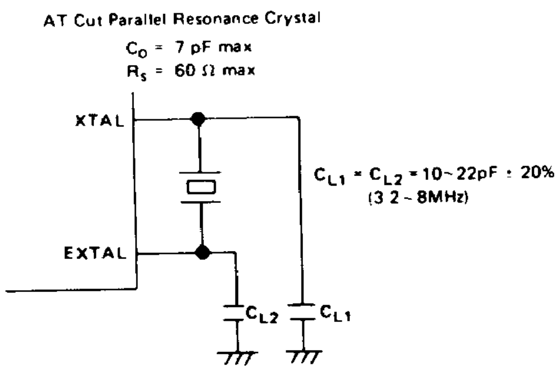
■ FUNCTIONAL PIN DESCRIPTION

• V_{CC}, V_{SS}

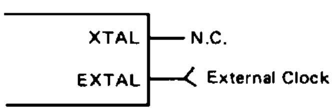
These two pins are used for power supply and GND. Recommended power supply voltage is 5V ±10%. If the operating voltage of the EPROM is 5V ±5%, 5V±5% should be used.

• XTAL, EXTAL

These two pins are connected with parallel resonant fundamental crystal, AT cut. For instance, in order to obtain the system clock 1MHz, a 4MHz resonant fundamental crystal is used because the devide-by-4 circuitry is included. An example of connection circuit is shown in Fig. 12. EXTAL accepts an external clock input of duty 45% to 55% to drive, then internal clock is a quarter the frequency of an external clock. External driving frequency will be less than 4 times as maximum internal clock. For external clock, XTAL pin should be open.



(a) Crystal Interface



(b) External Clock

Figure 12 Connection Circuit

• Standby ($\overline{STBY}$)

This pin is used to place the MCU in the Standby mode. If this goes to "Low" level, the oscillation stops, the internal clock is tied to V_{SS} or V_{CC} and the MCU is reset. In order to retain information in RAM during standby, write "0" into RAM enable bit (RAME). RAME is bit 6 of the RAM Control Register at address $0014. This disables the RAM, so the contents of RAM is guaranteed. For details of the standby mode, see the Standby section.

• Reset ($\overline{RES}$)

This input is used to reset the MCU. $\overline{RES}$ must be held "Low" for at least 20ms when the power starts up. It should be noted that, before clock generator stabilize, the internal state and I/O ports are uncertain, because MCU can not be reset without clock. To reset the MCU during system operation, it must be held "Low" for at least 3 system clock cycles. From the third cycle, all address buses become "High-impedance" and it continues while $\overline{RES}$ is "Low". If $\overline{RES}$ goes to "High", CPU does the following.

(1) I/O Port 2 bits, 2,1,0 are latched into bits PC2, PC1, PC0 of program control register.
(2) The contents of the two Start Addresses, $FFFE, $FFFF are brought to the program counter, from which program starts (see Table 1).
(3) The interrupt mask bit is set. In order to have the CPU recognize the maskable interrupts $\overline{IRQ_1}$ and $\overline{IRQ_2}$, clear it before those are used.

• Enable (E)

This output pin supplies system clock. Output is a single-phase, TTL compatible and 1/4 of the crystal oscillation frequency. It will drive two LS TTL load and 40pF capacitance.

• Non maskable Interrupt ($\overline{NMI}$)

When the falling edge of the input signal of this pin is recognized, NMI sequence starts. The current instruction is continued to complete, even if $\overline{NMI}$ signal is detected. Interrupt mask bit in Condition Code Register has no effect on NMI detection. In response to NMI interrupt, the information of Program Counter, Index Register, Accumulators, and Condition Code Register are stored on the stack. On completion of this sequence, vectoring address $FFFC and $FFFD are generated to load the contents to the program counter. Then the CPU branch to a non maskable interrupt service routine.

• Interrupt Request ($\overline{IRQ_1}$)

This level sensitive input requests maskable interrupt sequence. When $\overline{IRQ_1}$ goes to "Low", the CPU waits until it completes the current instruction that is being executed. Then, if the interrupt mask bit in Condition Code Register is not set, CPU begins interrupt sequence; otherwise, interrupt request is neglected.

Once the sequence has started, the information of Program Counter, Index Register, Accumulators, Condition Code Register are stored on the stack. Then the CPU sets the interrupt mask bit so that no further maskable interrupts may be responded.

Table 1 Interrupt Vectoring memory map

	Vector		Interrupt
	MSB	LSB	
Highest Priority	FFFE	FFFF	$\overline{RES}$
	FFEE	FFEF	TRAP
	FFFC	FFFD	$\overline{NMI}$
	FFFA	FFFB	Software Interrupt (SWI)
	FFF8	FFF9	$\overline{IRQ_1}$ (or $\overline{IS3}$)
	FFF6	FFF7	ICF (Timer Input Capture)
	FFF4	FFF5	OCF (Timer Output Compare)
	FFF2	FFF3	TOF (Timer Overflow)
Lowest Priority	FFF0	FFF1	SCI (RDRF + ORFE + TDRE)

At the end of the cycle, the CPU generates 16 bit vectoring addresses indicating memory addresses $FFF8 and $FFF9, and load the contents to the Program Counter, then branch to an interrupt service routine.

The Internal Interrupt will generate signal ($\overline{IRQ_2}$) which is quite the same as $\overline{IRQ_1}$ except that it will use the vector address $FFF0 to $FFF7.

When $\overline{IRQ_1}$ and $\overline{IRQ_2}$ are generated at the same time, the former precede the latter. Interrupt Mask Bit in the condition code register, if being set, will keep the both interrupts off.

$\overline{IRQ_1}$ has no internal latch. Therefore, if $\overline{IRQ_1}$ is removed during suspension, that $\overline{IRQ_1}$ is ignored.

On occurrence of Address error or Op-code error, TRAP interrupt is invoked. This interrupt has priority next to $\overline{RES}$. Regardless of the Interrupt Mask Bit condition, the CPU will start an interrupt sequence. The vector for this interrupt will be $FFEE, $FFEF.

The following pins are available only in single chip mode.

- **Input Strobe ($\overline{IS3}$) (SC_1)**

This signal controls $\overline{IS3}$ interrupt and the latch of Port 3. When the falling edge of this signal is detected, the flag of Port 3 Control Status Register is set.

For detailed explanation of Port 3 Control Status Register, see the I/O PORT 3 CONTROL STATUS REGISTER section.

- **Output Strobe ($\overline{OS3}$) (SC_2)**

This signal is used to send a strobe to an external device, indicating effective data is on the I/O pins. The timing chart for Output Strobe are shown in Figure 5.

The following pins are available for Expanded Modes.

- **Read/Write (R/$\overline{W}$) (SC_2)**

This TTL compatible output signal indicates peripheral and memory devices whether CPU is in Read ("High"), or in Write ("Low"). The normal stand-by state is Read ("High"). Its output will drive one TTL load and 90pF capacitance.

- **I/O Strobe ($\overline{IOS}$) (SC_1)**

In expanded non multiplexed mode 5 of operation, $\overline{IOS}$ goes to "Low" only when A_9 through A_{15} are "0" and A_8 is "1" This allows external access up to 256 addresses from $0100 to $01FF in memory. The timing chart is shown in Figure 2.

- **Address Strobe (AS) (SC_1)**

In the expanded multiplexed mode, address strobe signal appears at this pin. It is used to latch the lower 8 bits addresses multiplexed with data at Port 3. The 8-bit latch is controlled by address strobe as shown in Figure 18. Thereby, I/O Port 3 can become data bus during E pulse. The timing chart of this signal is shown in Figure 1.

Address Strobe (AS) is sent out even if the internal address area is accessed.

■ PORTS

There are four I/O Ports on HD63P01M1 MCU (three 8-bit ports and one 5-bit port). 2 control pins are connected to one of the 8-bit port. Each port has an independent write-only data direction register to program individual I/O pins for input or output.*

When the bit of associated Data Direction Register is "1". I/O pin is programmed for output, if "0", then programmed for an input.

There are four ports: Port 1, Port 2, Port 3, and Port 4. Addresses of each port and associated Data Direction Registers are shown in Table 2.

* Only one exception is bit 1 of Port 2 which becomes either a data input or a timer output. It cannot be used as an output port.

$\overline{RES}$ does not affect I/O port Data Register. Therefore, just after $\overline{RES}$, Data Register is uncertain. Data Direction Registers are reset.

Table 2 Port and Data Direction Register Addresses

Ports	Port Address	Data Direction Register Address
I/O Port 1	$0002	$0000
I/O Port 2	$0003	$0001
I/O Port 3	$0006	$0004
I/O Port 4	$0007	$0005

- **I/O Port 1**

This is an 8-bit port, each bit being defined individually as input or outputs by associated Data Direction Register. The 8-bit output buffers have three-state capability, maintaining in high impedance state when they are used for input. In order to be read accurately, the voltage on the input lines must be more than 2.0V for logic "1" and less than 0.8 V for logic "0".

These are TTL compatible. After the MCU has been reset, all I/O lines of Port 1 are configured as inputs in all modes except mode 1. In all modes except expanded non multiplexed mode (Mode 1), Port 1 is always parallel I/O. In mode 1, Port 1 will be output line for lower order address lines (A_0 to A_7).

- **I/O Port 2**

This port has five lines, whose I/O direction depends on its data direction register. The 5-bit output buffers have three-state capability, going high impedance state when used as inputs. In order to be read accurately, the voltage on the input lines must be more than 2.0V for logic "1" and less than 0.8V for logic "0". After the MCU has been reset, I/O lines are configured as inputs. These pins on Port 2 (pins 10,9,8 of the chip) are used to program the mode of operation during reset. The values of these three pins during reset are latched into the upper 3 bits (bit 7, 6 and 5) of Port 2 Data Register, which is explained in the MODE SELECTION section.

In all modes, Port 2 can be configured as I/O lines. This port also provides access to the Serial I/O and the Timer. However, note that bit 1 (P_{21}) is the only pin restricted to data input or Timer output.

- **I/O Port 3**

This is an 8-bit port which can be configured as I/O lines, a data bus, or an address bus multiplexed with data bus. Its function depends on hardware operation mode programmed by the user using 3 bits of Port 2 during Reset. Port 3 as a data bus is bi-directional. For an input from peripherals, regular TTL level must be supplied, that is greater than 2.0V for a logic "1" and less than 0.8V for a logic "0". This TTL compatible three-state buffer can drive one TTL load and 90pF capacitance. In the expanded Modes, data direction register will be inhibited after Reset and data direction will depend on the state of the R/$\overline{W}$ line. Function of Port 3 is shown below.

Single Chip Mode (Mode 7)

Parallel Inputs/Outputs as programmed by its corresponding Data Direction Register.

There are two control lines associated with this port in this mode, an input strobe ($\overline{IS3}$) and an output strobe ($\overline{OS3}$), both being used for handshaking. They are controlled by I/O Port 3 Control/Status Register. Function of these two control lines of Port 3 are summarized as follows:

(1) Port 3 input data can be latched using $\overline{IS3}$ (SC_1) as a input strobe signal.
(2) $\overline{OS3}$ can be generated by CPU read or write to Port 3's data register.
(3) $\overline{IRQ_1}$ interrupt can be generated by an $\overline{IS3}$ falling edge.

Port 3 strobe and latch timing is shown in Figs. 5 and 6 respectively.

I/O Port 3 Control/Status Register is explained as follows:

I/O Port 3 Control/Status Register

	7	6	5	4	3	2	1	0
$000F	$\overline{IS3}$ FLAG	$\overline{IS3}$ $\overline{IRQ_1}$ ENABLE	x	OSS	LATCH ENABLE	x	x	x

Bit 0 Not used.

Bit 1 Not used.

Bit 2 Not used.

Bit 3 LATCH ENABLE.

Bit 3 is used to control the input latch of Port 3. If the bit is set at "1", the input data on Port 3 is latched by the falling edge of $\overline{IS3}$. The latch is released by the MCU read to Port 3; now new data can be latched again by $\overline{IS3}$ falling edge. Bit 3 is cleared by a reset. If this bit is "0", $\overline{IS3}$ does not affect I/O Port 3 latch operation.

Bit 4 OSS (Output Strobe Select)

This bit identifies the cause of output strobe generation: a write operation or read operation to I/O Port 3. When the bit is cleared, the strobe will be generated by a read operation to Port 3. When the bit is not cleared, the strobe will be generated by a write operation. Bit 4 is cleared by a reset.

Bit 5 Not used.

Bit 6 $\overline{IS3}$ $\overline{IRQ_1}$ ENABLE.

If this bit is set, $\overline{IRQ_1}$ interrupt by $\overline{IS3}$ Flag is enabled. Otherwise the interrupt is disabled. The bit is cleared by a reset.

Bit 7 $\overline{IS3}$ FLAG.

Bit 7 is a read-only bit which is set by the falling edge of $\overline{IS3}$ (SC_1). It is cleared by a read of the Control/Status Register followed by a read/write of I/O Port 3. The bit is cleared by reset.

Expanded Non Multiplexed Mode (mode 1, 5)

In this mode, Port 3 becomes data bus. ($D_0 \sim D_7$)

Expanded Multiplexed Mode (mode 0, 2, 4, 6)

Port 3 becomes both the data bus ($D_0 \sim D_7$) and lower bits of the address bus ($A_0 \sim A_7$). An address strobe output is "High" while the address is on the port.

- **I/O Port 4**

This is an 8-bit port that becomes either I/O or address outputs depending on the selected operation mode. In order to be read accurately, the voltage at the input lines must be greater than 2.0V for a logic "1", and less than 0.8V for a logic "0". For outputs, each line is TTL compatible and can drive one TTL load and 90pF. Function of Port 4 for each mode is explained below.

Single Chip Mode (Mode 7): Parallel Inputs/Outputs as programmed by its associated data direction register.

Expanded Non Multiplexed Mode (Mode 5): In this mode, Port 4 becomes the lower address lines (A_0 to A_7) by writing "1"s on the data direction register. After reset, this port becomes inputs. In order to use these pins as addresses, they should be programmed as outputs.

When all of the eight bits are not required as addresses, the remaining lines can be used as I/O lines (Inputs only).

Expanded Non Multiplexed Mode (Mode 1): In this mode, Port 4 becomes output for upper order address lines (A_8 to A_{15}) regardless of the value of the direction register.

Expanded Multiplexed Mode (Mode 6): In this mode, Port 4 becomes the upper address lines (A_8 to A_{15}). After reset, this port becomes inputs. In order to use these pins as addresses, they should be programmed as outputs. When all of the eight bits are not required, the remaining lines can be used as I/O lines (input only).

Expanded Multiplexed Mode (Mode 0, 2, 4): In this mode, Port 4 becomes output for upper order address lines (A_8 to A_{15}) regardless of the value of data direction register.

The relation between each mode and I/O Port 1 to 4 is summarized in Table 3.

■ MODE SELECTION

The operation mode after the reset must be determined by the user wiring the 10, 9, and 8th pins externally. These three pins are lower order bits; I/O 0, I/O 1, I/O 2 of Port 2. They are latched into the control bits PC0, PC1, PC2 of I/O Port 2 register when reset goes "High". I/O Port 2 Register is shown below.

Port 2 DATA REGISTER

	7	6	5	4	3	2	1	0
$0003	PC2	PC1	PC0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0

An example of external hardware used for Mode Selection is shown in Fig. 13. The HD14053B is used to separate the peripheral device from the MCU during reset. It is necessary if the data may conflict between peripheral device and Mode generation circuit.

No mode can be changed through software because the bits 5, 6, and 7 of Port 2 Data Register are read-only. The mode selection of the HD63P01M1 is shown in Table 4.

The HD63P01M1 operates in three basic modes: (1) Single Chip Mode; (2) Expanded Multiplexed Mode (compatible with the HMCS6800 peripheral family), (3) Expanded Non Multiplexed Mode (compatible with HMCS6800 peripheral family).

- **Single Chip Mode (Mode 7)**

In the Single Chip Mode, all ports will become I/O. This is shown in Figure 15. In this mode, SC_1, SC_2 pins are configured for control lines of Port 3 and can be used as input strobe ($\overline{IS3}$) and output strobe ($\overline{OS3}$) for data handshaking.

- **Expanded Multiplexed Mode (Mode 0, 2, 4, 6)**

In this mode, Port 4 is configured for I/O (inputs only) or address lines. The data bus and the lower order address bus are multiplexed in Port 3 and can be separated by the Address Strobe.

Port 2 is configured for 5 parallel I/O or Serial I/O, or Timer, or any combination thereof. Port 1 is configured for 8 parallel I/O. In this mode, HD63P01M1 is expandable up to 65k words (See Fig. 16).

- **Expanded Non Multiplexed Mode (Mode 1, 5)**

In this mode, the HD63P01M1 can directly address HMCS6800 peripherals with no address latch. In mode 5, Port 3 becomes a data bus. Port 4 becomes A_0 to A_7 address bus or partial address bus and I/O (inputs only). Port 2 is configured for a parallel I/O, Serial I/O, Timer or any combination thereof. Port 1 is configured as a parallel I/O only. In this mode, HD63P01M1 is expandable to 256 locations. In mode 1, Port 3 becomes a data bus and Port 1 becomes A_0 to A_7 address bus, and Port 4 becomes A_8 to A_{15} address bus.

In this mode, the HD63P01M1 is expandable to 65k bytes with no address latch. (See Fig. 17)

- **Lower Order Address Bus Latch**
  Because the data bus is multiplexed with the lower order address bus in Port 3 in the expanded multiplexed mode, address bits must be latched. It requires the 74LS373 Transparent octal D-type to latch the LSB. Latch connection of the HD63P01M1 is shown in Figure 18.

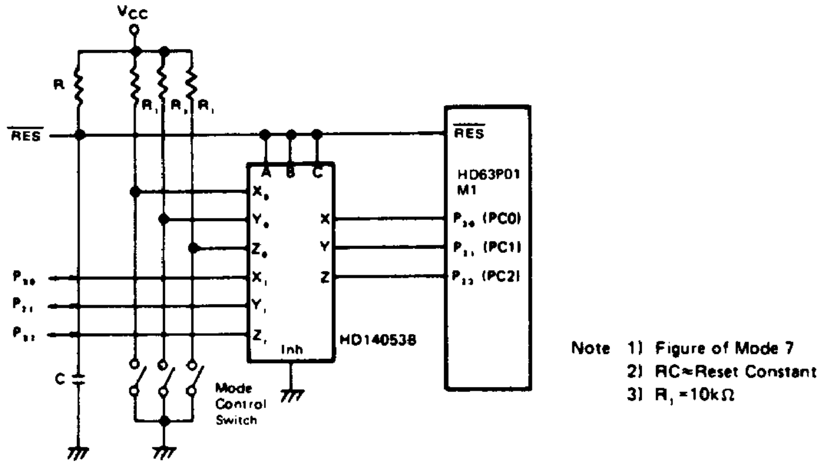
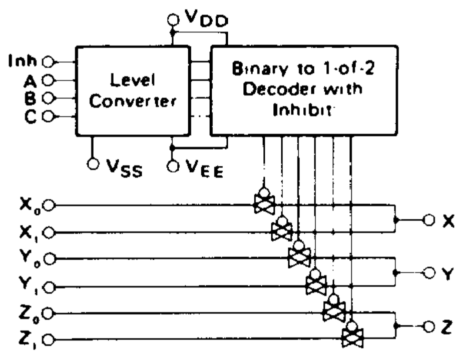


Figure 13 Recommended Circuit for Mode Selection



Truth Table

Control Input				On Switch		
Inhibit	Select			HD14053B		
	C	B	A			
0	0	0	0	Z_0	Y_0	X_0
0	0	0	1	Z_0	Y_0	X_1
0	0	1	0	Z_0	Y_1	X_0
0	0	1	1	Z_0	Y_1	X_1
0	1	0	0	Z_1	Y_0	X_0
0	1	0	1	Z_1	Y_0	X_1
0	1	1	0	Z_1	Y_1	X_0
0	1	1	1	Z_1	Y_1	X_1
1	X	X	X	–		

Figure 14 HD14053B Multiplexers/De-Multiplexers

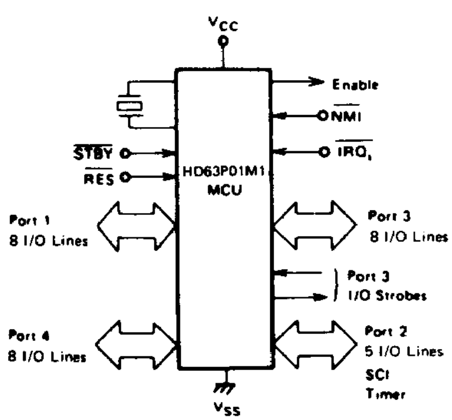


Figure 15 HD63P01M1 MCU Single-Chip Mode

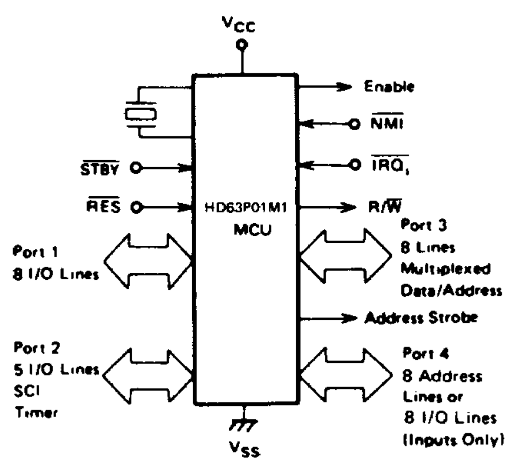
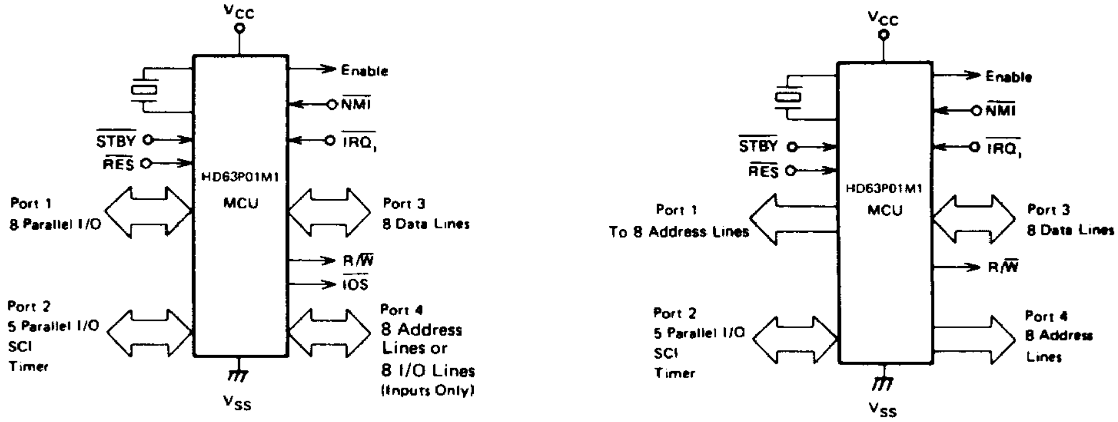


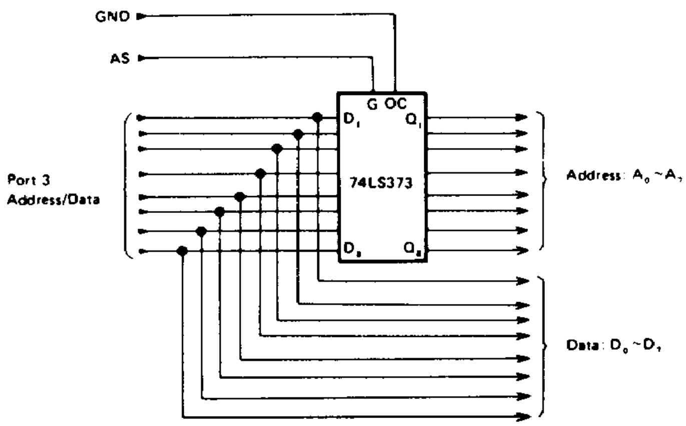
Figure 16 HD63P01M1 MCU Expanded Multiplexed Mode



(a) Mode 5

(b) Mode 1

Figure 17 HD63P01M1 MCU Expanded Non Multiplexed Mode



Function Table

Output Control (OC)	Enable G	Enable D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Figure 18 Latch Connection

- **Summary of Mode and MCU Signal**

This section gives a description of the MCU signals for the various modes. SC_1 and SC_2 are signals which vary with the mode.

Table 3 Feature of each mode and lines

MODE		PORT 1 Eight Lines	PORT 2 Five Lines	PORT 3 Eight Lines	PORT 4 Eight Lines	SC_1	SC_2
SINGLE CHIP	(Mode 7)	I/O	I/O	I/O	I/O	$\overline{IS3}$ (I)	$\overline{OS3}$ (O)
EXPANDED MUX (Mode 0, 2, 4, 6)		I/O	I/O	ADDRESS BUS ($A_0 \sim A_7$) DATA BUS ($D_0 \sim D_7$)	ADDRESS BUS* ($A_8 \sim A_{15}$)	AS(O)	R/$\overline{W}$(O)
EXPANDED NON-MUX	(Mode 5)	I/O	I/O	DATA BUS ($D_0 \sim D_7$)	ADDRESS BUS* ($A_0 \sim A_7$)	$\overline{IOS}$(O)	R/$\overline{W}$(O)
	(Mode 1)	ADDRESS BUS ($A_0 \sim A_7$)	I/O	DATA BUS ($D_0 \sim D_7$)	ADDRESS BUS ($A_8 \sim A_{15}$)	Not Used	R/$\overline{W}$(O)

*These lines can be substituted for I/O (Input Only) (except Mode 0, 2, 4).

I = Input
O = Output
R/$\overline{W}$ = Read/Write
$\overline{IS3}$ = Input Strobe
$\overline{OS3}$ = Output Strobe
$\overline{IOS}$ = I/O Select
SC = Strobe Control
AS = Address Strobe

Table 4 Mode Selection Summary

Mode	P_{22} (PC2)	P_{21} (PC1)	P_{20} (PC0)	ROM	RAM	Interrupt Vectors	Bus Mode	Operating Mode
7	H	H	H	I	I	I	I	Single Chip
6	H	H	L	I	I	I	MUX(3)	Multiplexed/Partial Decode
5	H	L	H	I	I	I	NMUX(3)	Non-Multiplexed/Partial Decode
4	H	L	L	E(1)	I	E	MUX	Multiplexed/RAM
3	L	H	H	—	—	—	—	Not Used
2	L	H	L	E(1)	I	E	MUX	Multiplexed/RAM
1	L	L	H	E(1)	I	E	NMUX	Non-Multiplexed
0	L	L	L	I	I	I(2)	MUX	Multiplexed Test

LEGEND :
- I – Internal
- E – External
- MUX – Multiplexed
- NMUX – Non-Multiplexed
- L – Logic "0"
- H – Logic "1"

(NOTES)
1) Internal ROM is disabled.
2) Reset vector is external for 4 cycles after $\overline{RES}$ goes "high".
3) Idle lines of Port 4 address outputs can be assigned to Input Port.

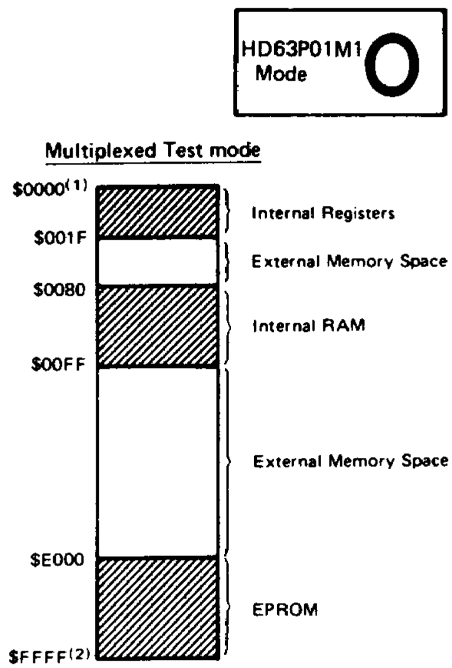
■ Memory Map

The MCU can provide up to 65k byte address space depending on the operating mode. Fig. 19 shows a memory map for each operating mode. The first 32 locations of each map are for the MCU's internal register only, as shown in Table 5.

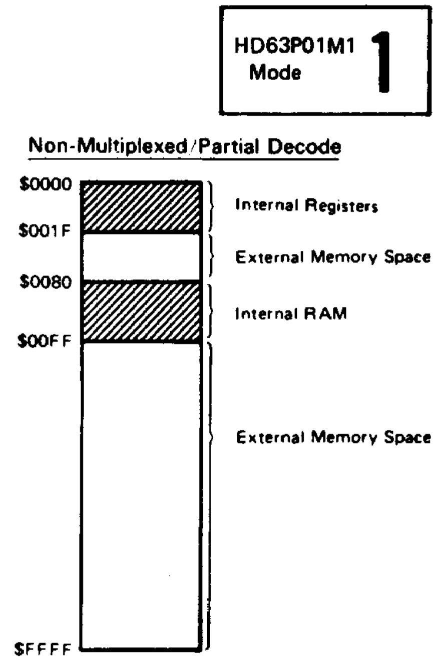
Table 5 Internal Register Area

Register	Address
Port 1 Data Direction Register****	00*
Port 2 Data Direction Register****	01
Port 1 Data Register	02*
Port 2 Data Register	03
Port 3 Data Direction Register****	04**
Port 4 Data Direction Register****	05***
Port 3 Data Register	06**
Port 4 Data Register	07***
Timer Control and Status Register	08
Counter (High Byte)	09
Counter (Low Byte)	0A
Output Compare Register (High Byte)	0B
Output Compare Register (Low Byte)	0C
Input Capture Register (High Byte)	0D
Input Capture Register (Low Byte)	0E
Port 3 Control and Status Register	0F**
Rate and Mode Control Register	10
Transmit/Receive Control and Status Register	11
Receive Data Register	12
Transmit Data Register	13
RAM Control Register	14
Reserved	15-1F

* External address in Mode 1
** External address in Modes 0, 1, 2, 4, 6; cannot be accessed in Mode 5
*** External address in Modes 0, 1, 2, 4
**** 1 = Output, 0 = Input



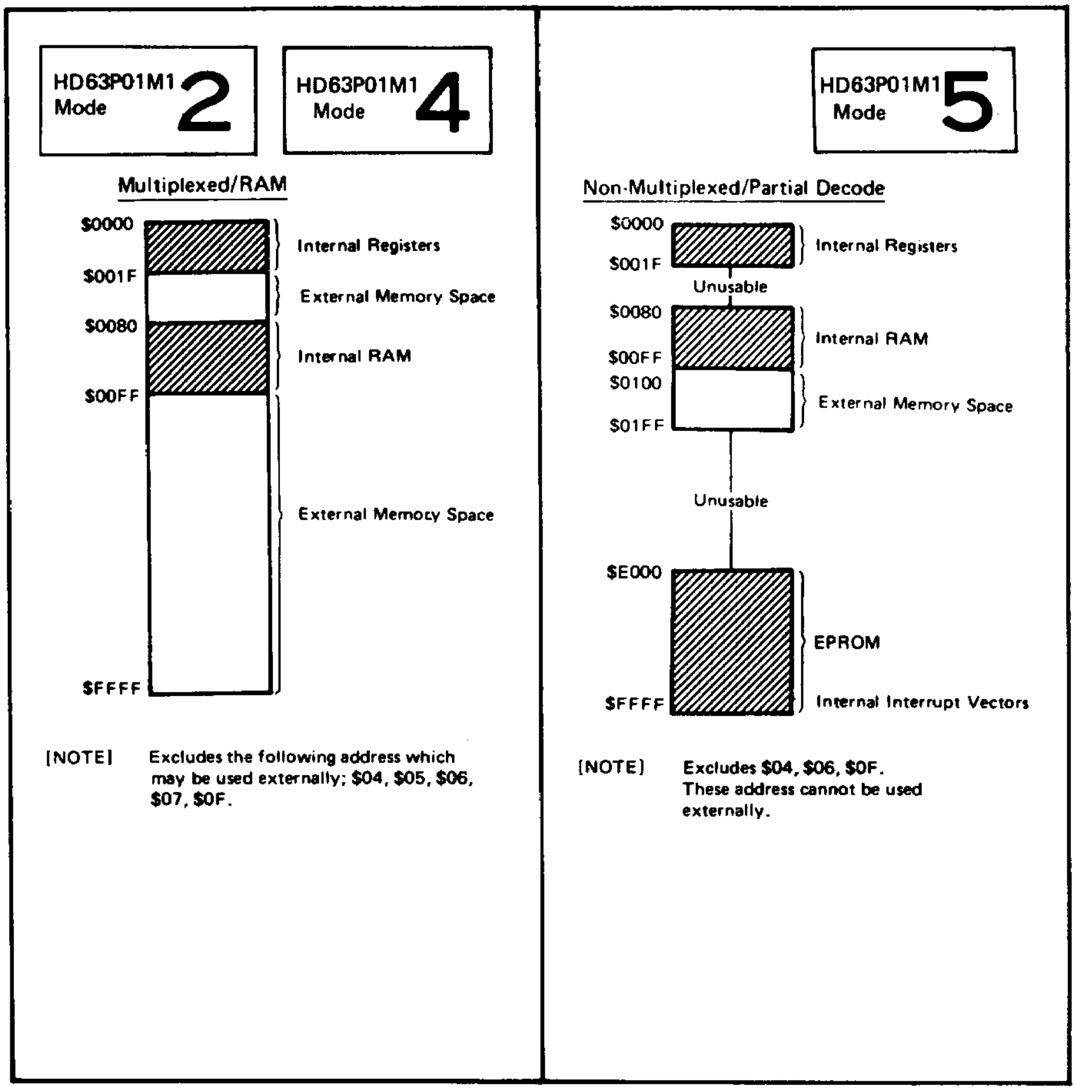
[NOTES]
1) Excludes the following addresses which may be used externally: $04, $05, $06, $07 and $0F.
2) Addresses $FFFE and $FFFF are considered external if accessed within 4 cycles after a positive edge of $\overline{\text{RES}}$ and internal at all other times.
3) After 4 CPU cycles, there must be no overlapping of internal and external memory spaces to avoid driving the data bus with more than one device.
4) This mode is the only mode which is used for testing.



[NOTE]
Excludes the following addresses which may be used externally; $00, $02, $04, $05, $06, $07 and $0F.

(to be continued)

Figure 19 HD63P01M1 Memory Maps



(to be continued)

Figure 19 HD63P01M1 Memory Maps

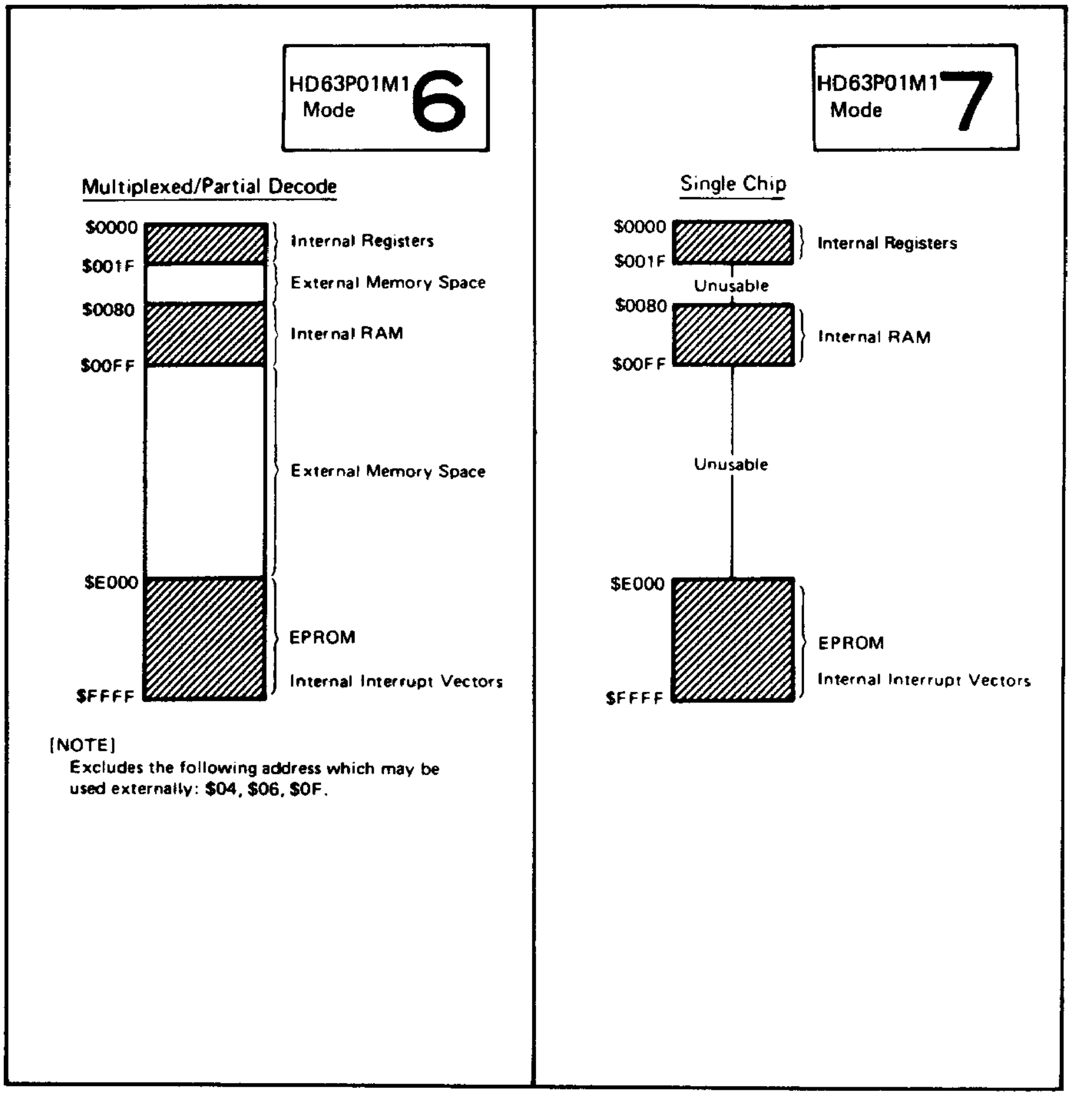


Figure 19 HD63P01M1 Memory Maps

■ PROGRAMMABLE TIMER

The HD63P01M1 contains 16-bit programmable timer which may be used to make measurement of input waveform. In addition to that it can generate an output waveform by itself. For both input and output waveform, the pulse width may vary from a few microseconds to several seconds.

The timer hardware consists of

- an 8-bit control and status register
- a 16-bit free running counter
- a 16-bit output compare register,
- a 16-bit input capture register

A block diagram of the timer is shown in Figure 20.

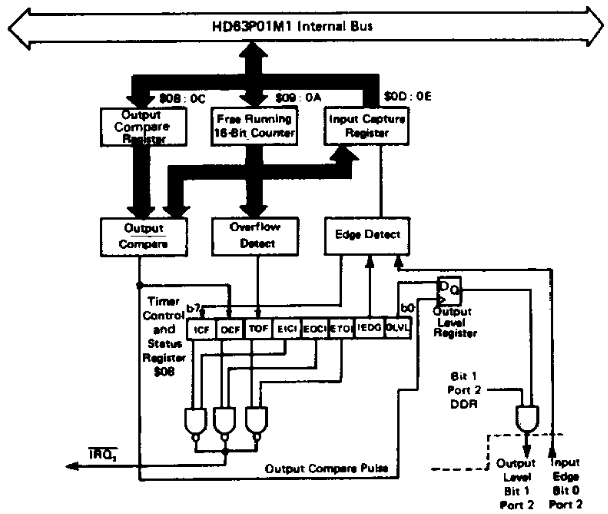


Figure 20 Programmable Timer Block Diagram

● **Free Running Counter ($0009: $000A)**

The key element in the programmable timer is a 16-bit free running counter, that is driven by an E (Enable) clock to increment its values. The counter value will be read out by the CPU software at any time with no effects on the counter. Reset will clear the counter.

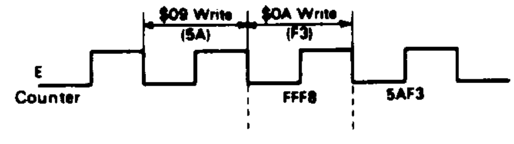
When the MSB of this counter is read, the LSB is stored in temporary latch. The data is fetched from this latch by the subsequent read of LSB. Thus consistent double byte data can be read from the counter.

When the CPU writes arbitrary data to the MSB ($09), the value of $FFF8 is being pre-set to the counter ($09, $0A) regardless of the write data value. Then the CPU writes arbitrary data to the LSB ($0A), the data is set to the "Low" byte of the counter, at the same time, the data preceedingly written in the MSB ($09) is set to "High" byte of the counter.

When the data is written to this counter, a double byte store instruction (ex. STD) must be used. If only the MSB of counter is written, the counter is set to $FFF8.

The counter value written to the counter using the double byte store instruction is shown in Figure 21.

To write to the counter may disturb serial operations, so it should be inhibited during using the SCI in internal clock mode.



($AF3 written to the counter)

Figure 21 Counter Write Timing

● **Output Compare Register ($000B:$000C)**

This is a 16-bit read/write register which is used to control an output waveform. The contents of this register are constantly being compared with current value of the free running counter.

When the contents match with the value of the free running counter, a flag (OCF) in the timer control/status register (TCSR) is set and the current value of an output level Bit (OLVL) in the TCSR is transferred to Port 2 bit 1. When bit 1 of the Port 2 data direction register is "1" (output), the OLVL value will appear on the bit 1 of Port 2. Then, the value of Output Compare Register and Output level bit may be changed for the next compare.

The output compare register is set to $FFFF during reset.

The compare function is inhibited at the cycle of writing to the high byte of the output compare register and at the cycle just after that to ensure valid compare. It is also inhibited in same manner at writing to the free running counter.

In order to write a data to Output Compare Register, a double byte store instruction (ex. STD) must be used.

● **Input Capture Register ($000D:$000E)**

The input capture register is a 16-bit read-only register used to hold the current value of free running counter when the proper transition of an external input signal occurs.

The input transition change required to trigger the counter transfer is controlled by the input edge bit (IEDG).

To allow the external input signal to go in the edge detect unit, the bit of the Data Direction Register corresponding to bit 0 of Port 2 must have been cleared (to zero).

To insure input capture in all cases, the width of an input pulse requires at least 2 Enable cycles.

● **Timer Control/Status Register (TCSR) ($0008)**

This is an 8-bit register. All 8 bits are readable and the lower 5-bit may be written. The upper 3 bits are read-only, indicating the timer status information as is shown below.

(1) A proper transition has been detected on the input pin (ICF).
(2) A match has been found between the value in the free running counter and the output compare register (OCF).
(3) When counting up to $0000 (TOF).

Each flag has an individual enable bit in TCSR which determines whether or not an interrupt request may occur ($\overline{IRQ_2}$). If the I-bit in Condition Code Register has been cleared, a priority vectored address occurs corresponding to each flag. A description of each bit is as follows.

Timer Control / Status Register

7	6	5	4	3	2	1	0	
ICF	OCF	TOF	EICI	EOCI	ETOI	IEDG	OLVL	$0008

Bit 0 OLVL (Output Level); When a match is found in the value between the counter and the output com-

pare register, this bit is transferred to the Port 2 bit 1. If the DDR corresponding to Port 2 bit 1 is set "1", the value will appear on the output pin of Port 2 bit 1.

Bit 1 IEDG (Input Edge): This bit control which transition of an input of Port 2 bit 0 will trigger the data transfer from the counter to the input capture register. The DDR corresponding to Port 2 bit 0 must be cleared in advance of using this function.
When IEDG = 0, trigger takes place on a negative edge ("High" to "Low" transition). When IEDG = 1, trigger takes place on a positive edge ("Low" to "High" transition).

Bit 2 ETOI (Enable Timer Overflow Interrupt); When set, this bit enables TOF interrupt to generate the interrupt request ($\overline{IRQ_2}$). When cleared, the interrupt is inhibited.

Bit 3 EOCI (Enable Output Compare Interrupt); When set, this bit enables OCF interrupt to generate the interrupt request ($\overline{IRQ_2}$). When cleared, the interrupt is inhibited.

Bit 4 EICI (Enable Input Capture Interrupt); When set, this bit enables ICF interrupt to generate the interrupt request ($\overline{IRQ_2}$). When cleared, the interrupt is inhibited.

Bit 5 TOF (Timer Over Flow Flag); This read-only bit is set at the transition of $FFFF to $0000 of the counter. It is cleared by CPU read of TCSR (with TOF set) followed by an CPU read of the counter ($0009).

Bit 6 OCF (Output Compare Flag); This read-only bit is set when a match is found in the value between the output compare register and the counter. It is cleared by a read of TCSR (with OCF set) followed by an CPU write to the output compare register ($000B or $000C).

Bit 7 ICF (Input Capture Flag); The read-only bit is set by a proper transition on the input, and is cleared by a read of TCSR (with ICF set) followed by an CPU read of Input Capture Register ($000D).

Reset will clear each bit of Timer Control and Status Register.

■ SERIAL COMMUNICATION INTERFACE

The HD63P01M1 contains a full-duplex asynchronous Serial Communication Interface (SCI). SCI may select the several kinds of the data rate. It consists of a transmitter and a receiver which operate independently but with the same data format and the same data rate. Both the transmitter and receiver communicate with the CPU via the data bus and with the outside world through Port 2 bit 2, 3 and 4. Description of hardware, software and register is as follows.

● Wake-Up Feature

In typical multiprocessor applications the software protocol will usually have the designated address at the initial byte of the message. The purpose of Wake-Up feature is to have the non-selected MCU neglect the remainder of the message. Thus the non-selected MCU can inhibit the all further interrupt process until the next message begins.

Wake-Up feature is re-enabled by a ten consecutive "1"s which indicates an idle transmit line. Therefore software protocol must put an idle period between the messages and must prevent it within the message.

With this hardware feature, the non-selected MCU is re-enabled or ("waked-up") by the next message.

● Programmable Options

The HD63P01M1 has the following programmable features.

- data format; standard mark/space (NRZ)
- clock source; external or internal
- baud rate; one of 4 rates per given E clock frequency or 1/8 of external clock
- wake-up feature; enabled or disabled
- interrupt requests; enabled or masked individually for transmitter and receiver
- clock output; internal clock enabled or disabled to Port 2 bit 2
- Port 2 (bits 3, 4); dedicated or not dedicated to serial I/O individually

● Serial Communication Hardware

The serial communications hardware is controlled by 4 registers as shown in Figure 22. The registers include:

- an 8-bit control/status register
- a 4-bit rate/mode control register (write-only)
- an 8-bit read-only receive data register
- an 8-bit write-only transmit data register

Besides these 4 registers, Serial I/O utilizes Port 2 bit 3 (input) and bit 4 (output). Port 2 bit 2 can be used when an option is selected for the internal-clock-out or the external-clock-in.

● Transmit/Receive Control Status Register (TRCSR)

TRCS Register consists of 8 bits which all may be read while only bits 0 to 4 may be written. The register is initialized to $20 on $\overline{RES}$. The bits of the TRCS register are explained below.

Transmit / Receive Control Status Register

7	6	5	4	3	2	1	0	
RDRF	ORFE	TDRE	RIE	RE	TIE	TE	WU	ADDR $0011

Bit 0 WU (Wake Up); Set by software and cleared by hardware on receipt of ten consecutive "1"s. While this bit is "1", RDRF and ORFE flags are not set even if data are received or errors are detected. Therefore received data are ignored. It should be noted that RE flag must have already been set in advance of WU flag's set.

Bit 1 TE (Transmit Enable); This bit enables transmitter. When this bit is set, bit 4 of Port 2 DDR is also forced to be set. It remains set even if TE is cleared. Preamble of ten consecutive "1"s is transmitted just after this bit is set, and then transmitter becomes ready to send data.
If this bit is cleared, the transmitter is disabled and serial I/O affects nothing on Port 2 bit 4.

Bit 2 TIE (Transmit Interrupt Enable); When this bit is set, TDRE (bit 5) causes an $\overline{IRQ_2}$ interrupt. When cleared TDRE interrupt is masked.

Bit 3 RE (Receive Enable); When set, Port 2 bit 3 can be used as an input of receive regardless of DDR value for this bit. When cleared, the receiver is disabled.

Bit 4 RIE (Receive Interrupt Enable); When this bit is set, RDRF (bit 7) or ORFE (bit 6) cause an $\overline{IRQ_2}$ interrupt. When cleared, this interrupt is masked.

Bit 5 TDRE (Transmit Data Register Empty); When the data is transferred from the Transmit Data Register to Output Shift Register, this bit is set by hardware. The bit is cleared by reading the status register followed by writing the next new data into the Transmit Data Register. TDRE is initialized to 1 by $\overline{RES}$.

Bit 6 ORFE (Over Run Framing Error); When overrun or framing error occurs (receive only), this bit is set by hardware. Over Run Error occurs if the attempt is made to transfer the new byte to the receive data register while the RDRF is "1". Framing Error occurs when the bit counter is not synchronized with the boundary of the byte in the receiving bit stream. When Framing Error is detected, RDRF is not set. Therefore Framing Error can be distinguished from Overrun Error. That is, if ORFE is "1" and RDRF is "1", Overrun Error is detected. Otherwise Framing Error occurs. The bit is cleared by reading the status register followed by reading the receive data register, or by $\overline{RES}$.

Bit 7 RDRF (Receive Data Register Full); This bit is set by hardware when the data is transferred from the receive shift register to the receive data register. It is cleared by reading the status register followed by reading the receive data register, or by $\overline{RES}$.

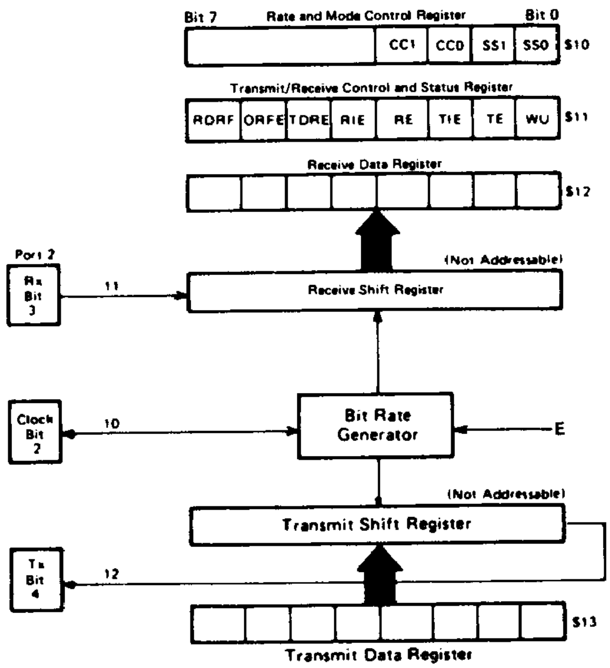
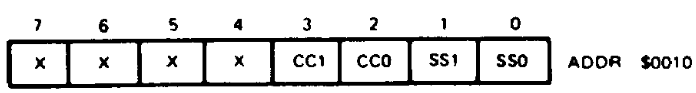


Figure 22 Serial I/O Register



Transfer Rate / Mode Control Register

Table 6 SCI Bit Times and Transfer Rates

		XTAL	2.4576 MHz	4.0 MHz	4.9152MHz
SS1	SS0	E	614.4 kHz	1.0 MHz	1.2288MHz
0	0	E ÷ 16	26 μs/38,400 Baud	16 μs/62,500 Baud	13 μs/76,800Baud
0	1	E ÷ 128	208μs/4,800 Baud	128 μs/7812.5 Baud	104.2μs/ 9,600Baud
1	0	E ÷ 1024	1.67ms/600 Baud	1.024ms/976.6 Baud	833.3μs/ 1,200Baud
1	1	E ÷ 4096	6.67ms/150 Baud	4.096ms/244.1 Baud	3.333ms/ 300Baud

Table 7 SCI Format and Clock Source Control

CC1 : CC0	Format	Clock Source	Port 2 Bit 2	Port 2 Bit 3	Port 2 Bit 4
0 0	–	–	–	–	–
0 1	NRZ	Internal	Not Used***	**	**
1 0	NRZ	Internal	Output*	**	**
1 1	NRZ	External	Input	**	**

* Clock output is available regardless of values for bits RE and TE.
** Bit 3 is used for serial input if RE = "1" in TRCS.
Bit 4 is used for serial output if TE = "1" in TRCS.
*** This pin can be used as I/O port.

- **Transfer rate/Mode Control Register (RMCR)**

The register controls the following serial I/O functions:
- Bauds rate • data format • clock source
- Port 2 bit 2 feature

It is 4-bit write-only register, cleared by $\overline{RES}$. The 4 bits are considered as a pair of 2-bit fields. The lower 2 bits control the bit rate of internal clock while the upper 2 bits control the format and the clock select logic.

Bit 0 SS0 }
Bit 1 SS1 } Speed Select

These bits select the Baud rate for the internal clock. The rates selectable are function of E clock frequency of the CPU. Table 6 lists the available Baud Rates.

Bit2 CC0 }
Bit 3 CC1 } Clock Control/Format Select

They control the data format and the clock select logic. Table 7 defines the bit field.

- **Internally Generated Clock**

If the user wish to use externally an internal clock of the serial I/O, the following requirements should be noted.
- CC1, CC0 must be set to "10".
- The maximum clock rate must be E/16.
- The clock rate is equal to the bit rate.
- The values of RE and TE have no effect.

- **Externally Generated Clock**

If the user wish to supply an external clock to the Serial I/O, the following requirements should be noted.
- The CC1, CC0 must be set to "11" (See Table 7).
- The external clock must be set to 8 times of the desired baud rate.
- The maximum external clock frequency is E/2 clock.

- **Serial Operations**

The serial I/O hardware must be initialized by the software before operation. The sequence will be normally as follows.
- Writing the desired operation control bits of the Rate and Mode Control Register.
- Writing the desired operation control bits of the TRCS register.

If Port 2 bit 3, 4 are used for serial I/O, TE, RE bits may be kept set. When TE, RE bit are cleared during SCI operation, and subsequently set again, it should be noted that TE, RE must be kept "0" for at least one bit time of the current baud rate. If TE, RE are set again within one bit time, there may be the case where the initializing of internal function for transmitter and receiver does not take place correctly.

- **Transmit Operation**

Data transmission is enabled by the TE bit in the TRCS register. When set, the output of the transmit shift register is connected with Port 2 bit 4 which is unconditionally configured as an output.

After $\overline{RES}$, the user should initialize both the RMC register and the TRCS register for desired operation. Setting the TE bit causes a transmission of ten-bit preamble of "1"s. Following the preamble, internal synchronization is established and the transmitter is ready to operate. Then either of the following states exists.

(1) If the transmit data register is empty (TDRE = 1), the consecutive "1"s are transmitted indicating an idle states.

(2) If the data has been loaded into the Transmit Data Register (TDRE = 0), it is transferred to the output shift register and data transmission begins.

During the data transfer, the start bit ("0") is first transferred. Next the 8-bit data (beginning at bit 0) and finally the stop bit ("1"). When the contents of the Transmit Data Register is transferred to the output shift register, the hardware sets the TDRE flag bit: If the CPU fails to respond to the flag within the proper time, TDRE is kept set and then a continuous string of 1's is sent until the data is supplied to the data register.

- **Receive Operation**

The receive operation is enabled by the RE bit. The serial input is connected with Port 2 bit 3. The receiver operation is determined by the contents of the TRCS and RMC register. The received bit stream is synchronized by the first "0" (start bit). During 10-bit time, the data is strobed approximately at the center of each bit. If the tenth bit is not "1" (stop bit), the system assumes a framing error and the ORFE is set.

If the tenth bit is "1", the data is transferred to the receive data register, and the RDRF flag is set. If the tenth bit of the next data is received and still RDRF is preserved set, then ORFE is set indicating that an overrun error has occurred.

After the CPU read of the status register as a response to RDRF flag or ORFE flag, followed by the CPU read of the receive data register, RDRF or ORFE will be cleared.

■ RAM CONTROL REGISTER

The register assigned to the address $0014 gives a status information about standby RAM.

RAM Control Register

	7	6	5	4	3	2	1	0
$0014	STBY PWR	RAME	x	x	x	x	x	x

Bit 0 Not used.
Bit 1 Not used.
Bit 2 Not used.

Bit 3 Not used.
Bit 4 Not used.
Bit 5 Not used.
Bit 6 RAM Enable.

Using this control bit, the user can disable the RAM. RAM Enable bit is set on the positive edge of $\overline{RES}$ and RAM is enabled. The program can write "1" or "0". If RAME is cleared, the RAM address becomes external address and the CPU may read the data from the outside memory.

Bit 7 Standby Bit

This bit can be read or written by the user program. It is cleared when the V_{CC} voltage is removed. Normally this bit is set by the program before going into stand-by mode. When the CPU recovers from stand-by mode, this bit should be checked. If it is "1", the data of the RAM is retained during stand-by and it is valid.

■ GENERAL DESCRIPTION OF INSTRUCTION SET

The HD63P01M1 has an upward object code compatible with the HD6801 to utilize all instruction sets of the HMCS6800. The execution time of the key instruction is reduced to increase the system through-put. In addition, the bit operation instruction, the exchange instruction between the index and the accumulator, the sleep instruction are added. This section describes:

- CPU programming model (See Fig. 23)
- Addressing modes
- Accumulator and memory manipulation instructions (See Table 8)
- New instructions
- Index register and stack manipulation instructions (See Table 9)
- Jump and branch instructions (See Table 10)
- Condition code register manipulation instructions (See Table 11)
- Op-code map (See Table 12)
- Cycle-by-Cycle Operation (See Table 13)

● CPU Programming Model

The programming model for the HD63P01M1 is shown in Figure 23. The double accumulator is physically the same as the accumulator A concatenated with the accumulator B, so that the contents of A and B is changed with executing operation of an accumulator D.

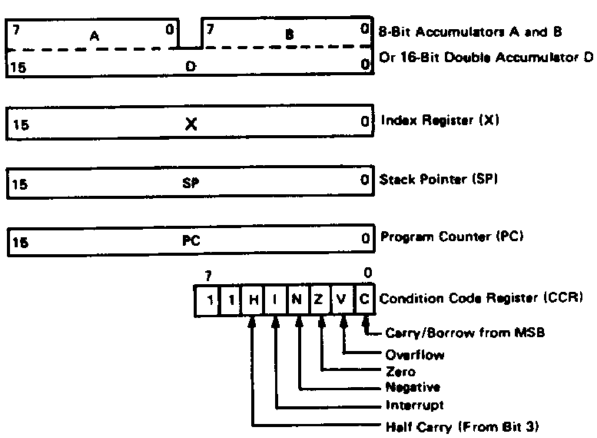


Figure 23 CPU Programming Model

● CPU Addressing Modes

The HD63P01M1 has seven address modes which depend on both of the instruction type and the code. The address mode for every instruction is shown along with execution time given in terms of machine cycles (Table 8 to 12). When the clock frequency is 4 MHz, the machine cycles will be microseconds.

Accumulator (ACCX) Addressing

Only the accumulator (A or B) is addressed. Either accumulator A or B is specified by one-byte instructions.

Immediate Addressing

In this mode, the operand is stored in the second byte of the instruction except that the operand in LDS and LDX, etc are stored in the second and the third byte. These are two or three-byte instructions.

Direct Addressing

In this mode, the second byte of instruction indicates the address where the operand is stored. Direct addressing allows the user to directly address the lowest 256 Bytes in the machine locations zero through 255. Improved execution times are achieved by storing data in these locations. For system configuration, it is recommended that these locations should be RAM and be utilized preferably for user's data realm. These are two-byte instructions except the AIM, OIM, EIM and TIM which have three- byte.

Extended Addressing

In this mode, the second byte indicates the upper 8 bits addresses where the operand is stored, while the third byte indicates the lower 8 bits. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing

In this mode, the contents of the second byte is added to the lower 8 bits in the Index Register. For each of AIM, OIM, EIM and TIM instructions, the contents of the third byte are added to the lower 8 bits in the Index Register. In addition, the resulting "carry" is added to the upper 8 bits in the Index Register. The result is used for addressing memory. Because the modified address is held in the Temporary Address Register, there is no change to the Index Register. These are two-byte instructions but AIM, OIM, EIM, TIM have three-byte.

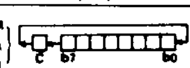
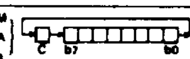
Implied Addressing

In this mode, the instruction itself gives the address; stack pointer, index register, etc. These are 1-byte instructions.

Relative Addressing

In this mode, the contents of the second byte is added to the lower 8 bits in the program counter. The resulting carry or borrow is added to the upper 8 bits. This helps the user to address the data within a range of −126 to +129 bytes of the current execution instruction. These are two-byte instructions.

Table 8 Accumulator, Memory Manipulation Instructions

Operations	Mnemonic	Addressing Modes															Boolean/ Arithmetic Operation	Condition Code Register					
		IMMED			DIRECT			INDEX			EXTEND			IMPLIED				5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#		H	I	N	Z	V	C
Add	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Double	ADDD	C3	3	3	D3	4	2	E3	5	2	F3	5	3				A : B + M : M + 1 → A : B	•	•	↕	↕	↕	↕
Add Accumulators	ABA													1B	1	1	A + B → A	↕	•	↕	↕	↕	↕
Add With Carry	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
AND	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3				A·M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3				B·M → B	•	•	↕	↕	R	•
Bit Test	BIT A	85	2	2	95	3	2	A5	4	2	B5	4	3				A·M	•	•	↕	↕	R	•
	BIT B	C5	2	2	D5	3	2	E5	4	2	F5	4	3				B·M	•	•	↕	↕	R	•
Clear	CLR							6F	5	2	7F	5	3				00 → M	•	•	R	S	R	R
	CLRA													4F	1	1	00 → A	•	•	R	S	R	R
	CLRB													5F	1	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
Compare Accumulators	CBA													11	1	1	A − B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	6	2	73	6	3				$\overline{M}$ → M	•	•	↕	↕	R	S
	COMA													43	1	1	$\overline{A}$ → A	•	•	↕	↕	R	S
	COMB													53	1	1	$\overline{B}$ → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	6	2	70	6	3				00 − M → M	•	•	↕	↕	①	②
	NEGA													40	1	1	00 − A → A	•	•	↕	↕	①	②
	NEGB													50	1	1	00 − B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts binary add of BCD characters into BCD format	•	•	↕	↕	↕	③
Decrement	DEC							6A	6	2	7A	6	3				M − 1 → M	•	•	↕	↕	④	•
	DECA													4A	1	1	A − 1 → A	•	•	↕	↕	④	•
	DECB													5A	1	1	B − 1 → B	•	•	↕	↕	④	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3				A ⊕ M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3				B ⊕ M → B	•	•	↕	↕	R	•
Increment	INC							6C	6	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	1	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	1	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Accumulator	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3				M → B	•	•	↕	↕	R	•
Load Double Accumulator	LDD	CC	3	3	DC	4	2	EC	5	2	FC	5	3				M + 1 → B, M → A	•	•	↕	↕	R	•
Multiply Unsigned	MUL													3D	7	1	A x B → A : B	•	•	•	•	•	⑪
OR, Inclusive	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → Msp, SP − 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → Msp, SP − 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	3	1	SP + 1 → SP, Msp → A	•	•	•	•	•	•
	PULB													33	3	1	SP + 1 → SP, Msp → B	•	•	•	•	•	•
Rotate Left	ROL							69	6	2	79	6	3				M A B 	•	•	↕	↕	⑥	↕
	ROLA													49	1	1		•	•	↕	↕	⑥	↕
	ROLB													59	1	1		•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	6	2	76	6	3				M A B 	•	•	↕	↕	⑥	↕
	RORA													46	1	1		•	•	↕	↕	⑥	↕
	RORB													56	1	1		•	•	↕	↕	⑥	↕

Note) Condition Code Register will be explained in Note of Table 11.

(to be continued)

Table 8 Accumulator, Memory Manipulation Instructions

Operations	Mnemonic	Addressing Modes															Boolean/ Arithmetic Operation	Condition Code Register					
		IMMED			DIRECT			INDEX			EXTEND			IMPLIED				5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#		H	I	N	Z	V	C
Shift Left Arithmetic	ASL							68	6	2	78	6	3				M } [C] ← [b7 … b0] ← 0	●	●	↕	↕	⑥	↕
	ASLA													48	1	1	A }	●	●	↕	↕	⑥	↕
	ASLB													58	1	1	B }	●	●	↕	↕	⑥	↕
Double Shift Left, Arithmetic	ASLD													05	1	1	[C] ← [ACC A/ ACC B] ← 0 (A7 … A0 B7 … B0)	●	●	↕	↕	⑥	↕
Shift Right Arithmetic	ASR							67	6	2	77	6	3				M } [b7 … b0] → [C] (b7 retained)	●	●	↕	↕	⑥	↕
	ASRA													47	1	1	A }	●	●	↕	↕	⑥	↕
	ASRB													57	1	1	B }	●	●	↕	↕	⑥	↕
Shift Right Logical	LSR							64	6	2	74	6	3				M } 0 → [b7 … b0] → [C]	●	●	R	↕	⑥	↕
	LSRA													44	1	1	A }	●	●	R	↕	⑥	↕
	LSRB													54	1	1	B }	●	●	R	↕	⑥	↕
Double Shift Right Logical	LSRD													04	1	1	0 → [ACC A/ ACC B] → [C] (A7 … A0 B7 … B0)	●	●	R	↕	⑥	↕
Store Accumulator	STAA				97	3	2	A7	4	2	B7	4	3				A → M	●	●	↕	↕	R	●
	STAB				D7	3	2	E7	4	2	F7	4	3				B → M	●	●	↕	↕	R	●
Store Double Accumulator	STD				DD	4	2	ED	5	2	FD	5	3				A → M B → M + 1	●	●	↕	↕	R	●
Subtract	SUBA	80	2	2	90	3	2	A0	4	2	B0	4	3				A − M → A	●	●	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	4	2	F0	4	3				B − M → B	●	●	↕	↕	↕	↕
Double Subtract	SUBD	83	3	3	93	4	2	A3	5	2	B3	5	3				A : B − M : M + 1 → A : B	●	●	↕	↕	↕	↕
Subtract Accumulators	SBA													10	1	1	A − B → A	●	●	↕	↕	↕	↕
Subtract With Carry	SBCA	82	2	2	92	3	2	A2	4	2	B2	4	3				A − M − C → A	●	●	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	4	2	F2	4	3				B − M − C → B	●	●	↕	↕	↕	↕
Transfer Accumulators	TAB													16	1	1	A → B	●	●	↕	↕	R	●
	TBA													17	1	1	B → A	●	●	↕	↕	R	●
Test Zero or Minus	TST							6D	4	2	7D	4	3				M − 00	●	●	↕	↕	R	R
	TSTA													4D	1	1	A − 00	●	●	↕	↕	R	R
	TSTB													5D	1	1	B − 00	●	●	↕	↕	R	R
And Immediate	AIM				71	6	3	61	7	3							M·IMM→M	●	●	↕	↕	R	●
OR Immediate	OIM				72	6	3	62	7	3							M+IMM→M	●	●	↕	↕	R	●
EOR Immediate	EIM				75	6	3	65	7	3							M⊕IMM→M	●	●	↕	↕	R	●
Test Immediate	TIM				7B	4	3	6B	5	3							M·IMM	●	●	↕	↕	R	●

Note) Condition Code Register will be explained in Note of Table 11.

- **New Instructions**

In addition to the HD6801 Instruction Set, the HD63P01M1 has the following new instructions:

AIM----(M) · (IMM) → (M)
Evaluates the AND of the immediate data and the memory, places the result in the memory.

OIM----(M) + (IMM) → (M)
Evaluates the OR of the immediate data and the memory, places the result in the memory.

EIM----(M) ⊕ (IMM) → (M)
Evaluates the EOR of the immediate data and the contents of memory, places the result in memory.

TIM----(M) · (IMM)
Evaluates the AND of the immediate data and the memory, changes the flag of associated condition code register

Each instruction has three bytes; the first is op-code, the second is immediate data, the third is address modifier.

XGDX--(ACCD) ↔ (IX)
Exchanges the contents of accumulator and the index register.

SLP----The MPU is brought to the sleep mode. For sleep mode, see the "sleep mode" section.

Table 9 Index Register, Stack Manipulation Instructions

Pointer Operations	Mnemonic	Addressing Modes															Boolean/ Arithmetic Operation	Condition Code Register					
		IMMED.			DIRECT			INDEX			EXTEND			IMPLIED				5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#		H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	5	2	BC	5	3				X−M:M+1	•	•	↕	↕	↕	↕
Decrement Index Reg	DEX													09	1	1	X − 1 → X	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	1	1	SP − 1 → SP	•	•	•	•	•	•
Increment Index Reg	INX													08	1	1	X + 1 → X	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	1	1	SP + 1 → SP	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑦	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑦	↕	R	•
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑦	↕	R	•
Store Stack Pntr	STS				9F	4	2	AF	5	2	BF	5	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑦	↕	R	•
Index Reg → Stack Pntr	TXS													35	1	1	X − 1 → SP	•	•	•	•	•	•
Stack Pntr → Index Reg	TSX													30	1	1	SP + 1 → X	•	•	•	•	•	•
Add	ABX													3A	1	1	B + X → X	•	•	•	•	•	•
Push Data	PSHX													3C	5	1	$X_L \rightarrow M_{sp}, SP - 1 \rightarrow SP$ $X_H \rightarrow M_{sp}, SP - 1 \rightarrow SP$	•	•	•	•	•	•
Pull Data	PULX													38	4	1	$SP + 1 \rightarrow SP, M_{sp} \rightarrow X_H$ $SP + 1 \rightarrow SP, M_{sp} \rightarrow X_L$	•	•	•	•	•	•
Exchange	XGDX													18	2	1	ACCD↔IX	•	•	•	•	•	•

Note) Condition Code Register will be explained in Note of Table 11.

Table 10 Jump, Branch Instruction

Operations	Mnemonic	Addressing Modes															Branch Test	Condition Code Register					
		RELATIVE			DIRECT			INDEX			EXTEND			IMPLIED				5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#		H	I	N	Z	V	C
Branch Always	BRA	20	3	2													None	•	•	•	•	•	•
Branch Never	BRN	21	3	2													None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	3	2													C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	3	2													C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	3	2													Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	3	2													N ⊕ V = 0	•	•	•	•	•	•
Branch If > Zero	BGT	2E	3	2													Z + (N ⊕ V) = 0	•	•	•	•	•	•
Branch If Higher	BHI	22	3	2													C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	3	2													Z + (N ⊕ V) = 1	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	3	2													C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	3	2													N ⊕ V = 1	•	•	•	•	•	•
Branch If Minus	BMI	2B	3	2													N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	3	2													Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	3	2													V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	3	2													V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	3	2													N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	5	2														•	•	•	•	•	•
Jump	JMP							6E	3	2	7E	3	3					•	•	•	•	•	•
Jump To Subroutine	JSR				9D	5	2	AD	5	2	BD	6	3					•	•	•	•	•	•
No Operation	NOP													01	1	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI													3B	10	1		①					
Return From Subroutine	RTS													39	5	1		•	•	•	•	•	•
Software Interrupt	SWI													3F	12	1		•	S	•	•	•	•
Wait for Interrupt*	WAI													3E	9	1		•	①	•	•	•	•
Sleep	SLP													1A	4	1		•	•	•	•	•	•

Note) *WAI puts R/$\overline{W}$ high; Address Bus goes to FFFF; Data Bus goes to the three state.
Condition Code Register will be explained in Note of Table 11.

Table 11 Condition Code Register Manipulation Instructions

Operations	Mnemonic	Addressing Modes IMPLIED OP	~	#	Boolean Operation	Condition Code Register 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	1	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	1	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	1	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	1	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	1	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	1	1	1 → V	•	•	•	•	S	•
Accumulator A → CCR	TAP	06	1	1	A → CCR	⑩					
CCR → Accumulator A	TPA	07	1	1	CCR → A	•	•	•	•	•	•

[NOTE 1] Condition Code Register Notes: (Bit set if test is true and cleared otherwise)

- ① (Bit V) Test: Result = 10000000?
- ② (Bit C) Test: Result ≠ 00000000?
- ③ (Bit C) Test: BCD Character of high-order byte greater than 9? (Not cleared if previously set)
- ④ (Bit V) Test: Operand = 10000000 prior to execution?
- ⑤ (Bit V) Test: Operand = 01111111 prior to execution?
- ⑥ (Bit V) Test: Set equal to N⊕C=1 after the execution of instructions
- ⑦ (Bit N) Test: Result less than zero? (Bit 15=1)
- ⑧ (All Bit) Load Condition Code Register from Stack.
- ⑨ (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt is required to exit the wait state.
- ⑩ (All Bit) Set according to the contents of Accumulator A.
- ⑪ (Bit C) Result of Multiplication Bit 7=1 of ACCB?

[NOTE 2] CLI instructions and interrupt.
If interrupt mask-bit is set (I="1") and interrupt is requested ($\overline{IRQ_1}$ = "0" or $\overline{IRQ_2}$ = "0"), and then CLI instruction is executed, the CPU responds as follows.

1. the next instruction of CLI is one-machine cycle instruction. Subsequent two instructions are executed before the interrupt is responded. That is, the next and the next of the next instruction are executed.
2. the next instruction of CLI is two-machine cycle (or more) instruction. Only the next instruction is executed and then the CPU jump to the interrupt routine.

Even if TAP instruction is used, instead of CLI, the same thing occurs.

Table 12 OP-Code Map

OP CODE						ACC A	ACC B	IND	EXT / DIR*	ACCA or SP IMM	DIR	IND	EXT	ACCB or X IMM	DIR	IND	EXT	
LO \ HI		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0000	0		SBA	BRA	TSX	NEG				SUB								0
0001	1	NOP	CBA	BRN	INS			AIM		CMP								1
0010	2			BHI	PULA			OIM		SBC								2
0011	3			BLS	PULB	COM				SUBD				ADDD				3
0100	4	LSRD		BCC	DES	LSR				AND								4
0101	5	ASLD		BCS	TXS			EIM		BIT								5
0110	6	TAP	TAB	BNE	PSHA	ROR				LDA								6
0111	7	TPA	TBA	BEQ	PSHB	ASR					STA				STA			7
1000	8	INX	XGDX	BVC	PULX	ASL				EOR								8
1001	9	DEX	DAA	BVS	RTS	ROL				ADC								9
1010	A	CLV	SLP	BPL	ABX	DEC				ORA								A
1011	B	SEV	ABA	BMI	RTI			TIM		ADD								B
1100	C	CLC		BGE	PSHX	INC				CPX				LDD				C
1101	D	SEC		BLT	MUL	TST				BSR	JSR				STD			D
1110	E	CLI		BGT	WAI			JMP		LDS				LDX				E
1111	F	SEI		BLE	SWI	CLR					STS				STX			F
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

UNDEFINED OP CODE ▱

* Only for instructions of AIM, OIM, EIM, TIM

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- **Instruction Execution Cycles**

In the HMCS6800 series, the execution cycle of each instruction is the number of cycles between the start of the current instruction fetch and just before the start of the subsequent instruction fetch.

The HD63P01M1 uses a mechanism of the pipeline control for the instruction fetch and the subsequent instruction fetch is performed during the current instruction being executed.

Therefore, the method to count instruction cycles used in the HMCS6800 series cannot be applied to the instruction cycles such as MULT, PULL, DAA and XGDX in the HD63P01M1.

Table 13 provides the information about the relationship among each data on the Address Bus, Data Bus, and R/$\overline{W}$ status in cycle-by-cycle basis during the execution of each instruction.

Table 13 Cycle-by-Cycle Operation

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
IMMEDIATE					
ADC ADD		1	Op Code Address+1	1	Operand Data
AND BIT		2	Op Code Address+2	1	Next Op Code
CMP EOR	2				
LDA ORA					
SBC SUB					
ADDD CPX		1	Op Code Address+1	1	Operand Data (MSB)
LDD LDS	3	2	Op Code Address+2	1	Operand Data (LSB)
LDX SUBD		3	Op Code Address+3	1	Next Op Code
DIRECT					
ADC ADD		1	Op Code Address+1	1	Address of Operand (LSB)
AND BIT		2	Address of Operand	1	Operand Data
CMP EOR	3	3	Op Code Address+2	1	Next Op Code
LDA ORA					
SBC SUB					
STA		1	Op Code Address+1	1	Destination Address
	3	2	Destination Address	0	Accumulator Data
		3	Op Code Address+2	1	Next Op Code
ADDD CPX		1	Op Code Address+1	1	Address of Operand (LSB)
LDD LDS	4	2	Address of Operand	1	Operand Data (MSB)
LDX SUBD		3	Address of Operand+1	1	Operand Data (LSB)
		4	Op Code Address+2	1	Next Op Code
STD STS		1	Op Code Address+1	1	Destination Address (LSB)
STX	4	2	Destination Address	0	Register Data (MSB)
		3	Destination Address+1	0	Register Data (LSB)
		4	Op Code Address+2	1	Next Op Code
JSR		1	Op Code Address+1	1	Jump Address (LSB)
		2	FFFF	1	Restart Address (LSB)
	5	3	Stack Pointer	0	Return Address (LSB)
		4	Stack Pointer−1	0	Return Address (MSB)
		5	Jump Address	1	First Subroutine Op Code
TIM		1	Op Code Address+1	1	Immediate Data
	4	2	Op Code Address+2	1	Address of Operand (LSB)
		3	Address of Operand	1	Operand Data
		4	Op Code Address+3	1	Next Op Code
AIM EIM		1	Op Code Address+1	1	Immediate Data
OIM		2	Op Code Address+2	1	Address of Operand (LSB)
	6	3	Address of Operand	1	Operand Data
		4	FFFF	1	Restart Address (LSB)
		5	Address of Operand	0	New Operand Data
		6	Op Code Address+3	1	Next Op Code

– Continued –

Table 13 Cycle-by-Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
INDEXED					
JMP	3	1	Op Code Address+1	1	Offset
		2	FFFF	1	Restart Address (LSB)
		3	Jump Address	1	First Op Code of Jump Routine
ADC ADD	4	1	Op Code Address+1	1	Offset
AND BIT		2	FFFF	1	Restart Address (LSB)
CMP EOR		3	IX+Offset	1	Operand Data
LDA ORA		4	Op Code Address+2	1	Next Op Code
SBC SUB					
TST					
STA	4	1	Op Code Address+1	1	Offset
		2	FFFF	1	Restart Address (LSB)
		3	IX+Offset	0	Accumulator Data
		4	Op Code Address+2	1	Next Op Code
ADDD	5	1	Op Code Address+1	1	Offset
CPX LDD		2	FFFF	1	Restart Address (LSB)
LDS LDX		3	IX+Offset	1	Operand Data (MSB)
SUBD		4	IX+Offset+1	1	Operand Data (LSB)
		5	Op Code Address+2	1	Next Op Code
STD STS	5	1	Op Code Address+1	1	Offset
STX		2	FFFF	1	Restart Address (LSB)
		3	IX+Offset	0	Register Data (MSB)
		4	IX+Offset+1	0	Register Data (LSB)
		5	Op Code Address+2	1	Next Op Code
JSR	5	1	Op Code Address+1	1	Offset
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer	0	Return Address (LSB)
		4	Stack Pointer−1	0	Return Address (MSB)
		5	IX+Offset	1	First Subroutine Op Code
ASL ASR	6	1	Op Code Address+1	1	Offset
COM DEC		2	FFFF	1	Restart Address (LSB)
INC LSR		3	IX+Offset	1	Operand Data
NEG ROL		4	FFFF	1	Restart Address (LSB)
ROR		5	IX+Offset	0	New Operand Data
		6	Op Code Address+2	1	Next Op Code
TIM	5	1	Op Code Address+1	1	Immediate Data
		2	Op Code Address+2	1	Offset
		3	FFFF	1	Restart Address (LSB)
		4	IX+Offset	1	Operand Data
		5	Op Code Address+3	1	Next Op Code
CLR	5	1	Op Code Address+1	1	Offset
		2	FFFF	1	Restart Address (LSB)
		3	IX+Offset	1	Operand Data
		4	IX+Offset	0	00
		5	Op Code Address+2	1	Next Op Code
AIM EIM	7	1	Op Code Address+1	1	Immediate Data
OIM		2	Op Code Address+2	1	Offset
		3	FFFF	1	Restart Address (LSB)
		4	IX+Offset	1	Operand Data
		5	FFFF	1	Restart Address (LSB)
		6	IX+Offset	0	New Operand Data
		7	Op Code Address+3	1	Next Op Code

– Continued –

Table 13 Cycle-by-Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
EXTEND					
JMP	3	1	Op Code Address+1	1	Jump Address (MSB)
		2	Op Code Address+2	1	Jump Address (LSB)
		3	Jump Address	1	Next Op Code
ADC ADD TST AND BIT CMP EOR LDA ORA SBC SUB	4	1	Op Code Address+1	1	Address of Operand (MSB)
		2	Op Code Address+2	1	Address of Operand (LSB)
		3	Address of Operand	1	Operand Data
		4	Op Code Address+3	1	Next Op Code
STA	4	1	Op Code Address+1	1	Destination Address (MSB)
		2	Op Code Address+2	1	Destination Address (LSB)
		3	Destination Address	0	Accumulator Data
		4	Op Code Address+3	1	Next Op Code
ADDD CPX LDD LDS LDX SUBD	5	1	Op Code Address+1	1	Address of Operand (MSB)
		2	Op Code Address+2	1	Address of Operand (LSB)
		3	Address of Operand	1	Operand Data (MSB)
		4	Address of Operand+1	1	Operand Data (LSB)
		5	Op Code Address+3	1	Next Op Code
STD STS STX	5	1	Op Code Address+1	1	Destination Address (MSB)
		2	Op Code Address+2	1	Destination Address (LSB)
		3	Destination Address	0	Register Data (MSB)
		4	Destination Address+1	0	Register Data (LSB)
		5	Op Code Address+3	1	Next Op Code
JSR	6	1	Op Code Address+1	1	Jump Address (MSB)
		2	Op Code Address+2	1	Jump Address (LSB)
		3	FFFF	1	Restart Address (LSB)
		4	Stack Pointer	0	Return Address (LSB)
		5	Stack Pointer−1	0	Return Address (MSB)
		6	Jump Address	1	First Subroutine Op Code
ASL ASR COM DEC INC LSR NEG ROL ROR	6	1	Op Code Address+1	1	Address of Operand (MSB)
		2	Op Code Address+2	1	Address of Operand (LSB)
		3	Address of Operand	1	Operand Data
		4	FFFF	1	Restart Address (LSB)
		5	Address of Operand	0	New Operand Data
		6	Op Code Address+3	1	Next Op Code
CLR	5	1	Op Code Address+1	1	Address of Operand (MSB)
		2	Op Code Address+2	1	Address of Operand (LSB)
		3	Address of Operand	1	Operand Data
		4	Address of Operand	0	00
		5	Op Code Address+3	1	Next Op Code

— Continued —

Table 13 Cycle-by-Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
IMPLIED					
ABA ABX ASL ASLD ASR CBA CLC CLI CLR CLV COM DEC DES DEX INC INS INX LSR LSRD ROL ROR NOP SBA SEC SEI SEV TAB TAP TBA TPA TST TSX TXS	1	1	Op Code Address+1	1	Next Op Code
DAA XGDX	2	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
PULA PULB	3	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer+1	1	Data from Stack
PSHA PSHB	4	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer	0	Accumulator Data
		4	Op Code Address+1	1	Next Op Code
PULX	4	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer+1	1	Data from Stack (MSB)
		4	Stack Pointer+2	1	Data from Stack (LSB)
PSHX	5	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer	0	Index Register (LSB)
		4	Stack Pointer−1	0	Index Register (MSB)
		5	Op Code Address+1	1	Next Op Code
RTS	5	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer+1	1	Return Address (MSB)
		4	Stack Pointer+2	1	Return Address (LSB)
		5	Return Address	1	First Op Code of Return Routine
MUL	7	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	FFFF	1	Restart Address (LSB)
		4	FFFF	1	Restart Address (LSB)
		5	FFFF	1	Restart Address (LSB)
		6	FFFF	1	Restart Address (LSB)
		7	FFFF	1	Restart Address (LSB)

— Continued —

Table 13 Cycle-by-Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
IMPLIED					
WAI	9	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer	0	Return Address (LSB)
		4	Stack Pointer−1	0	Return Address (MSB)
		5	Stack Pointer−2	0	Index Register (LSB)
		6	Stack Pointer−3	0	Index Register (MSB)
		7	Stack Pointer−4	0	Accumulator A
		8	Stack Pointer−5	0	Accumulator B
		9	Stack Pointer−6	0	Conditional Code Register
RTI	10	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer+1	1	Conditional Code Register
		4	Stack Pointer+2	1	Accumulator B
		5	Stack Pointer+3	1	Accumulator A
		6	Stack Pointer+4	1	Index Register (MSB)
		7	Stack Pointer+5	1	Index Register (LSB)
		8	Stack Pointer+6	1	Return Address (MSB)
		9	Stack Pointer+7	1	Return Address (LSB)
		10	Return Address	1	First Op Code of Return Routine
SWI	12	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		3	Stack Pointer	0	Return Address (LSB)
		4	Stack Pointer − 1	0	Return Address (MSB)
		5	Stack Pointer − 2	0	Index Register (LSB)
		6	Stack Pointer − 3	0	Index Register (MSB)
		7	Stack Pointer − 4	0	Accumulator A
		8	Stack Pointer − 5	0	Accumulator B
		9	Stack Pointer − 6	0	Conditional Code Register
		10	Vector Address FFFA	1	Address of SWI Routine (MSB)
		11	Vector Address FFFB	1	Address of SWI Routine (LSB)
		12	Address of SWI Routine	1	First Op Code of SWI Routine
SLP	4	1	Op Code Address+1	1	Next Op Code
		2	FFFF	1	Restart Address (LSB)
		↑ Sleep ↓	FFFF		High Impedance-Non MPX Mode Address Bus -MPX Mode ↓
		3	FFFF		Restart Address (LSB)
		4	Op Code Address+1		Next Op Code

— Continued —

Table 13 Cycle-by-Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$	Data Bus
RELATIVE					
BCC BCS		1	Op Code Address+1	1	Branch Offset
BEQ BGE	3	2	FFFF	1	Restart Address (LSB)
BGT BHI		3	{ Branch Address······Test="1"	1	First Op Code of Branch Routine
BLE BLS			Op Code Address+1···Test="0"		Next Op Code
BLT BMT					
BNE BPL					
BRA BRN					
BVC BVS					
BSR		1	Op Code Address+1	1	Offset
		2	FFFF	1	Restart Address (LSB)
	5	3	Stack Pointer	0	Return Address (LSB)
		4	Stack Pointer−1	0	Return Address (MSB)
		5	Branch Address	1	First Op Code of Subroutine

■ LOW POWER CONSUMPTION MODE

The HD63P01M1 has two low power consumption modes; sleep and standby mode.

● Sleep Mode

On execution of SLP instruction, the MCU is brought to the sleep mode. In the sleep mode, the CPU sleeps (the CPU clock becomes inactive), but the contents of the registers in the CPU are retained. In this mode, the peripherals of CPU will remain active. So the operations such as transmit and receive of the SCI data and counter may keep in operation. In this mode, the power consumption is reduced to about 1/6 the value of a normal operation.

The escape from this mode can be done by interrupt, $\overline{RES}$, $\overline{STBY}$. The $\overline{RES}$ resets the MCU and the $\overline{STBY}$ brings it into the standby mode (This will be mentioned later). When interrupt is requested to the CPU and accepted, the sleep mode is released, then the CPU is brought in the operation mode and jumps to the interrupt routine. When the CPU has masked the interrupt after recovering from the sleep mode, the next instruction of SLP starts to execute. However, in such a case that the timer interrupt is inhibited on the timer side, the sleep mode cannot be released due to the absence of the interrupt request to the CPU.

This sleep mode is available to reduce an average power consumption in the applications of the HD63P01M1 which may not be always running.

● Standby Mode

Bringing $\overline{STBY}$ "Low", the CPU becomes reset and all clocks of the HD63P01M1 become inactive. It goes into the standby mode. This mode remarkably reduces the power consumptions of the HD63P01M1.

In the standby mode, if the HD63P01M1 is continuously supplied with power, the contents of RAM is retained. The standby mode should escape by the reset start. The following is the typical application of this mode.

First, $\overline{NMI}$ routine stacks the MCU's internal information and the contents of SP in RAM, disables RAME bit of RAM control register, sets the Standby bit, and then goes into the standby mode. If the Standby bit keeps set on reset start, it means that the power has been kept during standby mode and the contents of RAM is normally guaranteed. The system recovery may be possible by returning SP and bringing into the condition before the standby mode has started. The timing relation for each line in this application is shown in Figure 24.

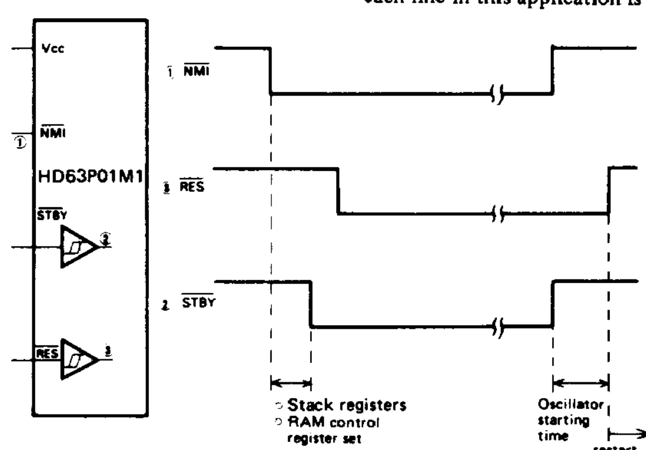


Figure 24 Standby Mode Timing

■ ERROR PROCESSING

When the HD63P01M1 fetches an undefined instruction or fetches an instruction from unusable memory area, it generates the highest priority internal interrupt, that may protect from system upset due to noise or a program error.

● Op-Code Error

Fetching an undefined op-code, the HD63P01M1 will stack the CPU register as in the case of a normal interrupt and vector to the TRAP ($FFEE, $FFEF), that has a second highest priority ($\overline{RES}$ is the highest).

● Address Error

When an instruction is fetched from other than a resident ROM, RAM, or an external memory area, the CPU starts the same interrupt as op-code error. In the case which the instruction is fetched from external memory area and that area is not usable, the address error cannot be detected.

The addresses which cause address error in particular mode are shown in Table 14.

This feature is applicable only to the instruction fetch, not to normal read/write of data accessing.

Table 14 Address Error

Mode	0	1	2, 4	5	6	7
Address	$0000 ~ $001F	$0000 ~ $001F	$0000 ~ $001F	$0000 ~ $007F $0200 ~ $DFFF	$0000 ~ $001F	$0000 ~ $007F $0100 ~ $DFFF

System Flow chart of HD63P01M1 is shown in Fig. 25.

Transitions among the active mode, sleep mode, standby mode and reset are shown in Fig. 26.

Figures 27, 28, 29 and 30 shows a system configuration.

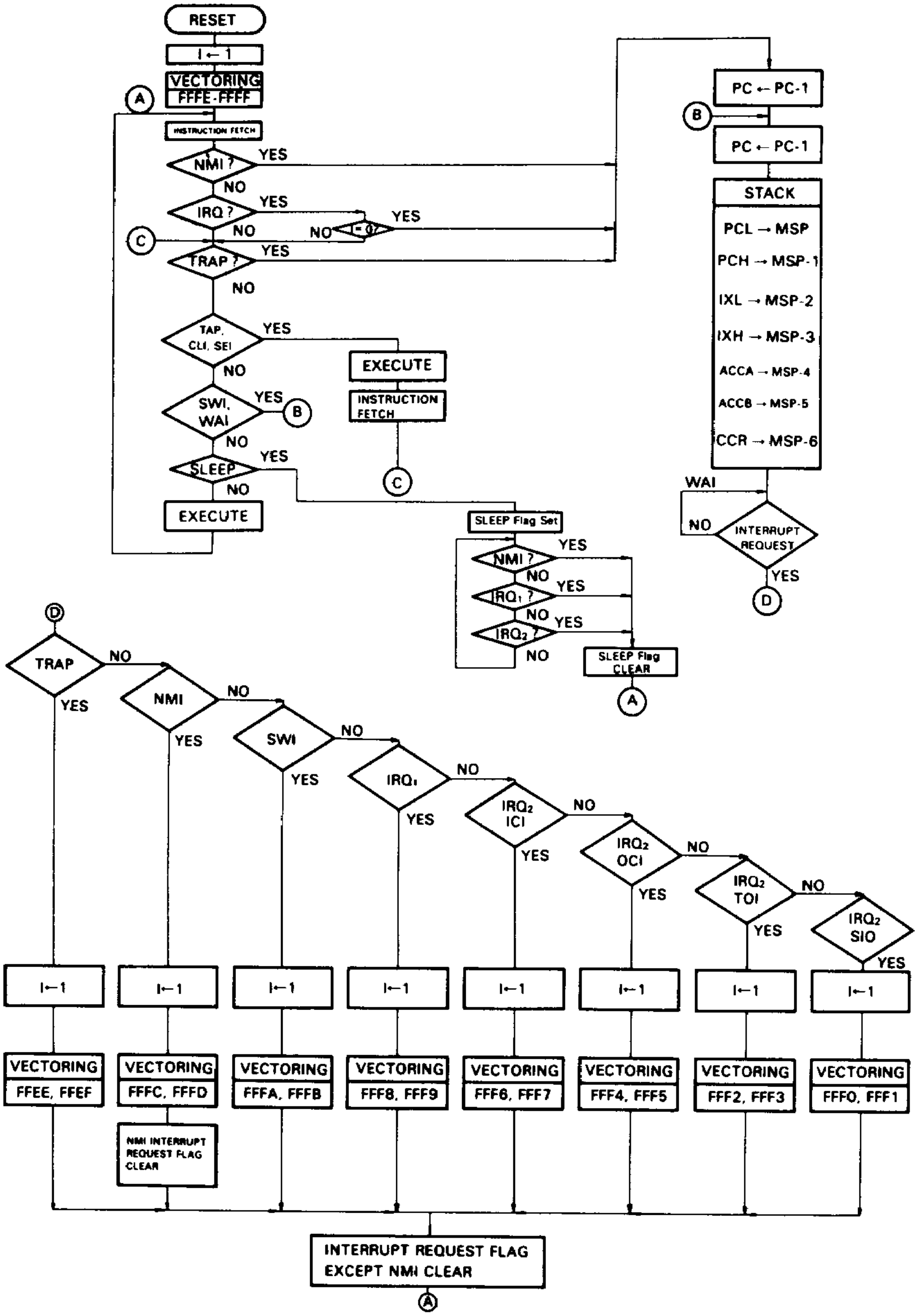


Figure 25 HD63P01M1 System Flow Chart

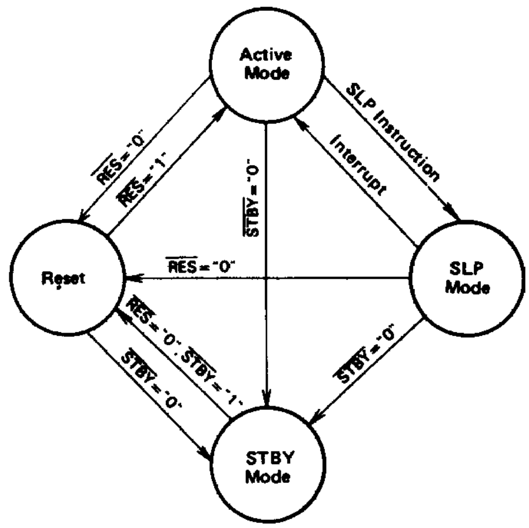


Figure 26 Transitions among Active Mode, Standby Mode, Sleep Mode, and Reset

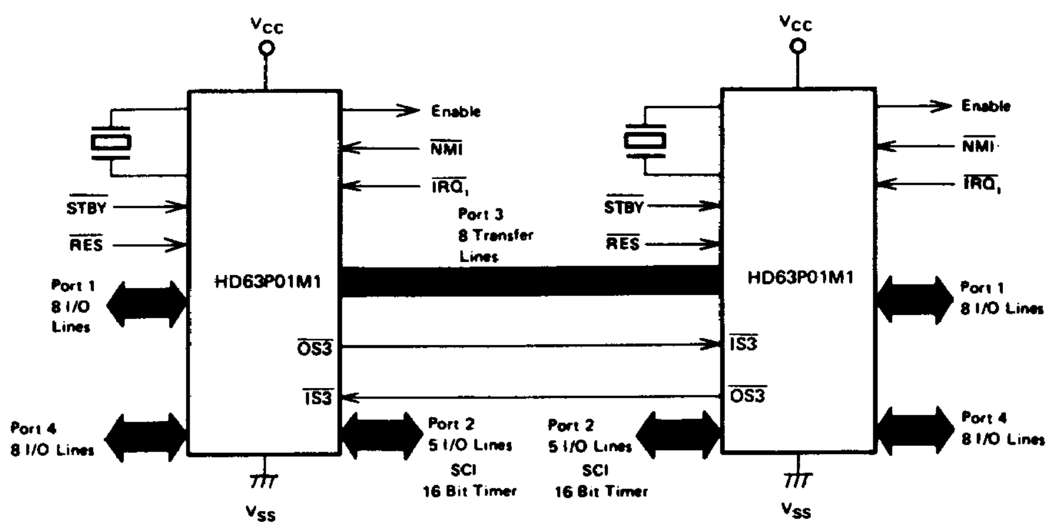


Figure 27 HD63P01M1 MCU Single-Chip Dual Processor Configuration

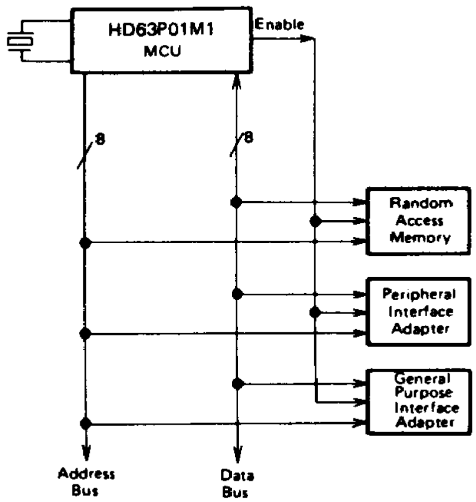


Figure 28 HD63P01M1 MCU Expanded Non-Multiplexed Mode (Mode 5)

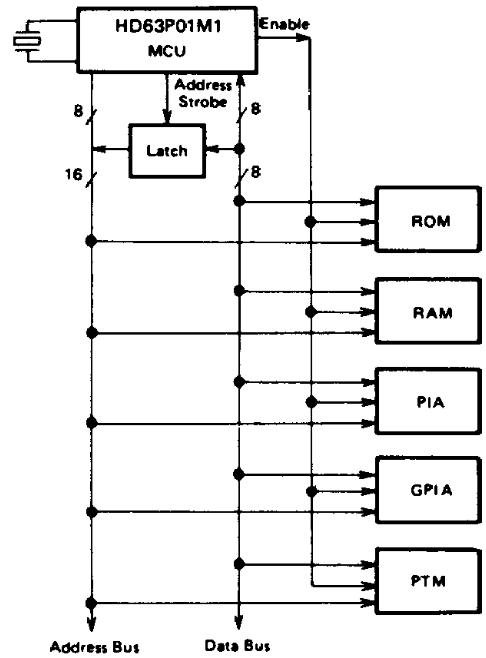


Figure 29 HD63P01M1 MCU Expanded Multiplexed Mode (Modes 2, 4 and 6)

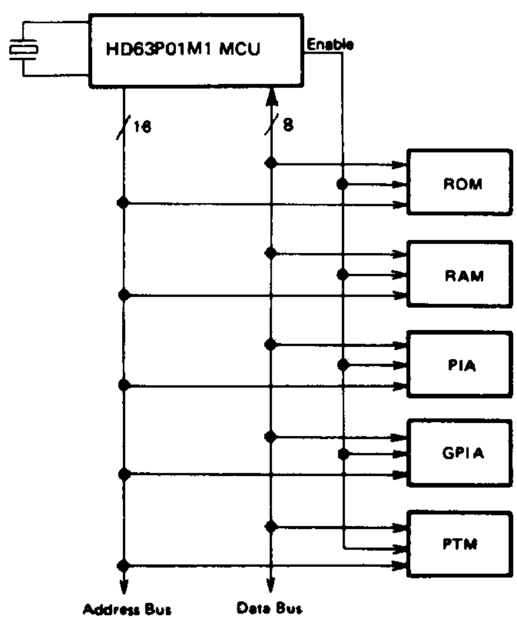
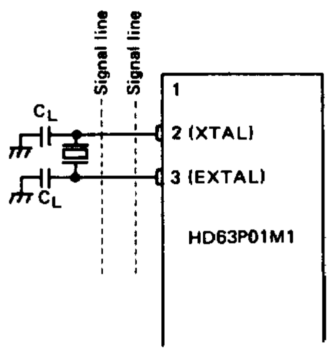


Figure 30 HD63P01M1 MCU Expanded Non-Multiplexed Mode (Mode 1)

■ PRECAUTION TO THE BOARD DESIGN OF OSCILLATION CIRCUIT

As shown in Fig. 31, there is a case that the cross talk disturbs the normal oscillation if signal lines are put near the oscillation circuit. When designing a board, pay attention to this . Crystal and C_L must be put as near the HD63P01M1 as possible.



Do not use this kind of print board design.

Figure 31 Precaution to the boad design of oscillation circuit

■ PIN CONDITIONS AT SLEEP AND STANDBY STATE

● Sleep State

The conditions of power supply pins (pins 1 and 21), clock pins (pins 2 and 3), input pins (pins 4, 5, 6 and 7) and E clock pin (pin 40) are the same as those of operation. Refer to Table 15 for the other pin conditions. Both address (A_0 ~ A_{12}) and chip enable ($\overline{CE}$) for the EPROM are in "1" state.

● Standby State

Only power supply pins (pins 1 and 21) and $\overline{STBY}$ pin (pin 7) are active. As for the clock pin EXTAL(pin3), its input is fixed internally so the MCU is not influenced by the pin conditions. XTAL (pin 2) is in "1" output. All the other pins are in high impedance. Both address (A_0 ~ A_{12}) and chip enable ($\overline{CE}$) for the EPROM are in "1" output.

Table 15 Pin Condition in Sleep Mode

Pin \ Mode		0	1	2, 4	5	6	7
Port 1 P_{10}~P_{17}	Function	I/O Port	Lower Address Bus	I/O Port	←	←	←
	Condition	Keep the condition just before sleep	Output "1"	Keep the condition just before sleep	←	←	←
Port 2 P_{20}~P_{24}	Function	I/O Port	←	←	←	←	←
	Condition	Keep the condition just before sleep	←	←	←	←	←
Port 3 P_{30}~P_{37}	Function	$\bar{E}$: Lower Address Bus E: Data Bus	Data Bus	$\bar{E}$: Lower Address Bus E: Data Bus	Data Bus	$\bar{E}$: Lower Address Bus E: Data Bus	I/O Port
	Condition	$\bar{E}$: Output "1" E: High Impedance	High Impedance	$\bar{E}$: Output "1" E: High Impedance	High Impedance	$\bar{E}$: Output "1" E: High Impedance	Keep the condition just before sleep
Port 4 P_{40}~P_{47}	Function	Upper Address	←	←	Lower Address Bus or Input Port	Upper Address Bus or Input Port	I/O Port
	Condition	Output "1"	←	←	Address Bus: Output "1" Port: Keep the condition just before sleep	←	Keep the condition just before sleep
SC_2		Output "1" (Read Condition)	←	←	←	←	Output "1"
SC_1		Output Address Strobe	←	←	Output "1"	Output Address Strobe	Input Pin

Table 16 Pin Condition during Reset

Pin \ Mode	0	1	2, 4	5	6	7
Port 1 $P_{10} \sim P_{17}$	high impedance (input)	←	←	←	←	←
Port 2 $P_{20} \sim P_{24}$	high impedance (input)	←	←	←	←	←
Port 3 $P_{30} \sim P_{37}$	$\overline{E}$: "1" output E: "1" output (Note) (high impedance)	high impedance	$\overline{E}$: "1" output E: "1" output (Note) (high impedance)	high impedance	$\overline{E}$: "1" output E: "1" output (Note) (high impedance)	high impedance (input)
Port 4 $P_{40} \sim P_{47}$	high impedance (input)	←	←	←	←	←
SC_2	"1" output (READ)	←	←	←	←	"1" output
SC_1	$\overline{E}$: "1" output E: high impedance	←	←	"1" output	$\overline{E}$: "1" output E: high impedance	high impedance (input)
$A_0 \sim A_{12}$, $\overline{CE}$	"1" output	←	←	←	←	←

[Note] In mode 0, 2, 4, 6, port 3 is set to "1" output state during E = "1" and it causes the conflict with the output of external memory. Following 1 and 2 should be done to avoid the conflict;
(1) Construct the system that disables the external memory during reset.
(2) Add 4.7kΩ pull-down resistance to the SC_1 pin (AS) to make SC_1 pin "0" level during E = "1".
This operation makes port 3 high impedance state.

■ PRECAUTION TO EMULATE THE HD6301V1 BY HD63P01M1

The internal EPROM of the HD63P01M1 provides 8k bytes address space located from $E000 through $FFFF. The followings should be noted to emulate the HD6301V1 (4k bytes internal ROM) with the HD63P01M1.

1. Mode 5 (Expanded Non-multiplexed Mode) and Mode 7 (Single Chip Mode)
   Use 4k bytes of EPROM address space located from $F000 through $FFFF.
2. Mode 6 (Expanded Multiplexed Mode)
   Use 4k bytes of EPROM address space located from $F000 through $FFFF. But do not use 4k bytes from $E000 through $EFFF because these addresses are internal for the HD63P01M1, while these are external for the HD6301V1.
3. Mode 1, 2, 4
   No need to be careful, since ROM address is external in these cases.

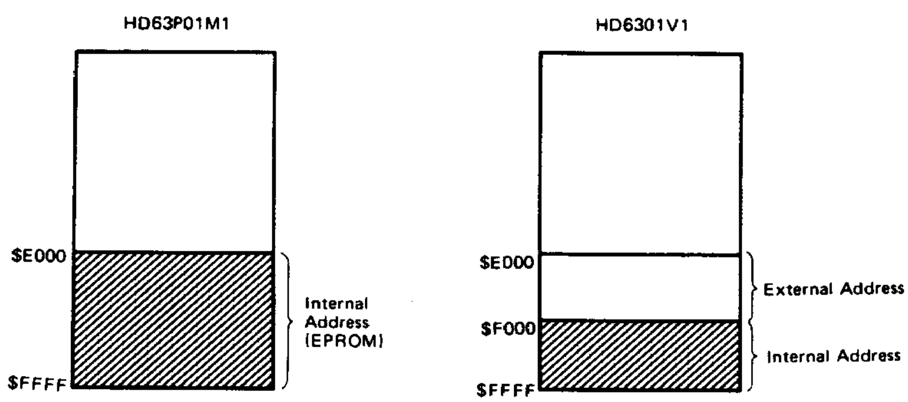


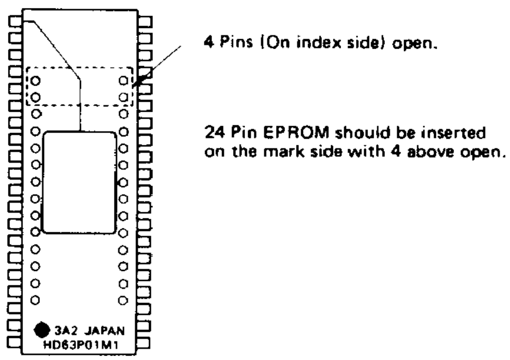
Figure 32 Address Map of Mode 6

■ PRECAUTION TO USE THE EPROM ON-PACKAGE 8 BIT SINGLE CHIP MICROCOMPUTER

Please pay attention to the followings, since this MCU has special structure with pin socket on the package.

(1) Don't apply high static voltage or surge voltage over MAXIMUM RATINGS to the socket pins as well as the LSI pins. If not, that may cause permanent damage to the device.

(2) When using 32k EPROM (24 pin), insert it on the mark side and let the four above pins open.



(3) When using this in production like mask ROM type single chip microcomputer, pay attention to the followings to keep the good contact between the EPROM pins and socket pins.

(a) When soldering the LSI on a print circuit board, the recommended condition is

Temperature : lower than 250°C
Time : within 10 sec.

(b) Note that the detergent or coating will not get in the socket during flux washing or board coating after soldering, because that may cause bad effect on socket contact.

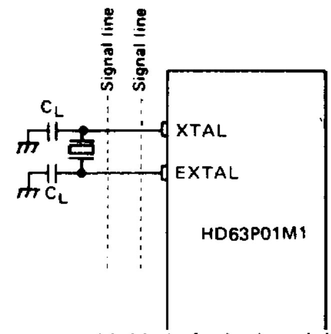
(c) Avoid permanent application of this under the condition of vibratory place and system.

(d) The socket, inserted and pulled repeatedly loses its contactability. It is recommended to use new one when applied in production.

Ask our sales agent about anything unclear.

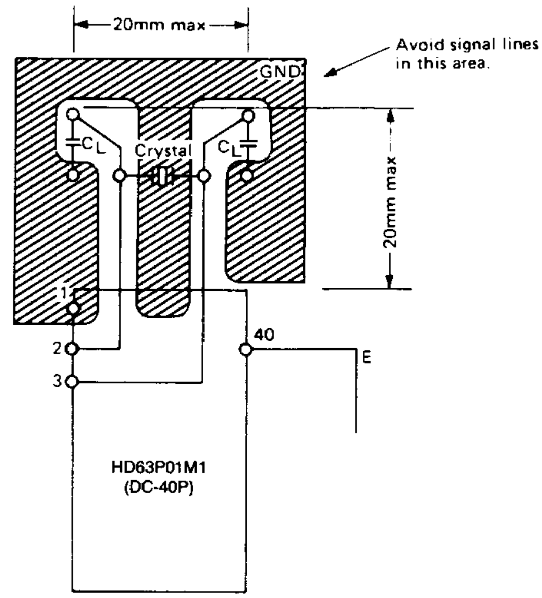
■ PRECAUTION TO THE BOARD DESIGN OF OSCILLATION CIRCUIT

As shown in Fig. 33, there is a case that the cross talk disturbs the normal oscillation if signal lines are put near the oscillation circuit. When designing a board, pay attention to this. Crystal and C_L must be put as near the HD63P01M1 as possible.



Do not use this kind of print board design.

Figure 33 Precaution to the boad design of oscillation circuit



(Top view)

Figure 34 Example of Oscillation Circuits in Board Design

■ WARNING CONCERNING POWER START-UP

$\overline{RES}$ must be held low for at least 20 ms when the power starts up. In this case, the internal reset function is not effective until the oscillation begins at power-on. The $\overline{RES}$ signal is input to the LSI in synchronism with the internal clock ϕ (shown in Figure 35).

Therefore, after power starts up, the LSI conditions such as its I/O ports and operating mode, are unstable. Fix the level of I/O ports by means of an external circuit to determine the level for system operation during the oscillator stabilization time.

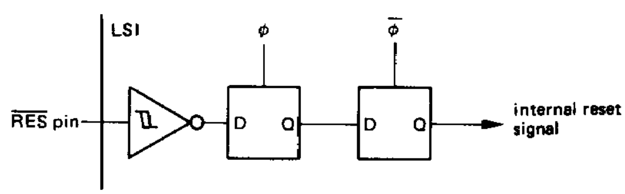


Figure 35 $\overline{RES}$ circuit

■ **WARNING CONCERNING WAI INSTRUCTION**

If the HALT signal is accepted by the MCU while the WAI instruction is executing, the CPU will not operate correctly after HALT mode is canceled.

WAI is a instruction which waits for an interrupt. The corresponding interrupt routine is executed after an interrupt occurs.

However, during the execution of the WAI instruction, $\overline{HALT}$ input makes the CPU malfunction and fetch an abnormal interrupt vectoring address.

In HALT mode, the CPU operates correctly without the WAI instruction, and WAI is executed correctly without $\overline{HALT}$ input. Therefore, if $\overline{HALT}$ input is necessary, make interrupts wait during the loop routine, as shown in Figure 36.

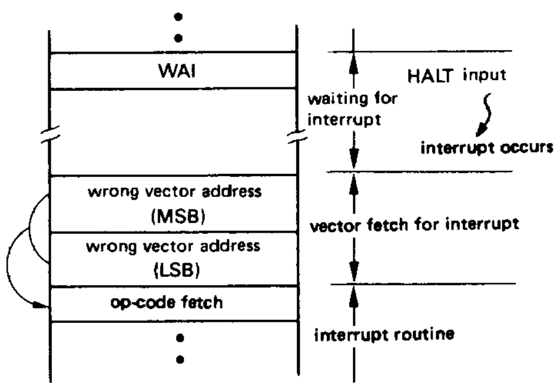
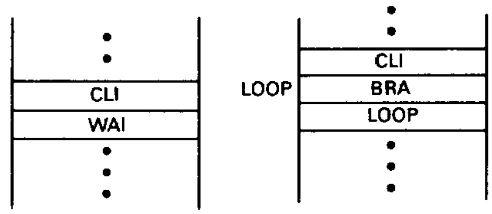


Figure 36 MAC function during WAI



i) MAL function ii) Recommended method

Figure 37 Program to wait for interrupt

■ **WRITE-ONLY REGISTER**

When the CPU reads a write-only register, the read data is always $FF, regardless of the value in the write-only register. Therefore, be careful of the results of instructions which read a write-only register and perform an arithmetic or logical operation on its contents, such as AIM, ADD, or ROL, is executed, because the arithmetic or logical operation is always done with the data $FF. In particular, don't use the AIM, OIM or EIM instruction to manipulate the DDR bit of PORT.

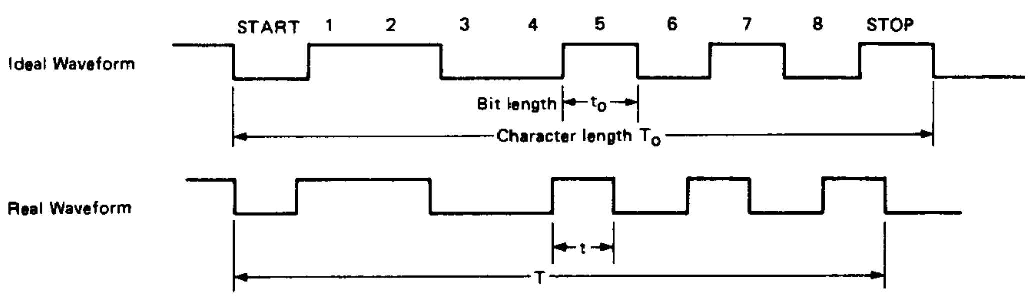
■ **RECEIVE MARGIN OF THE SCI**

Receive margin of the SCI contained in the HD63P01M1 is shown in Table 17.

Note: SCI = Serial Communication Interface

Table 17

Bit distortion tolerance (t−to) /to	Character distortion tolerance (T−To) /To
±25%	±3.75%



■ DIFFERENCES BETWEEN HD6301V1, HD6303R, HD6303R1, HD63P01M1, AND HD63701V0

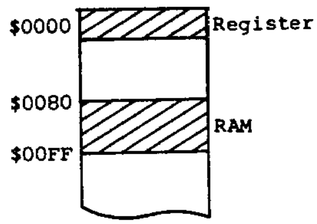
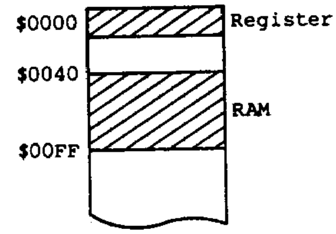
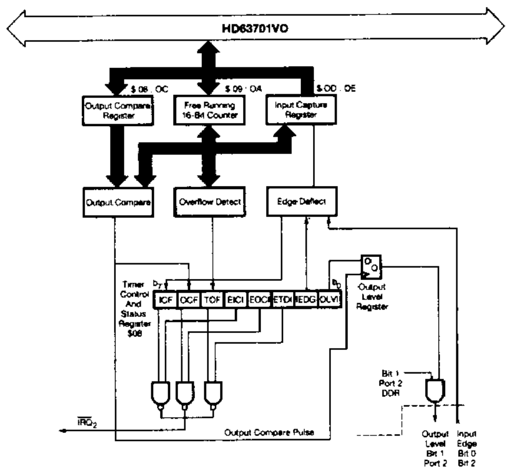
<table>
<tr><th colspan="2">Item</th><th colspan="2">HD6301V</th><th>HD63701V0</th></tr>
<tr><td rowspan="4">Function</td><td>RAM</td><td colspan="2">RAM Size: 128-byte
Address: $0080–$00FF

</td><td>RAM Size: 192-byte
Address: $0040–$00FF

</td></tr>
<tr><td>Operation Mode</td><td colspan="2">Mode 4: Expanded Multiplexed Mode = Mode 2</td><td>HD63701V0 does not have Mode 4</td></tr>
<tr><td>Timer</td><td colspan="2">After providing supply voltage, output level is undefined (0 or 1) unless the contents of the Output Compare Register matches with those of the Free Running Counter. The Output Level Register is not initialized by reset.


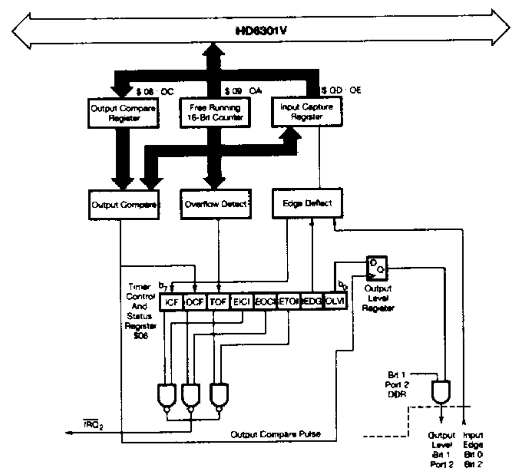
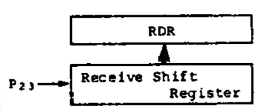
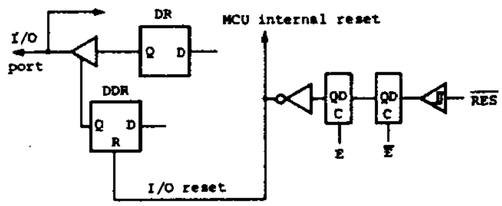
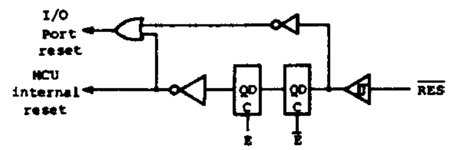
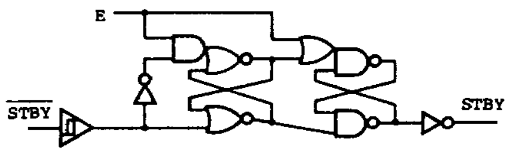
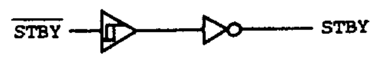
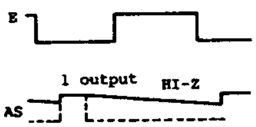
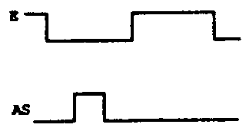
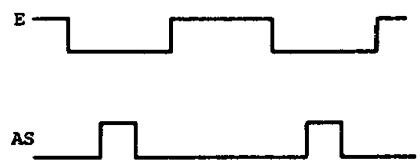
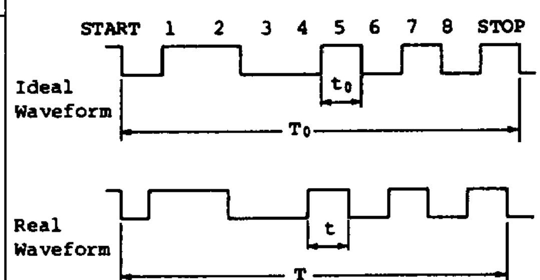
Figure 20 Programmable Timer Block Diagram</td><td>The Output Level Register is initialized to 0 by reset.


Figure 20 Programmable Timer Block Diagram</td></tr>
<tr><td>SCI</td><td>HD6301V1, HD6303R, HD63P01M1

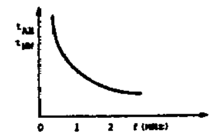
When framing error occurs, receive data is not transferred from the Receive Shift Register to Receive Data Register (RDR).

</td><td>HD6303R1

Receive data is transferred from Receive Shift Register to RDR even if framing error occurs.</td><td>Receive data is transferred from Receive Shift Register to RDR even if framing error occurs.</td></tr>
</table>

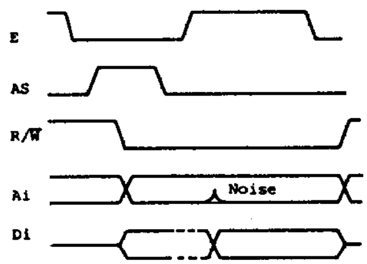
■ DIFFERENCES BETWEEN HD6301V1, HD6303R, HD6303R1, HD63P01M1, AND HD63701V0 (Continued)

	Item	HD6301V		HD63701V0
Function	Port Reset	The DDR of port is reset synchronously with E clock. I/O state is undefined from providing power supply till oscillation start (max. 20ms). 		The DDR of port is reset asynchronously with E clock. CPU enters into high impedance state (input state) by bringing RES Low. Reset release and MCU internal reset is performed synchronously with E clock. 
Function	Standby Mode	STBY signal is latched synchronously with E clock. 		STBY signal is latched asynchronously with E clock. CPU enters into standby state by bringing STBY low. 
Function	AS (Address Strobe)	HD63P01M1	HD6301V1, HD6303R, HD6303R1	
		 In Expanded Multiplexed Mode (mode 0, 2, 4 or 6), AS becomes high impedance state for a half E clock cycle during reset. Therefore, I/O Port 3 functions as data bus during reset.	 During reset, AS functions normally.	 During reset, AS functions normally.
Function	SCI Receive Margin	HD6301V1, HD6303R, HD6303R1	HD63P01M1	The SCI receive margin is shown below.
		The SCI receive margin is shown below. Bit distortion tolerance $(t-t_0)/t_0$: ±37.5% Character distortion tolerance $(T-T_0)/T_0$: +3.5% / −2.5%	The SCI receive margin is shown below. Bit distortion tolerance $(t-t_0)/t_0$: ±25% Character distortion tolerance $(T-T_0)/T_0$: ±3.75%	 Bit distortion tolerance $(t-t_0)/t_0$: ±37.5% Character distortion tolerance $(T-T_0)/T_0$: ±3.75%

■ **DIFFERENCES BETWEEN HD6301V1, HD6303R, HD6303R1, HD63P01M1, AND HD63701V0 (Continued)**

<table>
<tr><th colspan="2">Item</th><th colspan="2">HD6301V</th><th rowspan="2">HD63701V0</th></tr>
<tr><td rowspan="2">Function</td><td></td><td>HD6301V1, HD6303R, HD6303R1</td><td>HD63P01M1</td></tr>
<tr><td>Supply Voltage</td><td>V_{CC} = 5V ± 10%
(f = 0.1 ~ 2 MHz)
V_{CC} = 3 ~ 6V
(f = 0.1 ~ 0.5 MHz)</td><td>V_{CC} = 5V ± 10%
(f = 0.1 ~ 1 MHz)</td><td>V_{CC} = 5V ± 10% (f = 0.1 ~ 2 MHz)</td></tr>
<tr><td>Function</td><td>Address/Data Hold Time (t_{AH}, t_{HW})</td><td colspan="2">t_{AH} = 20 ns min.
t_{HW} = 20 ns min.
t_{AH} and t_{HW} are constant independently of operating frequency.</td><td>t_{AH}, t_{HW} = 60 ns (f = 1 MHz)
= 40 ns (f = 1.5 MHz)
= 30 ns (f = 2 MHz)
t_{AH} and t_{HW} are proportion to 1/f. (f = operating frequency)
</td></tr>
<tr><td rowspan="6">Specification</td><td>Address Delay Time</td><td colspan="2">(1) t_{AD1} and t_{AD2} are constant independently of operating frequency. In HD63B01V (B version of HD6301V), t_{AD1} and t_{AD2} are 160 ns max. at 0.1 MHz through 2 MHz operation.
(2) t_{ADL} is related to operating frequency. (t_{ADL} is in proportion to 1/f. f = operating frequency)</td><td>t_{AD1}, t_{AD2} and t_{ADL} are related to operating frequency (They are in proportion to 1/f. f = operating frequency). Therefore, if HD637B01V operates at lower operating frequency, t_{AD1}, t_{AD2} and t_{ADL} will become 160 ns or more. t_{AD1}, t_{AD2} and t_{ADL} are calculated as follows.
t_{AD} (f MHz) ≒ 250 ns (1 MHz) × 1/f (MHz)</td></tr>
<tr><td>I_{in} and C_{in} of $\overline{RES}$</td><td colspan="2">I_{in} = 1.0 μA max., C_{in} = 12.5 pF max.</td><td>I_{in} = 10 μA max. C_{in} = 50 pF max. Since $\overline{RES}$ is multiplexed with V_{PP}, C_{in} and I_{in} are larger than those of HD6301V.</td></tr>
<tr><td>Load Capacitance of E</td><td colspan="2">2 - LSTTL + 40pF
I_{OL} = 0.8 mA, I_{OH} = −200 μA</td><td>1 - TTL + 90pF
I_{OL} = 1.6 mA, I_{OH} = −200 μA</td></tr>
<tr><td>Load Capacitance of Port 1</td><td colspan="2">1 - TTL + 30pF</td><td>1 - TTL + 90pF</td></tr>
<tr><td>Spec. of Crystal Oscillator</td><td colspan="2">Spec.
R_s = 60Ω max.</td><td>Spec.<table><tr><td>Clock frequency (MHz)</td><td>2.5</td><td>4.0</td><td>6.0</td><td>8.0</td></tr><tr><td>Rs max. (Ω)</td><td>500</td><td>120</td><td>80</td><td>60</td></tr></table></td></tr>
<tr><td>Storage Temperature</td><td colspan="2">T_{stg} = −55 − +150°C</td><td>T_{stg} = −55 − +125°C</td></tr>
</table>

■ DIFFERENCES BETWEEN HD6301V1, HD6303R, HD6303R1, HD63P01M1, AND HD63701V0 (Continued)

<table>
<tr><th></th><th>Item</th><th colspan="2">HD6301V</th><th>HD63701V0</th></tr>
<tr><td rowspan="3">Function</td><td rowspan="2">GND Noise</td><td>HD6301V1, HD6303R</td><td>HD6303R1, HD63P01M1</td><td rowspan="2">Noise is reduced by 50%.</td></tr>
<tr><td>
If load capacitance in each data line and GND impedance are large, noise may appear on address bus during MCU write cycle and data won't be written into RAM correctly. The noise is caused by GND impedance which becomes large when large transient current flows into GND at High to Low transition of data line.</td><td>Noise is reduced by 33%.</td></tr>
<tr><td>Miscellaneous</td><td colspan="3">Chip design and manufacturing process of the HD6301V differ from those of the HD63701V0. Therefore, actual spec. and margin are different between the HD6301V and the HD63701V0. Please carefully examine your system before applying HD6301V or HD63701V0 to your system.</td></tr>
</table>

RELIABILITY AND QUALITY ASSURANCE

1. VIEWS ON QUALITY AND RELIABILITY

Basic views on quality in Hitachi are to meet individual user's purchase purpose and quality required, and to be at the satisfied quality level considering general marketability. Quality required by users is specifically clear if the contract specification is provided. If not, quality required is not always definite. In both cases, efforts are made to assure the reliability so that semiconductor devices delivered can perform their ability in actual operating circumstances. To realize such quality in manufacturing process, the key points should be to establish quality control system in the process and to enhance morale for quality.

In addition, quality required by users on semiconductor devices is going toward higher level as performance of electronic system in the market is going toward higher one and is expanding size and application fields. To cover the situation, actual bases Hitachi is performing is as follows;

(1) Build the reliability in design at the stage of new product development.
(2) Build the quality at the sources of manufacturing process.
(3) Execute the harder inspection and reliability confirmation of final products.
(4) Make quality level higher with field data feed back.
(5) Cooperate with research laboratories for higher quality and reliability.

With the views and methods mentioned above, utmost efforts are made for users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Targets

Reliability target is the important factor in manufacture and sales as well as performance and price. It is not practical to rate reliability target with failure rate at the certain common test condition. The reliability target is determined corresponding to character of equipments taking design, manufacture, inner process quality control, screening and test method, etc. into consideration, and considering operating circumstances of equipments the semiconductor device used in, reliability target of system, derating applied in design, operating condition, maintenance, etc.

2.2 Reliability Design

To achieve the reliability required based on reliability targets, timely sude and execution of design standardization, device design (including process design, structure design), design review, reliability test are essential.

(1) Design Standardization

Establishment of design rule, and standardization of parts, material and process are necessary. As for design rule, critical items on quality and reliability are always studied at circuit design, device design, layout design, etc. Therefore, as long as standardized process, material, etc. are used, reliability risk is extremely small even in new development devices, only except for in the case special requirements in function needed.

(2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in the case new process and new material are employed, technical study is deeply executed prior to device development.

(3) Reliability Evaluation by Test Site

Test site is sometimes called Test Pattern. It is useful method for design and process reliability evaluation of IC and LSI which have complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode
   - Analysis of relation between failure mode and manufacturing process condition
   - Search for failure mechanism analysis
   - Establishment of QC point in manufacturing
2. Effectiveness of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and comparison can be made with process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

   etc.

2.3 Design Review

Design review is organized method to confirm that design satisfies the performance required including users' and design work follows the specified ways, and whether or not technical improved items accumulated in test data of individual major fields and field data are effectively built in. In addition, from the standpoint of enhancement of competitive power of products, the major purpose of design review is to ensure quality and reliability of the products. In Hitachi, design review is performed from the planning stage for new products and even for design changed products. Items discussed and determined at design review are as follows;

(1) Description of the products based on specified design documents.
(2) From the standpoint of specialty of individual participants, design documents are studied, and if unclear matter is found, sub-program of calculation, experiments, investigation, etc. will be carried out.
(3) Determine contents of reliability and methods, etc. based on design document and drawing.
(4) Check process ability of manufacturing line to achieve design goal.
(5) Discussion about preparation for production.
(6) Planning and execution of sub-programs for design change proposed by individual specialist, and for tests, experiments and calculation to confirm the design change.
(7) Reference of past failure experiences with similar devices, confirmation of method to prevent them, and planning and execution of test program for confirmation of them. These studies and decisions are made using check lists made individually depending on the objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

General views of overall quality assurance in Hitachi are as follows;

(1) Problems in individual process should be solved in the

process. Therefore, at final product stage, the potential failure factors have been already removed.

(2) Feedback of information should be made to ensure satisfied level of process ability.

(3) To assure reliability required as an result of the things mentioned above is the purpose of quality assurance.

The followings are regarding device design, quality approval at mass production, inner process quality control, product inspection and reliability tests.

3.2 Quality Approval

To ensure quality and reliability required, quality approval is carried out at trial production stage of device design and mass production stage based on reliability design described at section 2.

The views on quality approval are as follows;

(1) The third party performs approval objectively from the standpoint of customers.

(2) Fully consider past failure experiences and information from field.

(3) Approval is needed for design change and work change.

(4) Intensive approval is executed on parts material and process.

(5) Study process ability and fluctuation factor, and set up control points at mass production stage.

Considering the views mentioned above, quality approval shown in Fig. 1 is performed.

3.3 Quality and Reliability Control at Mass Production

For quality assurance of products in mass production, quality control is executed with organic division of functions in manufacturing department, quality assurance department, which are major, and other departments related. The total function flow is shown in Fig. 2. The main points are described below.

3.3.1 Quality Control of Parts and Material

As the performance and the reliability of semiconductor devices are getting higher, importance is increasing in quality control of material and parts, which are crystal, lead frame, fine wire for wire bonding, package, to build products, and materials needed in manufacturing process, which are mask pattern and chemicals. Besides quality approval on parts and materials stated in section 3.2, the incoming inspection is, also, key in quality control of parts and materials. The incoming inspection is performed based on incoming inspection specification following purchase specification and drawing, and sampling inspection is executed based on MIL-STD-105D mainly.

The other activities of quality assurance are as follows:

(1) Outside Vendor Technical Information Meeting

(2) Approval on outside vendors, and guidance of outside vendors

(3) Physical chemical analysis and test

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

Inner process quality control is performing very important function in quality assurance of semiconductor devices. The following is description about control of semi-final products, final products, manufacturing facilities, measuring equipments,

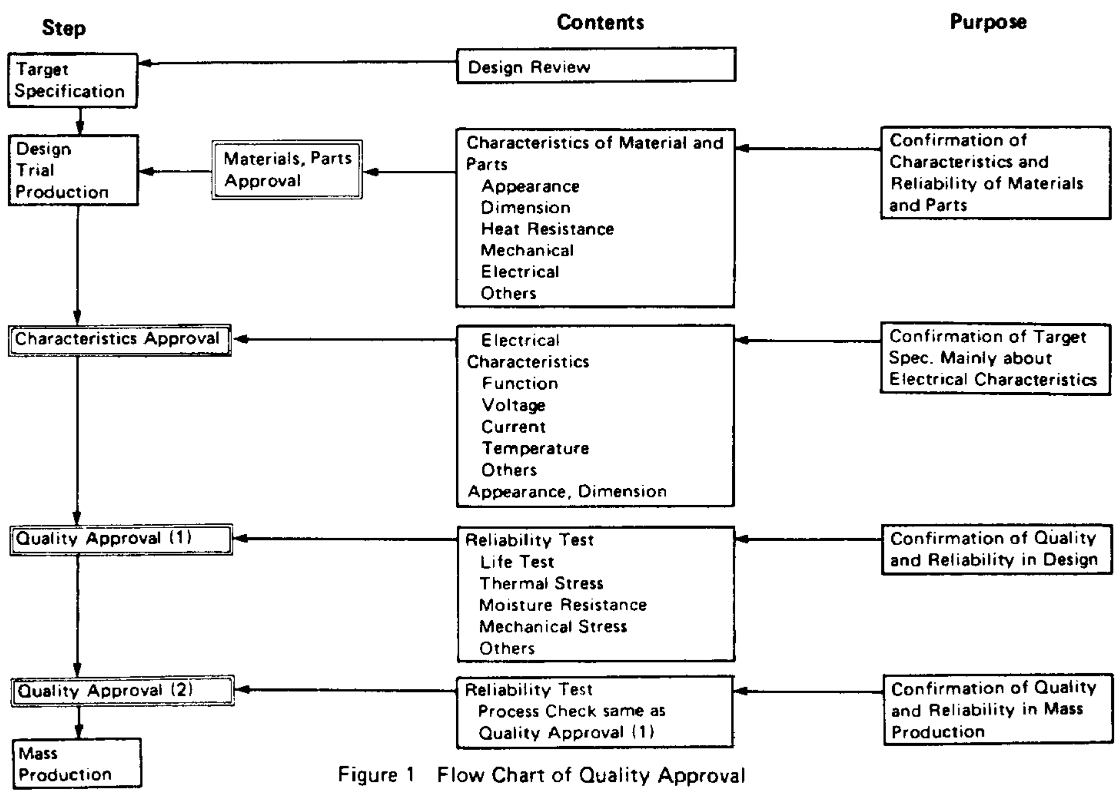


Figure 1 Flow Chart of Quality Approval

circumstances and sub-materials. The quality control in the manufacturing process is shown in Fig. 3 corresponding to the manufacturing process.

(1) Quality Control of Semi-final Products and Final Products

Potential failure factors of semiconductor devices should be removed preventively in manufacturing process. To achieve it, check points are set-up in each process, and products which have potential failure factor are not transfer to the next process. Especially, for high reliability semiconductor devices, manufacturing line is rigidly selected, and the quality control in the manufacturing process is tightly executed – rigid check in each process and each lot, 100% inspection in appropriate ways to remove failure factor caused by manufacturing fluctuation, and execution of screening needed, such as high temperature aging and temperature cycling. Contents of inner process quality control are as follows;

- Condition control on individual equipments and workers, and sampling check of semifinal products.
- Proposal and carrying-out improvement of work
- Education of workers
- Maintenance and improvement of yield
- Picking-up of quality problems, and execution of counter-measures
- Transmission of information about quality

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Equipments for manufacturing semiconductor devices have been developing extraordinarily with necessary high performance devices and improvement of production, and are important factors to determine quality and reliability. In Hitachi, automatization of manufacturing equipments are promoted to improve manufacturing fluctuation, and controls are made to maintain proper operation of high performance equipments and perform the proper function. As for maintenance inspection for quality control, there are daily inspection which is performed daily based on specification related, and periodical inspection which is performed periodically. At the inspection, inspection points listed in the specification are checked one by one not to make any omission. As for adjustment and maintenance of measuring equipments, maintenance number, specification are checked one by one to maintain and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-materials

Quality and reliability of semiconductor device is highly

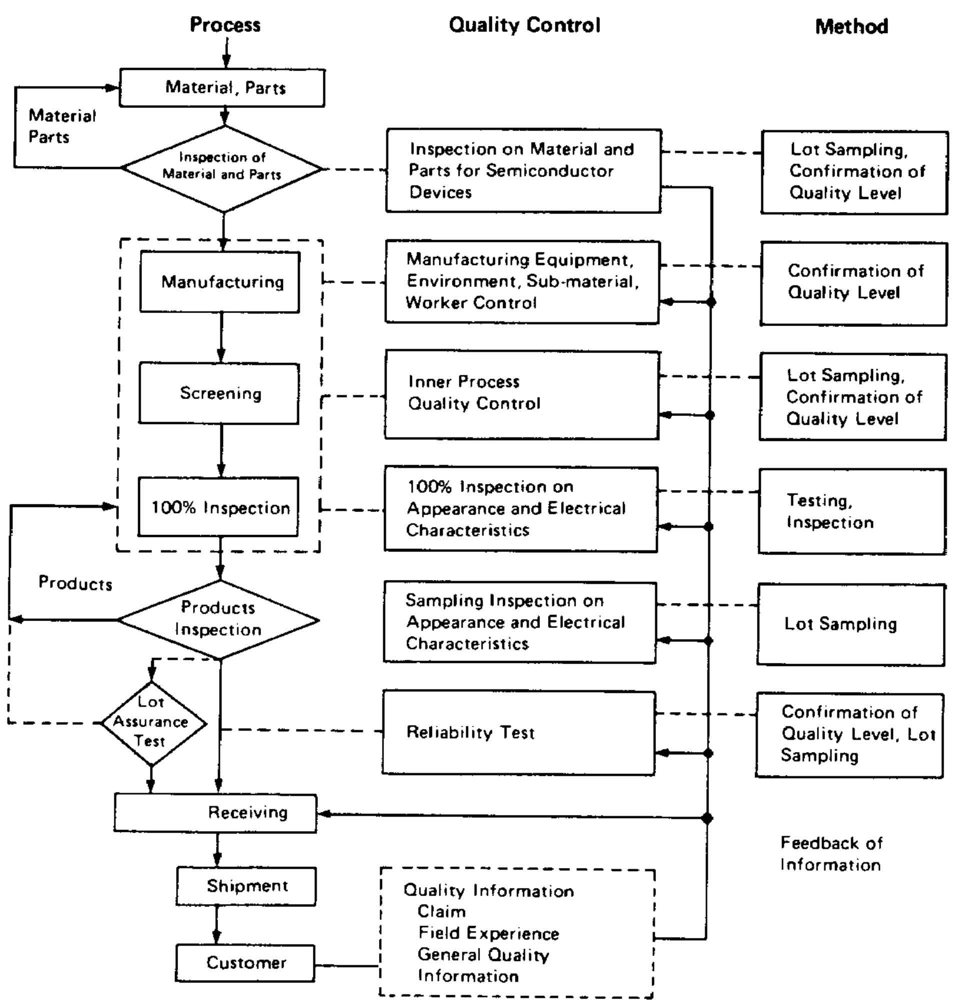


Figure 2 Flow Chart of Quality Control in Manufacturing Process

affected by manufacturing process. Therefore, the controls of manufacturing circumstances – temperature, humidity, dust – and the control of submaterials – gas, pure water – used in manufacturing process are intensively executed. Dust control is described in more detail below.

Dust control is essential to realize higher integration and higher reliability of devices. In Hitachi, maintenance and improvement of cleanness in manufacturing site are executed with paying intensive attention on buildings, facilities, air-conditioning systems, materials delivered-in, clothes, work, etc., and periodical inspection on floating dust in room, falling dusts and dirtiness of floor.

3.3.3 Final Product Inspection and Reliability Assurance

(1) Final Product Inspection

Lot inspection is done by quality assurance department for products which were judged as good products in 100% test, which is final process in manufacturing department. Though 100% of good products is expected, sampling inspection is executed to prevent mixture of failed products by mistake of work, etc. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Lot inspection is executed based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability of semiconductor devices, periodical reliability tests and reliability tests on individual manufacturing lot required by user are performed.

Table 1 Quality Control Check Points of Material and Parts (Example)

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

	Process	Control Point		Purpose of Control
	Purchase of Material			
Wafer		Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
	Surface Oxidation	Oxidation		Assurance of Resistance
	Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
	Photo Resist	Photo Resist		
	Inspection on Photo Resist		Dimension, Appearance	Dimension Level
	◇ PQC Level Check			Check of Photo Resist
	Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
	Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc.) Cleanness of surface,
	◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	Prior Check of V_{IH} Breakdown Voltage Check
	Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
	Inspection on Evaporation			
	◇ PQC Level Check			
	Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
	Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
	Chip Scribe		Appearance of Chip	
	Inspection on Chip Appearance			
	◇ PQC Lot Judgement			
Frame	Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
			Appearance after Wire Bonding	Quality Check of Wire Bonding
	◇ PQC Level Check		Pull Strength, Compression Width, Shear Strength	Prevention of Open and Short
	Inspection after Assembling		Appearance after Assembling	
	◇ PQC Lot Judgement			
Package	Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
	◇ PQC Level Check	Marking	Marking Strength	
	Final Electrical Inspection			
	◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
	Appearance Inspection			
	Sampling Inspection on Products			
	Receiving			
	Shipment			

Figure 3 Example of Inner Process Quality Control

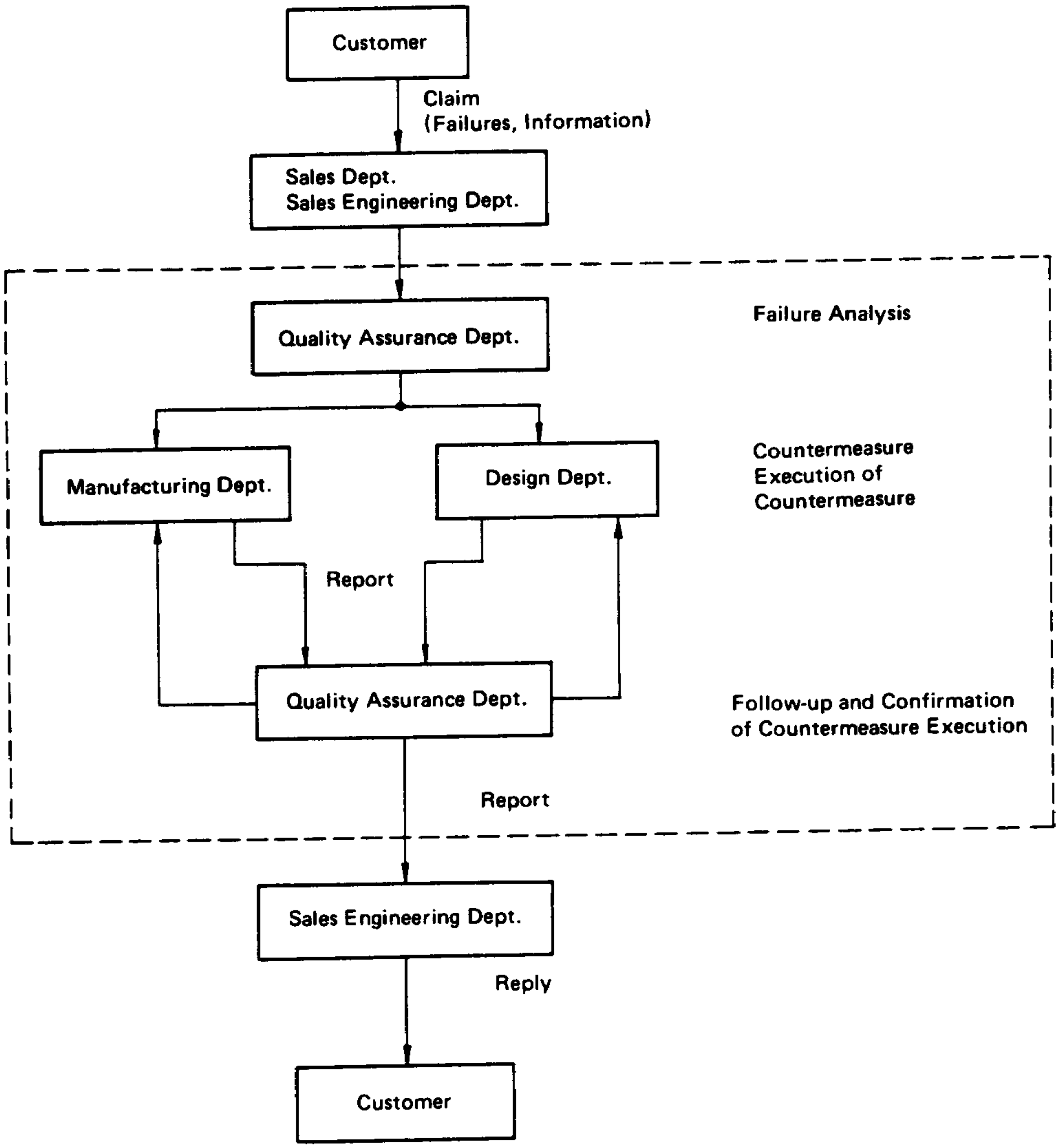


Figure 4 Process Flow Chart of Field Failure

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RELIABILITY TEST DATA OF MICROCOMPUTER

1. INTRODUCTION

Microcomputer is required to provide higher reliability and quality with increasing function, enlarging scale and widening application. To meet this demand, Hitachi is improving the quality by evaluating reliability, building up quality in process, strengthening inspection and analyzing field data etc..

This chapter describes reliability and quality assurance data for Hitachi 8-bit single-chip microcomputer based on test and failure analysis results. More detail data and new information will be reported in another reliability data sheet.

2. PACKAGE AND CHIP STRUCTURE

2.1 Package

The reliability of plastic molded type has been greatly improved, recently their applications have been expanded to automobiles measuring and control systems, and computer terminal equipment operated under relatively severe conditions and production output and application of plastic molded type will continue to increase.

To meet such requirements, Hitachi has considerably improved moisture resistance, operation stability, and chip and plastic manufacturing process.

Plastic package type structure is shown in Figure 1 and Table 1.

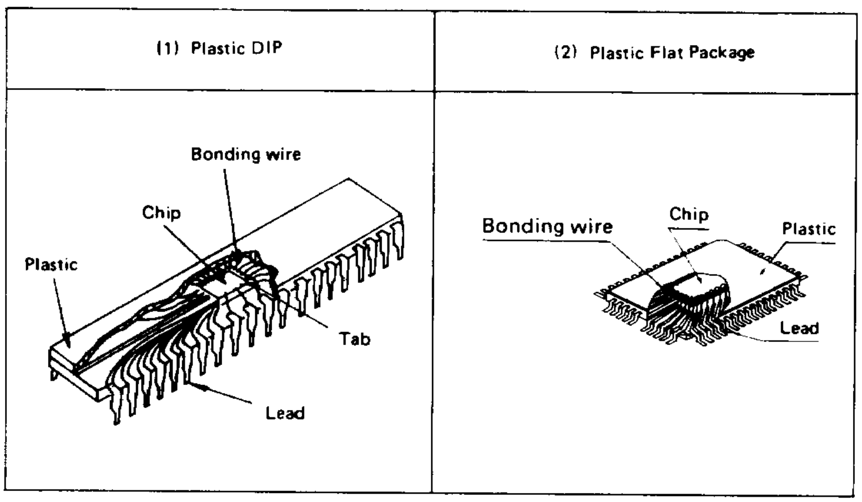


Figure 1 Package Structure

Table 1 Package Material and Properties

Item	Plastic DIP	Plastic Flat Package
Package	Epoxy	Epoxy
Lead	Solder dipping Alloy 42or Cu	Solder plating Alloy 42
Die bond	Au-Si or Ag paste	Au-Si or Ag paste
Wire bond	Thermo compression	Thermo compression
Wire	Au	Au

2.2 Chip Structure

HMCS6800 family are produced in NMOS E/D technology or low power CMOS technology. Si-gate process is used in both types because of high reliability and high density.

Chip structure and basic circuit are shown in Figure 2.

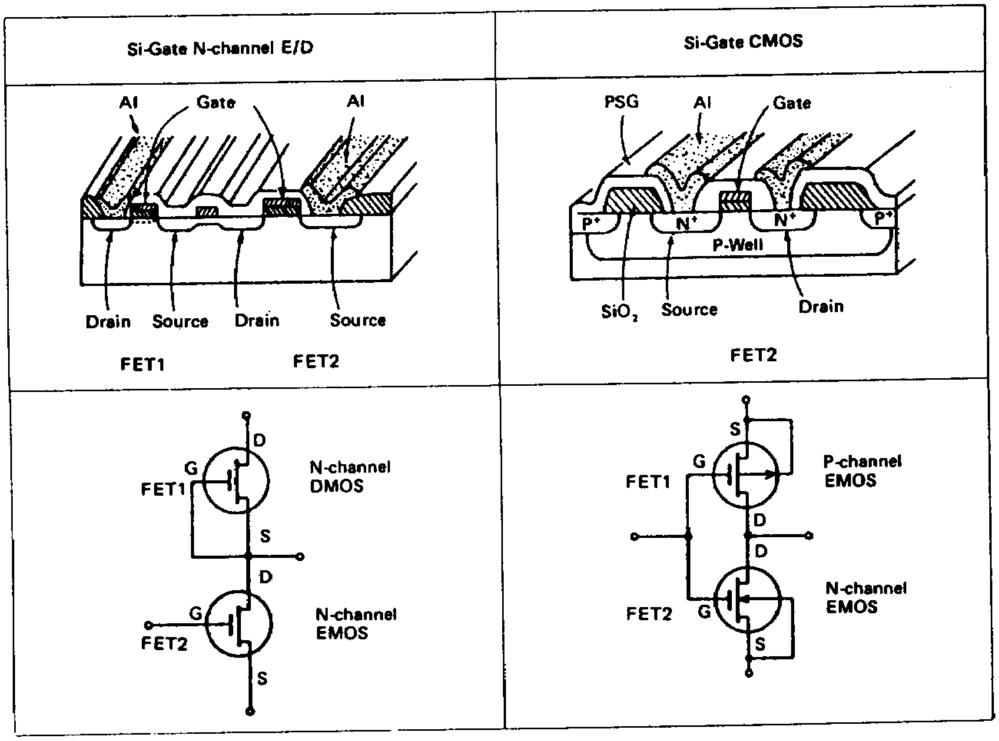


Figure 2 Chip Structure and Basic Circuit

3. QUALITY QUALIFICATION AND SCREENING STANDARDS AND EVALUATION

3.1 Reliability Test Methods

Reliability test methods shown in Table 2-1 are used to qualify and evaluate the new products and new process. The data in devices for various reliability tests.

Table 2.1

Test Items	Test Condition	MIL-STD-883B Method No.
Operating Life Test	125°C, 1000 hrs.	1005,2
High Temperature, Storage Low Temperature, Storage Steady State Humidity Steady State Humidity Biased	Tstg max. 1000 hrs. Tstg min. 1000 hrs. 65°C 95% RH, 1000 hrs. 85°C 85% RH, 1000 hrs.	1008,1
Temperature Cycling Temperature Cycling Thermal Shock Soldering Heat Mechanical Shock Vibration Fatigue Variable Frequency Constant Acceleration Lead Integrity	-55°C ~ 150°C, 10 cycles -20°C ~ 125°C, 200 cycles 0°C ~ 100°C, 100 cycles 260°C, 10 sec 1500G 0.5 msec, 3 times/X, Y, Z 60Hz 20G, 32 hrs./X, Y, Z 20 ~ 2000Hz 20G, 4 min./X, Y, Z 20000G, 1 min./X, Y, Z 225gr, 90° 3 times	1010,4 1011,3 2002,2 2005,1 2007,1 2001,2 2004,3

Table 2.2 LTPD % Comparison for Different Device Grades (J-Version)

Test	Condition	Industrial, Automotive (J-Version)	Standard
Operating Life Test	125°C, 1000 hrs.	5	10
High Temperature Storage	T_{stg} max. 1000 hrs.	5	10
Low Temperature Storage	T_{stg} min. 1000 hrs.	5	10
Moisture Resistance	65°C/95% RH, 1000 hrs.	2	5
Moisture Resistance	85°C/85% RH Bias,1000 hrs.	5	10
Moisture Resistance	65°C~10°C, Over 90% RH, 10 cycles	5	10
Temperature Cycling	-55°C ~ 150°C, 10 cycles	0.2	0.5
	-20°C ~ 125°C, 2k cycles	5	—
	-20°C ~ 125°C, 200 cycles	—	5
	150°C ~ -65°C, 15 cycles	10	—
	100°C ~ 0°C, 15 cycles	—	10
Soldering Heat	260°C, 10 sec.	10	15
Solderability	230°C, 5 sec.	20	20
Lead Integrity	225 gr., 90°, 3 times	10	15
Mechanical Shock	1500 G, 0.5 msec, 3 times/X, Y, Z	10	15
Vibration Fatigue	60 Hz, 20 G, 32 hrs./X, Y, Z	10	15
Variable Frequency	20 Hz, ~ 2000 Hz, 20 G, 4 min./X, Y, Z	10	15
Constant Acceleration	20,000 G, 1 min./X, Y, Z	10	15

(LTPD %, Confidence Level 90%)

3.2 Reliability Test Results

Reliability test results of standard 8-bit single-chip microcomputer devices are shown in Table 3 to Table 7. There is little difference according to device series, as the design and production process, etc. are standardized.

Table 3 Standard Dynamic Life Test

Device Type	Sample Size	Component Hours	Failures
HD6801P	191 pcs.	191000	0
HD6805P	114	114000	0
HD6301P	336	336000	0
HD6305P	154	154000	0
HD63L05P	77	77000	0
HD68P01	45	45000	0
HD63P01	45	45000	0
HD68P05	45	45000	0

Estimated Field Failure Rate
= 0.016%/1000 hrs at Ta = 75°C for NMOS (HD6801P, HD6805P)
= 0.009%/1000 hrs at Ta = 75°C for CMOS (HD6301P, HD6305P)
(Activation Energy 0.7eV, Confidence Level 60%)

Table 4 Standard High Temperature, High Humidity Test (Moisture Resistance Test)

(1) 85°C 85%RH Bias Test

Device Type	V_{CC} Bias	168 hrs	500 hrs	1000 hrs
HD6801P	5.5V	0/45	0/45	0/45
HD6805P	5.5V	0/90	0/90	0/90
HD6301P	5.5V	0/176	0/131	0/131
HD6305P	5.5V	0/45	0/45	0/45

(2) High Temperature-High Humidity Storage Life Test

Device Type	Condition	168 hrs	500 hrs	1000 hrs
HD6801P	65°C 95% RH	0/90	0/90	0/90
HD6805P	65°C 95% RH	0/135	0/135	0/135
HD6301P	65°C 95% RH	0/603	0/603	0/603
HD6301P	65°C 95% RH	0/234	0/234*	0/233
HD6301F	65°C 95% RH	0/77	0/77	0/77
HD6305P	65°C 95% RH	0/112	0/112	0/112
HD6305F	65°C 95% RH	0/45	0/45	0/45
HD63L05FP	65°C 95% RH	0/160	0/160	0/160

*Aluminum corrosion

(3) Pressure Cooker Test
(Condition: 2 atm 121°C)

Device Type	40 hrs	60 hrs	100 hrs	200 hrs
HD6801P	0/45	0/45	0/45	0/45
HD6805P	0/44	0/44	0/44	0/44
HD6301P	0/135	0/135	0/135	0/135
HD6301F	0/110	0/110	0/110*	0/109*
HD6305P	0/88	0/88	0/88	0/88
HD6305F	0/44	0/44	0/44	0/44
HD63L05FP	0/80	0/80	0/80*	2/79**

*Leakage current
**Leakage current and Aluminum corrosion

(4) MIL-STD-883B Moisture Resistance Test
(Condition: 65°C ~ −10°C, over 90% RH)

Device Type	10 cycles	20 cycles	40 cycles
HD6801P	0/50	0/50	0/50
HD6805P	0/32	0/32	0/32
HD6301P	0/75	0/75	0/75
HD6301F	0/45	0/45	0/45
HD6305P	0/77	0/77	0/77
HD6305F	0/45	0/45	0/45
HD63L05FP	0/22	0/22	0/22

Table 5 Standard Temperature Cycling Test

(Condition; -55°C ~ 25°C ~ 150°C)

Device Type	10 cycles	100 cycles	200 cycles
HD6801P	0/102	0/102	0/102
HD6805P	0/442	0/90	0/90
HD6301P	0/510	0/258	0/258
HD6305P	0/364	0/154	0/154
HD68P01	0/44	0/44	0/44
HD63P01	0/45	0/45	0/45
HD68P05	0/90	0/41	0/41

Table 6 Standard High Temperature, Low Temperature Storage Life Test

Device Type	Ta	168 hrs	500 hrs	1000 hrs
HD6801P	150°C	0/112	0/112	0/112
	-55°C	0/45	0/45	0/45
HD6805P	150°C	0/154	0/154	0/154
	-55°C	0/44	0/44	0/44
HD6301P	150°C	0/180	0/180	0/180
	-55°C	0/88	0/88	0/88
HD6305P	150°C	0/135	0/135	0/135
	-55°C	0/44	0/44	0/44
HD63L05P	150°C	0/88	0/88	0/88
	-55°C	0/22	0/22.	0/22

Table 7 Mechanical and Environmental Test

Test Item	Condition	Plastic DIP		Flat Plastic Package	
		Sample Size	Failure	Sample Size	Failure
Thermal Shock	0°C ~ 100°C 10 cycles	110	0	100	0
Soldering Heat	260°C, 10 sec.	180	0	22	0
Salt Water Spray	35°C, NaCl 5% 24 hrs	110	0	22	0
Solderability	230°C, 5 sec. Rosin flux	159	0	34	0
Drop Test	75cm, maple board 3 times	110	0	22	0
Mechanical Shock	1500G, 0.5ms 3 times/X, Y, Z	110	0	22	0
Vibration Fatigue	60 Hz, 20G 32hrs/X, Y, Z	110	0	22	0
Vibration Variable Freq.	100 ~ 2000Hz 20G, 4 times/X, Y, Z	110	0	22	0
Lead Integrity	225g, 90° Bending 3 times	110	0	22	0

4. PRECAUTION

4.1 Storage

It is preferable to store semiconductor devices in the following ways to prevent detrioration in their electrical characteristics, solderability, and appearance, or breakage.

(1) Store in an ambient temperature of 5 to 30°C, and in a relative humidity of 40 to 60%.
(2) Store in a clean air environment, free from dust and active gas.
(3) Store in a container which does not induce static electricity.
(4) Store without any physical load.
(5) If semiconductor devices are stored for a long time, store them in the unfabricated form. If their lead wires are formed beforehand, bent parts may corrode during storage.
(6) If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30°C or lower. Unpacked devices must not be stored for over 3 months.
(7) Take care not to allow condensation during storage due to rapid temperature changes.

4.2 Transportation

As with storage methods, general precautions for other electronic component parts are applicable to the transportation of semiconductors, semiconductor-incorporating units and other similar systems. In addition, the following considerations must be given, too:

(1) Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive container or aluminium foil.
(2) In order to prevent device breakage from clothes-induced static electricity, workers should be properly grounded with a resistor while handling devices. The resistor of about 1 M ohm must be provided near the worker to protect from electric shock.
(3) When transporting the printed circuit boards on which semiconductor devices are mounted, suitable preventive measures against static electricity induction must be taken; for example, voltage built-up is prevented by shorting terminal circuit. When a belt conveyor is used, prevent the conveyor belt from being electrically charged by applying some surface treatment.
(4) When transporting semiconductor devices or printed circuit boards, minimize mechanical vibration and shock.

4.3 Handling for Measurement

Avoid static electricity, noise and surge-voltage when semiconductor devices are measured. It is possible to prevent breakage by shorting their terminal circuits to equalize electrical potential during transportation. However, when the devices are to be measured or mounted, their terminals are left open to provide the possibility that they may be accidentally touched by a worker, measuring instrument, work bench, soldering iron, belt conveyor, etc. The device will fail if it touches something which leaks current or has a static charge. Take care not to allow curve tracers, synchroscopes, pulse generators, D.C. stabilizing power supply units etc. to leak current through their terminals or housings.

Especially, while the devices are being tested, take care not to apply surge voltage from the tester, to attach a clamping circuit to the tester, or not to apply any abnormal voltage through a bad contact from a current source.

During measurement, avoid miswiring and short-circuiting. When inspecting a printed circuit board, make sure that no soldering bridge or foreign matter exists before turning on the power switch.

Since these precautions depend upon the types of semiconductor devices, contact Hitachi for further details.

4.4 Soldering

Semiconductor devices should not be left at high temperatures for a long time. Regardless of the soldering method, soldering must be done in a short time and at the lowest possible temperature. Soldering work must meet soldering heat test conditions, namely, 260°C for 10 seconds and 350°C for 3 seconds at a point 1 to 1.5 mm away from the end of the device package.

Use of a strong alkali or acid flux may corrode the leads, deteriorating device characteristics. The recommended soldering iron is the type that is operated with a secondary voltage supplied by a transformer and grounded to protect from lead current. Solder the leads at the farthest point from the device package.

4.5 Removing Residual Flux

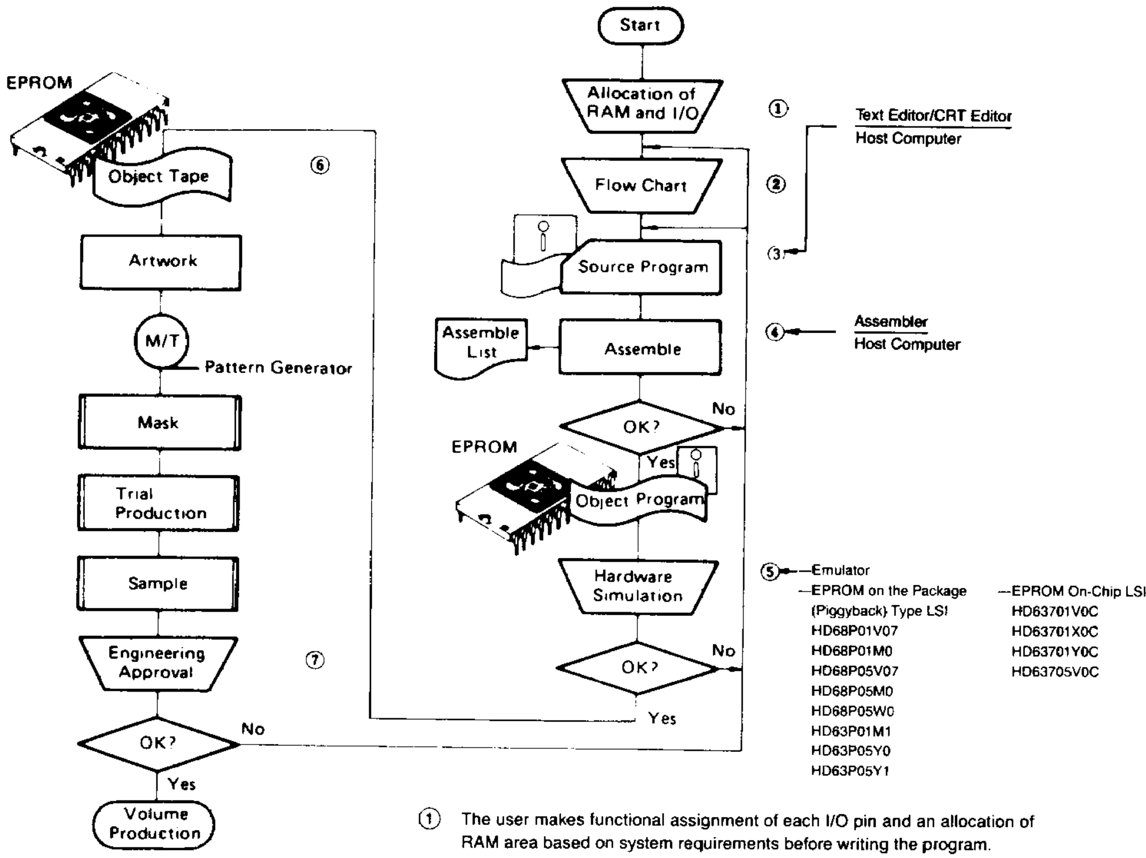
To ensure the reliability of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If chloric detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures will cause swollen chip coating due to solvent permeation, select the type of detergent and cleaning condition carefully. Do not use any trichloroethylene solvent. For ultrasonic cleaning, the following conditions are advisable:

- Frequency: 28 to 29 kHz (to avoid device resonation)
- Ultrasonic output: 15W/ℓ
- Keep the devices out of direct contact with the power generator.
- Cleaning time: Less than 30 seconds

DESIGN PROCEDURE AND SUPPORT TOOLS FOR 8-BIT SINGLE-CHIP MICROCOMPUTER

Hitachi sells software cross assemblers and hardware emulators that operate with various host computers. These support tools aid in the development of the user's program. The user's program is transmitted to the factory and mask programmed into the ROM portion of the microcomputer. The finished mask programmed devices are shipped by Hitachi.

Figure 1 shows the typical program design procedure and Table 1 shows support tools for 8-bit single-chip microcomputers.



① The user makes functional assignment of each I/O pin and an allocation of RAM area based on system requirements before writing the program.

② The user prepares and follows a flowchart determined by system requirements to write the program in mnemonic code.

③ The user prepares a source program on floppy disk from the encoded program.

④ The user assembles and complies the source program on a host computer to generate the object program and detect assembly errors.

⑤ The user verifies the program with a hardware emulator, EPROM on-chip LSI, or EPROM on the package (piggyback) type microcomputer.

⑥ The user sends the completed program in EPROM to Hitachi along with completed ordering specification form and mask option list.

⑦ Hitachi prepares masks for the ROM and mask options according to the information sent by the user. Hitachi manufactures and ships sample devices to the user. Mass production can begin after the user evaluates and confirms that the program is correct in the sample devices.

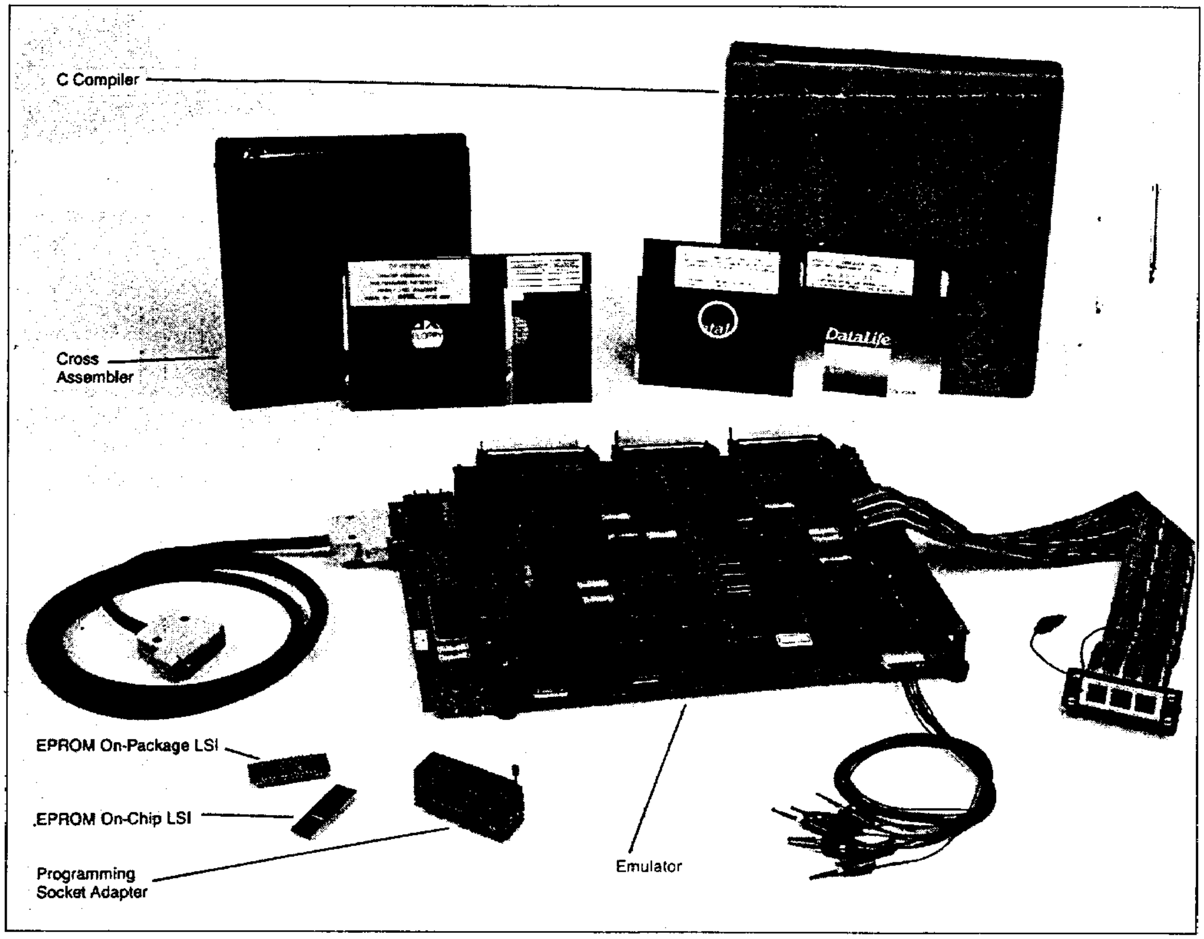
Figure 1 Program Design Procedure

Table 1: SYSTEM DEVELOPMENT SUPPORT TOOLS

Description	Tool Part No. \ Device Type	HD6301V1, HD6303R, HD63P01M1, HD63701V0	HD6301X0, HD6303X, HD63701X0	HD6301Y0, HD6303Y, HD63701Y0	HD6305U0, HD6305V0, HD63705V0	HD6305X0, HD6305X1, HD6305X2	HD6305Y0, HD6305Y1, HD6305Y2, HD63P05Y0	HD63L05F1	HD65901	HD6801S0, HD6801V0, HD6803, HD68P01M0, HD68P01V07	HD6805S1, HD6805U1, HD6805V1, HD68P05M0, HD68P05V07	HD6805T2(7)	HD6805W1, HD68P05W0
Emulator	HS31VEML04H(1) (H31MIX4)(2)	●											
	HS31XEML02H(1) (H31MIX2)(2)		●										
	HS31YEML03H(1) (H31MIX3)(2)			●									
	HS35VEML03H(1) (H35MIX3)(2)				●								
	HS35YEML05H(1) (H35MIX5)(2)					●	●						
	H3L5EVT1(1)							●					
	H61EVT2(1)									●			
	H65EVT2(1)										●		
	H65EVT3(1)												●
Evaluation Board	HD65901EV Board								●				
Emulation Memory Board up to 64k Byte	H64EMB01									●			
	H64EMB02		●	●									
Programing Socket Adapter	H31VSA01A	●											
	H35VSA01A				●								
	H67PWA01		●										
	HS31YESS11H			●									
Cross Assembler (IBM PC)	S31IBMPC(3)	●	●	●						●			
	S35IBMPC(3)				●	●	●	●			●	●	●
	HD65901XASM(4)								●				
C Compiler (IBM PC)	US31PCLI1SF(3)	●	●	●									
Documentation	Data Sheet #U71(5)	●	●	●	●	●	●	●	(8)	●	●	●	●
	Handbook #U07(6)	●	●	●									
	Handbook #U08(6)				●	●	●	●					
	Application Note Surface Mount Package User's Manual (#M15)	●	●	●	●	●	●	●					

(NOTE)
1. Emulators include an RS-232C port for connection to IBM PC, or PC compatible machines. Software not included.
2. Same as footnote (1) above, but shipped with cross assembler (8" floppy disk) that operates with Hitachi's H68SD5 development system.
3. Developed by one of Hitachi's engineering subsidiaries. Cross assemblers include software utility to download/upload code between PC host and emulator.
4. Includes cross assembler and software simulator.
5. Data sheets are found in databook #U71.
6. Includes user's manuals, hardware and software application notes, and other relevant information.
7. Not available from Hitachi. Use third party vendor support tool.
8. User's manual/data sheet.

IBM PC is a trademark of International Business Machine Corporation.



Typical Support Tools

■ SINGLE-CHIP MICROCOMPUTER SUPPORT SYSTEMS

Hitachi and its engineering subsidiaries make hardware and software support tools to operate with many popular host computers and expedite the development of the microcomputer-based target system. The support system includes in-circuit emulators, cross assemblers, passive socket adapters for easily programming EPROM on-chip devices, and documentation.

In addition to hardware and software support, Hitachi has Field Application Engineers (FAE) to help identify the most cost-effective IC(s) for your application and answer your technical questions.

■ IN-CIRCUIT EMULATOR FUNCTIONS*

- Serial interface connection to many host computers via RS-232C port.
- Executes user's program in real-time on some emulators, or when loaded in emulator's memory starting from a selected address. Execution is interrupted when breakpoints are detected, or when RESET or ABORT is switched.
- Single step tracing of user's program is possible. Data in registers and data in memory are displayed after every execution.
- Breakpoints can be set in user's program by using the program counter address, data bus, or external signal probes. Breakpoints can be displayed and changed.
- Data in internal registers of the subject microcomputer can be displayed or changed.
- Real-time tracing is possible on most emulators; the emulator stores and displays bus data and external signals for up to 1011 machine cycles on some emulators, or 2035 machine cycles on other emulators before and after the address where a breakpoint is set.
- Line assembler and disassembler on some emulators.

*Functions listed in the overview may not exactly apply to all emulators. Refer to the applicable emulator user's manual for further information.

■ CROSS ASSEMBLER FUNCTIONS (PC-DOS)

The software is divided into six main parts.

- **Structured Relocatable Cross Macro Assembler**

  The cross assembler is designed to meet the specification outlined in Hitachi's HD6301 and HD6305 assembler user's manual, which means that mnemonic, macro and directive compatability is maintained.

  The assembler also offers a structured code facility, similar to that found in some high level languages. The main structured features are listed below:

  IF . . . THEN . . . ELSE . . . DO . . . WHILE . . . REPEAT . . . UNTIL . . . FOR . . . TO
  CALL (with parameters passed on the stack)
- **Linker**

  The linker concatenates and locates all relocatable modules into an executable object file (Motorola S-type format). Start addresses of relocatable program and data sections can be entered at linkage time.

- **Macro Librarian**
  Named libraries of useful macros can be built by the user, saving time during generation of source code. The macro librarian is searched during assembly time for the appropriate macro definitions that do not appear in the source file.
- **Object Module Librarian**
  Named libraries of useful object modules can be built by the user. The libraries called up at linkage time are searched by the linker to see if unsatisfied external references can be resolved. Object modules which satisfy the unresolved references are automatically included in the executable object file (S-record format).
- **Emulator Interface Software**
  The interface software allows connection between Hitachi's serially linked emulators and the IBM PC using an RS232 asynchronous interface.
  Commands from the PC keyboard are directed to the emulator and responses are displayed on the screen. File upload and download in Motorola S-type format enables assembled and linked programs to be run on the emulator. Real time trace facilities are available on all serial linked emulators.
- **EPROM Programmer Interface Software**
  The interface software allows connection to most proprietary EPROM Programmers for downloading (or uploading) executable object modules in Motorola S-type* data format. The programmers can be run either in REMOTE CONTROL or LOCAL mode.
  In local mode, programmer commands can be entered on the programmer keyboard and upload/download of object modules can be activated using the IBM PC keyboard.
  In remote control mode, all programmer commands are entered via the IBM PC keyboard.
  All programmer commands will be specific to the particular programmer used.

■ C COMPILER FUNCTIONS (PC-DOS)

The HD6301 and HD6303** compiler comprises three programs, a pre-processor, the main compiler and an optimiser. The system also provides standard library files (which facilitates I/O and floating point operations), the standard "include" files which contain the necessary declarations for the usage of library function. Runtime object files for integer and floating point arithmetic are included. Compatible with Hitachi and Microtec Research*** assemblers.

- **Compiler Options**
  The following tables indicate the options available during pre-processing and compiling.

*Motorola S-type is a trademark of Motorola, Inc.
**Conforms to Kerninghan and Ritchie C programming language standard rather than ANSI C programming language standard.
***Microtec Research is a trademark of Microtec Research, Inc.

Table 1. Pre-processor Options

No.	Option	Description
1	A	Issues error messages to the pre-processor source program file.
2	D	Defines a macro name
3	L	Inserts the original source program lines into the pre-processed source program as comments.

Table 2. Compiler Options

No.	Option	Description
1	P	Generates object code which calls a profiler routine (a routine which profiles the history of the program execution) everytime a function is called (see Note 1).
3	L	Generates object code which calls a stack check routine everytime a function is called (see Note 1).

Note 1: The profiler routine and the stack check routine should be prepared in a separate module for your own target system.

- **Limits in Compilation**
  (1) Length of an input line: 512 characters
  (2) Length of a character string: 510 characters
  (3) Number of external names: 156
  (4) Effective length of identifiers: 8 characters
  (5) Effective length of external identifiers: 6
  (6) Nest of conditional complication: 32 level
  (7) Nesting of file inclusion: 14 level
  (8) Number of macro parameters: 32
  (9) Length of a macro definition: 512 characters
  (10) Recursive expansion of a macro name: 32 times
- **Data Size**
  (1) Char type: 8 bit
  (2) Short type, int type: 16 bit
  (3) Long type: 32 bit
  (4) Float type: 32 bit
  (5) Double type: 64 bit
  (6) Pointer type: 16 bit
  No data alignment is done in allocation of structured data

(3) *Character Handling Library Functions*
isalnum, isalpha, issascii, iscntl, isdigit, islower, isprint, ispunct, isspace, isupper, tolower, toupper.

(4) *Character String Handling Library Functions*
index, rindex, strcat, strcmp, strcpy, strlen, strncat, strncopy

(5) *Data Conversion Library Function*
atoi, atol

(6) *Memory Allocation Library Functions (see Note 2)*
malloc, calloc, free, cfree

(7) *Miscellaneous Library Functions*
NOTE 2: To use the I/O library functions and Memory allocation library functions, low level routines must be prepared by the user according to the target system requirements.