Genesys Logic, Inc.

GL652USB

USB 7 PORT HUB CONTROLLER

DATA SHEET, Version 1.2
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1 FEATURES

- High performance and low-cost solution for USB hub
- USB Specification Compliance
  - Conforms to USB specification Rev. 1.1
  - Supports 1 device address and 2 endpoints
- 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Single cycle instruction execution
  - Operation Speed: DC to 24 MHz clock input
  - Performance: 12 MIPS @ 24MHz
- I/O ports
  - 7-port hub
- Internal memory
  - 64 bytes of RAM
  - 1.75K × 14 of program ROM
- On-chip 3.3v output
  - No external regulator required
- Integrated USB transceiver
- 12 MHz external clock
- Improved output drivers with slew-rate control to reduce EMI
- Internal power-on reset(POR)
- Internal power-fail detector for ESD recovery
- Support suspend/normal mode power management
- Support power management for downstream port devices
- Automatic switching between self/bus powered mode
- Smart LED traffic indicator
  - The higher data traffic flows through one port, the higher frequency that port's LED will blink.
- Applications:
  - Stand-alone USB hub
  - PC motherboard USB hub
- 48 pin LQFP package

2 FUNCTION OVERVIEW

The GL652USB is an 8 port USB hub with 1 upstream port and 7 downstream ports. It uses an 8-bit RISC-like uC to encode/decode the host commands. The GL652USB is designed mainly for stand-alone hub and can also be integrated in PC motherboard or any other devices to support USB hub function. The GL652USB can switch between self-power and bus-power automatically without re-plug in. The GL652USB can be configured as individual mode or ganged mode for the power management of downstream port devices. To prevent from abnormal current consumption of downstream port devices, the GL652USB supplies power enable flags by reading the over-current flags. The GL652USB supports smart traffic indication through the LED lighting. The higher data traffic flows through one port, the higher frequency of that port's LED blinks. To minimize the power consumption, the GL652USB will turn LED off and stop the clock when they are suspended.

3 PIN DEFINITIONS AND DESCRIPTIONS

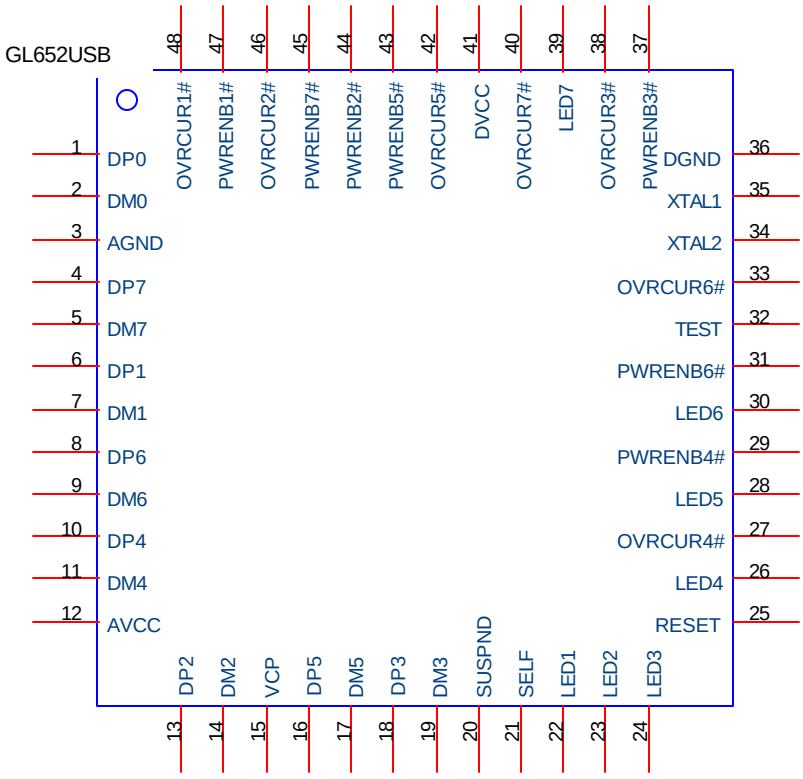
- GL652USB

Pin No.	Name	I/O	Description
1	DP0	I/O	Upstream port USB data+
2	DM0	I/O	Upstream port USB data-
3	AGND	-	Analog ground
4	DP7	I/O	Downstream port 7 USB data+
5	DM7	I/O	Downstream port 7 USB data-
6	DP1	I/O	Downstream port 1 USB data+
7	DM1	I/O	Downstream port 1 USB data-
8	DP6	I/O	Downstream port 6 USB data+
9	DM6	I/O	Downstream port 6 USB data-
10	DP4	I/O	Downstream port 4 USB data+
11	DM4	I/O	Downstream port 4 USB data-
12	AVCC	-	Analog VCC(5V)
13	DP2	I/O	Downstream port 2 USB data+
14	DM2	I/O	Downstream port 2 USB data-
15	VCP	-	3.3V output
16	DP5	I/O	Downstream port 5 USB data+
17	DM5	I/O	Downstream port 5 USB data-
18	DP3	I/O	Downstream port 3 USB data+
19	DM3	I/O	Downstream port 3 USB data-
20	SUSPND	O	Suspend indication output
21	SELF	I	1: SELF-powered. 0: INDIVIDUAL-powered
22	LED1	O	LED traffic indicator for downstream port 1
23	LED2	O	LED traffic indicator for downstream port 2
24	LED3	O	LED traffic indicator for downstream port 3
25	RESET	I	Reset input
26	LED4	O	LED traffic indicator for downstream port 4
27	OVCUR4#	I	Over current flag for downstream port4
28	LED5	O	LED traffic indicator for downstream port 5

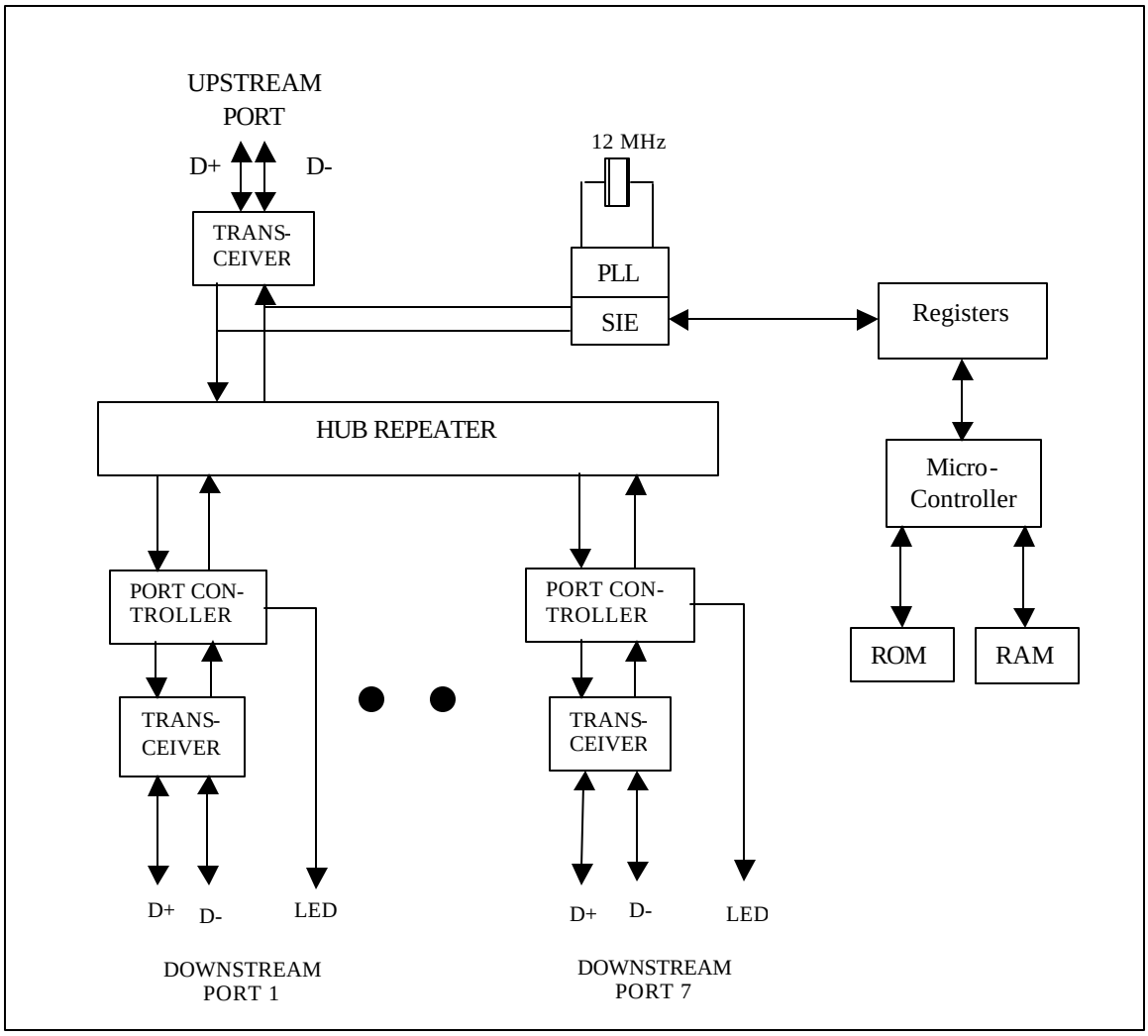
29	PWRENB4#	O	Power enable for downstream port 4
30	LED6	O	LED traffic indicator for downstream port 6
31	PWRENB6#	O	Power enable for downstream port 6
32	TEST	I	Test mode input
33	OVCUR6#	I	Over current flag for downstream port6
34	XTAL2	O	Ceramic resonator or crystal out
35	XTAL1	I	Ceramic resonator or crystal in
36	DGND	-	Digital ground
37	PWRENB3#	O	Power enable for downstream port 3
38	OVCUR3#	I	Over current flag for downstream port3
39	LED7	O	LED traffic indicator for downstream port 7
40	OVCUR7#	I	Over current flag for downstream port7
41	DVCC	-	Digital VCC(5V)
42	OVCUR5#	I	Over current flag for downstream port5
43	PWRENB5#	O	Power enable for downstream port 5
44	PWRENB2#	O	Power enable for downstream port 2
45	PWRENB7#	O	Power enable for downstream port 7
46	OVCUR2#	I	Over current flag for downstream port2
47	PWRENB1#	O	Power enable for downstream port 1
48	OVCUR1#	I	Over current flag for downstream port1

Note 1: "#" means low active
Note 2: If using crystal, TEST pull low. If using oscillator, TEST pull high.

Table 1 GL652USB Pin Definitions and Descriptions



4 BLOCK DIAGRAM



5 REGISTER SUMMARY

MNEMONIC	OFFSET	DESCRIPTION
DEVCTL	00h	Device control register
EVTFLG	01h	USB function interrupt flag
RXCTL0	02h	Endpoint 0 RX control
TXCTL0	03h	Endpoint 0 TX control
TXCTL1	04h	Endpoint 1 TX control
FFDAT	05h	Data buffer (FIFO) I/O port
BUFCTL	06h	Data buffer control register
PORTSEL	07h	Hub port to be configured
HUB_STAT_CHG	08h	Hub status and status change indicator
PORT_STATUS	09h	Hub ports status indicator
BUS_PORT_DATA	0Ah	Hub ports status change indicator
HOST_CMD	0Bh	Host command to downstream ports
ENP1_IND	0Ch	Endpoint 1 indicator
TRXFLAG	0Dh	Downstream port traffic flag
LED_INIT	0Eh	LED initial state
GPIOD	0Fh	General purpose I/O pin status
REV	10h	Chip revision
DEVSTUS	11h	USB device address and configuration status

Register Description

Terminology:

R/O:	read only
R/W:	read / write
R/W1C:	read / write “1” to clear
W/O:	write only

DEVCTL (offset 00, default = 00h)

R/W	*R/W*	*R/W*				*R/O*	*R/O*
USBRDY	SFRAME	PWRDN	--	--	--	SELF	GANG

USBRDY : 0 - USB interface is not ready. The device drives USB with SE0.
1 - USB interface is ready. The device stops driving USB with SE0.
After power-on reset, USBRDY is cleared and the device looks like disconnected. Set USBRDY to ‘1’ to enable USB interface.

SFRAME : short frame option for test purpose
Set SFRAME to ‘1’ will shorten frame length to 1/15 ms. It is to shorten the time required for test.

PWRDN : power down mode
In suspend state, firmware can set PWRDN to put the controller into power down mode. In this mode, the embedded micro-controller and most internal activities are frozen. Hardware will automatically clear PWRDN upon hardware reset or resume activities occur.

SELF : 0 - HUB is bus powered.
1 - HUB is self powered.
GANG : 0 - HUB is in individual mode.
1 - HUB is in ganged mode.

EVTFLG (offset 01, default = 00h)

R/W1C	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*
USBRST	SOF	C_LCPWR	WAKEUP	SUSPD	EP1TX	EP0TX	EP0RX

Interrupt event flag –
EP0RX : a SETUP or OUT transaction to endpoint 0 is accepted
EP0TX : USB host controller accepts data transmitted via endpoint 0.
EP1TX : USB host controller accepts data transmitted via endpoint 1
SUSPD : the controller goes into suspend state
WAKEUP : remote wakeup is detected when global suspended
SOF : SOF detected or generated by HUB timer.
C_LCPWR : POWER source change.
USBRST : End of USB reset

RXCTL0 (offset 02, default = 40h)

R/W	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
RXDIS	RXSETUP	RXOUT	RXSEQ	RXCNT3	RXCNT2	RXCNT1	RXCNT0

Status of endpoint 0 receiving –
RXCNT3~0 : EP0 received data byte count.
RXSEQ : 1 - The received data PID is DATA1
0 - The received data PID is DATA0
RXOUT : 1 - The received token PID is OUT.
RXSETUP : 1 - The received token PID is SETUP.
RXDIS : 0 - Endpoint 0 FIFO is empty and ready for data-packet receiving.
1 - Endpoint 0 FIFO is filled with data and will reject the new-coming data packet.

If RXDIS = 1, the device will not accept an OUT transaction addressed to it, and will respond with a NAK to an error-free transaction. Hardware will automatically set RXDIS after a successful receiving. After processing, the micro-controller should clear RXDIS to enable next data-packet receiving or free FF0 for filling of the data to transmit. Note that a SETUP transaction addressed to the device is always accepted even though RXDIS = 1.

TXCTL0 (offset 03, default = 00h)

	R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
--	EP0STL	EP0OE	EP0SEQ	EP0CNT3	EP0CNT2	EP0CNT1	EP0CNT0

Endpoint 0 transmit setting –
EP0CNT3~0 : number of data bytes to transmit
EP0OE : enable data transmit
1 – ready to transmit data packet
0 – not ready to transmit data packet (default)
EP0SEQ : data packet type
0 –DATA0
1 –DATA1
EP0STL : set endpoint 0 stall
1 – EP0 will respond to USB host controller with STALL packet
EP0STL will be automatically cleared when a setup transaction is accepted.

After filling the data-to-transmit into FF0, the micro-controller should setup this register to enable endpoint 0 data transmit. If EP0OE = 0, endpoint 0 will respond to a valid IN transaction with a NAK. EP0OE will be automatically cleared after a successful transmission, or when endpoint 0 has incidentally accepted another SETUP or OUT transaction.

TXCTL1 (offset 04, default = 00h)

	R/W	*R/W*	*R/W*	*R/O*	*R/O*	*R/O*	*R/W*
--	EP1STL	EP1OE	EP1SEQ	EP1CNT3	EP1CNT2	EP1CNT1	EP1CNT0

Endpoint 1 transmit setting –
EP1CNT3~0 : number of data bytes to transmit. EP1CNT3~1 are always '0'.
EP1OE : enable data transmit
1 – ready to transmit data packet
0 – not ready to transmit data packet (default)
EP1SEQ : data packet type
0 –DATA0
1 –DATA1
EP1STL : set endpoint 1 stall
1 – EP1 will respond to USB host controller with STALL packet
0 – default

After preparing the data to transmit, the micro-controller should setup this register to enable endpoint 1 data transmit. If EP1OE = 0, endpoint 1 will respond to a valid IN transaction with a NAK. After a successful transmission, the device will automatically clear EP1OE.

FFDAT (offset 05, default = 00h)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
FFD7	FFD6	FFD5	FFD4	FFD3	FFD2	FFD1	FFD0

If FFSEL1 (in BUFCTL) = 1'b0, this is FF0 access-window; if FFSEL1 = 1'b1, this is FF1 access-window. Each FFDAT read/write will automatically increase the FIFO pointer, which is a 3-bit circular counter, by 1. Writing FPRST with '1' (in BUFCTL) will reset the pointer. Note that to fill FF0, RXDIS (in RXCTL0) must be first cleared.

BUFCTL (offset 06)

					W/O		*R/W*
--	--	--	--	--	FPRST	--	FFSEL1

Data buffer control –
FFSEL1 : FIFO 0/1 selector
1'b0 – select endpoint 0 data buffer
1'b1 – select endpoint 1 data buffer
FPRST : reset FIFO 0/1 pointer (write only)

PORTSEL (offset 07, default = 00h)

	R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
--	PORTSEL 7	PORTSEL 6	PORTSEL 5	PORTSEL 4	PORTSEL 3	PORTSEL 2	PORTSEL 1

PORTSEL : PORT 1~7 under request
PORTSEL1 1'b1 – port 1 selected
PORTSEL2 1'b1 – port 2 selected
PORTSEL3 1'b1 – port 3 selected
PORTSEL4 1'b1 – port 4 selected
PORTSEL5 1'b1 – port 4 selected
PORTSEL6 1'b1 – port 4 selected
PORTSEL7 1'b1 – port 4 selected

HUB_STAT_CHG (offset 08, default = 00h)

R/O	*R/O*					*R/O*	*R/O*
LCPWR	OVCUR	--	--	--	--	C_LCPWR	C_OVCUR

HUB status and status change
LCPWR : HUB local power status
1'b0 – local power good
1'b1 – local power lost
OVRCUR : HUB over current indicator
1'b0 – No over-current condition currently exists
1'b1 – A hub over-current condition exists
C_LCPWR : Local power status change
1'b0 – No change has occurred to local power status
1'b1 – local power status has changed
C_OVRCUR : HUB over current indicator change
1'b0 – No change has occurred to the over-current indicator
1'b1 – Hub over-current indicator has changed

PORT_STATUS (offset 09, default = 00h)

R/O	*R/O*		*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
PT_LOW_SPD	PT_PWR	--	PT_RST	PT_OVCUR	PT_SUS	PT_EN	PT_CON

Port status indicator:
PT_LOW_SPD : 1'b0 – full speed device connected, 1'b1 – low speed device connected
PT_PWR : 1'b0 – port is in power off state, 1'b1 – port is not in power off state
PT_RST : 1'b0 – Reset signaling not asserted, 1b'1 – Reset signaling asserted
PT_OVCUR : 1'b0 – No over-current condition occurred on this port
1'b1 – An over-current condition exists on this port
PT_SUS : 1'b0 – port not suspended, 1'b1 – port suspended or resuming
PT_EN : 1'b0 – port is disabled, 1'b1 – port is enabled
PT_CON : 1'b0 – No device is present, 1'b1 – A device is present on this port

BUS_PORT_DATA (offset 0A, default = 00h)

R/O	*R/O*		*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
VP	VM	--	C_PT_RST	C_PT_OVCUR	C_PT_SUS	C_PT_EN	C_PT_CON

Bus state and Port status change indicator:
VP : VP state on the downstream port
VM : VM state on the downstream port
C_PT_RST : 1'b0 – No change, 1'b1 – Reset complete
C_PT_OVCUR : 1'b0 – No change has occurred to over-current indicator
1'b1 – over-current indicator has changed
C_PT_SUS : 1'b0 – No change, 1'b1: – Resume complete
C_PT_EN : Set to one when a port is disabled because of a Port_error condition
C_PT_CON : 1'b0 – No change has occurred to current connect status
1'b1 – Current connect status has changed

HOST_CMD (offset 0B, default = 0Fh)

W/O	*W/O*	*W/O*	*W/O*	*W/O*	*W/O*	*W/O*	*W/O*
HB_CMD3	HB_CMD2	HB_CMD1	HB_CMD0	PT_CMD3	PT_CMD2	PT_CMD1	PT_CMD0

Host command to the hub:
PT_CMD3~0 : 4'h0 –SetPortFeature(PORT_SUSPEND)
: 4'h1 –SetPortFeature(PORT_RESET)
: 4'h2 –SetPortFeature(PORT_POWER)
: 4'h3 –ClearPortFeature(PORT_ENABLE)
: 4'h4 –ClearPortFeature(PORT_SUSPEND)
: 4'h5 –ClearPortFeature(PORT_POWER)
: 4'h6 –ClearPortFeature(C_PORT_RESET)
: 4'h7 –ClearPortFeature(C_PORT_OVER_CURRENT)
: 4'h8 –ClearPortFeature(C_PORT_SUSPEND)
: 4'h9 –ClearPortFeature(C_PORT_ENABLE)
: 4'hA –ClearPortFeature(C_PORT_CONNECTION)
HB_CMD3 : 1'b1 –SetHubFeature(C_HUB_LOCAL_POWER)
HB_CMD2 : 1'b1 –SetHubFeature(C_HUB_OVER_CURRENT)
HB_CMD1 : 1'b1 –ClearHubFeature(C_HUB_LOCAL_POWER)
HB_CMD0 : 1'b1 –ClearHubFeature(C_HUB_OVER_CURRENT)

ENP1_IND (offset 0C, default = 00h)

R/O	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
PT7	PT6	PT5	PT4	PT3	PT2	PT1	HUB

Endpoint 1 interrupt change indicator

TRXFLAG (offset 0D, default = 00h)

	R/W1C	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*
--	P7_TRX	P6_TRX	P5_TRX	P4_TRX	P3_TRX	P2_TRX	P1_TRX

Upstream traffic flag:
P1_TRX : upstream traffic happens on downstream port 1
P2_TRX : upstream traffic happens on downstream port 2
P3_TRX : upstream traffic happens on downstream port 3
P4_TRX : upstream traffic happens on downstream port 4
P5_TRX : upstream traffic happens on downstream port 5
P6_TRX : upstream traffic happens on downstream port 6
P7_TRX : upstream traffic happens on downstream port 7

LED_INIT (offset 0E, default = 00h)

	R/W1C	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*	*R/W1C*
--	P7_ON	P6_ON	P5_ON	P4_ON	P3_ON	P2_ON	P1_ON

LED initial flag:
P1_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P2_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P3_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P4_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P5_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P6_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.
P7_ON : if 1'b1, LED is always on, otherwise, judge according to TRXFLAG register.

GPIOD (offset 0F, default = 0Fh)

	R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
--	GPIO6D/ LED7	GPIO5D/ LED6	GPIO4D/ LED5	GPIO3D/ LED4#	GPIO2D/ LED3#	GPIO1D/ LED2#	GPIO0D/ LED1#

General purpose I/O pin status –
If GPIOXOE = 1 (X: 0 ~ 6), GPIOX is driven with the level of internal GPIOXD latch, which is the same as corresponding GPIOXD bit. If GPIOXOE = 0, GPIOXD reflects the level of GPIOX pin, which may be different from internal GPIOXD latch. The value written to GPIOD will be stored in an internal latch, no matter what direction the GPIOX pins are in. Bits 6 to 0 have been pre-assigned specific functions for LED indicators. (active low).

REV (offset 10, default = current revision)

R/O	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0

This register returns current silicon revision number of the HUB.
Current revision is 8'h11. (Revision 1.1)

DEVSTUS (offset 11, default = 00h)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
HCONFIG	DEVADR6	DEVADR5	DEVADR4	DEVADR3	DEVADR2	DEVA DR1	DEVADR0

USB device status registers. Procedure to set the device address:

1. After USB reset, the device responds to default address 0, and hub configuration = 0.
2. USB host controller issues SET_ADDRESS request to the device. (INTRB asserted)
3. Micro-controller recognizes the request, then set DEVADR register with appropriate value.
4. Micro-controller prepares the status stage of SET_ADDRESS request by programming TXCTL0 register.
5. When the hub configuration value is not equal zero, HCONFIG is set to one.

USB reset will clear this register.

6 MAXIMUM RATINGS

Maximum ratings are the extreme limits to which the GL652USB can be exposed without permanently damaging it. The GL652USB contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Keep V_{IN} and V_{OUT} within the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Connect unused inputs to the appropriate voltage level, either GND or V_{DD}.

Symbol	Characteristic	Value	Unit
T_{STG}	Storage temperature	-55 to +150	°C
T_{OP}	Operating temperature	0 to +70	°C
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	DC input voltage	-0.5 to +V_{DD} + 0.5	V
I	Maximum current per pin excluding V_{DD} and V_{SS}	25	mA
I_{MGND}	Maximum current out of GND	100	mA
I_{MVCC}	Maximum current out of V_{CC}	100	mA
V_{ESD}	Static discharge voltage	>4000	V

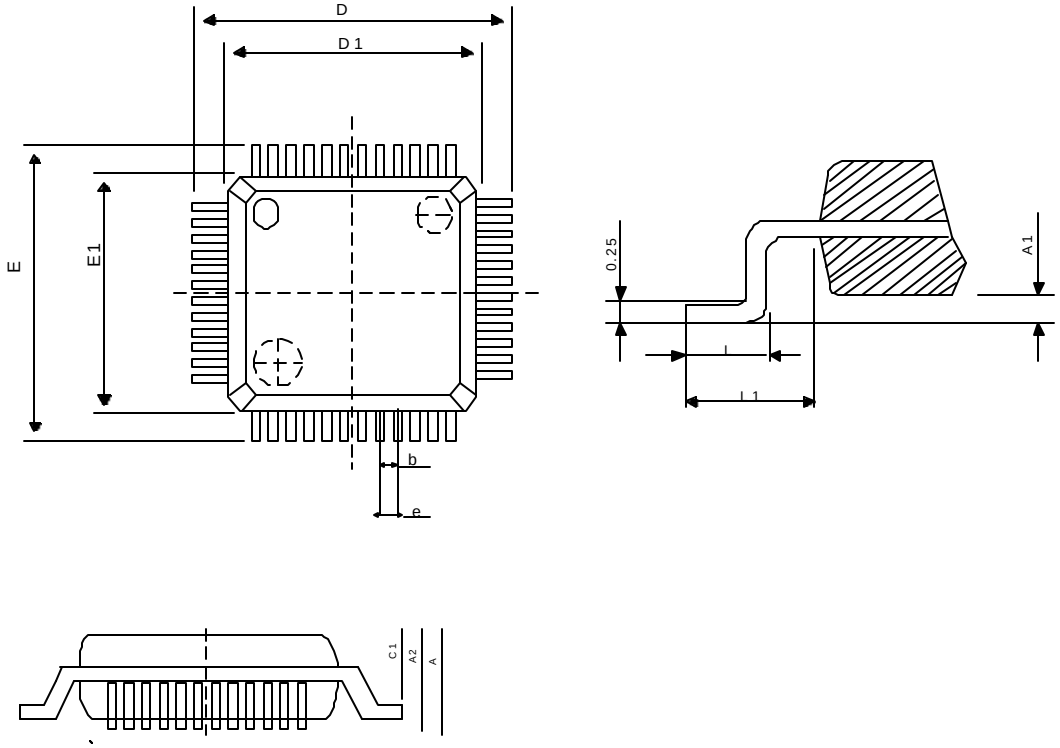
7 ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Tese Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Digital Power Supply		4.5	5.0	5.5	V
V_{DDA}	Analog Power Supply		4.5	5.0	5.5	V
I_{DD}	Digital Supply Current					mA
I_{DDA}	Analog Supply Current					mA
USB Bus: DP and DM						
V_{CP}	Regulated Voltage Output		3.0	3.3	3.6	V
V_{DI}	Static Input Voltage		0	-	V_{CP}	V
V_{DO}	Static Output Voltage		0	-	V_{CP}	V
Digital I/O Pins						
V_{IL}	Input Logic Low Voltage		-	-	0.8	V
V_{IH}	Input Logic High Voltage		2.0	-	-	V
V_{OL}	Output Logic Low Voltage	I_O=-4.0mA	-	-	0.1xV_{DD}	V
V_{OH}	Output Logic High Voltage	I_O=+4.0mA	0.9xV_{DD}	-	-	V

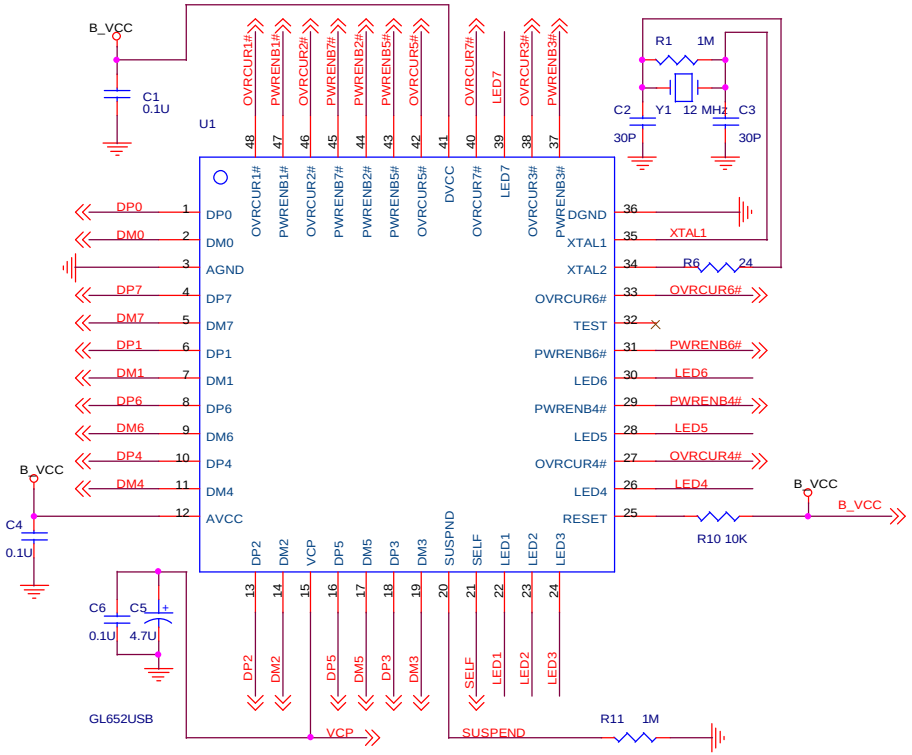
8 PACKAGE DIAGRAM

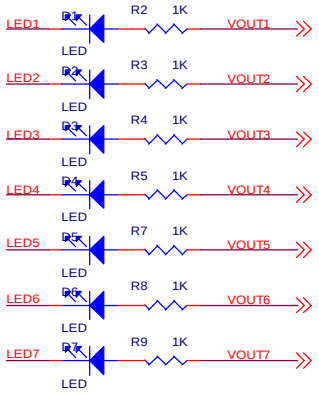
48-LQFP

SYVBOIS	MIN	MAX
A		1.6
A1	0.05	0.15
A2	1.35	1.45
C1	0.09	0.16
D	9.00BSC	
D1	7.00BSC	
E	9.00BSC	
E1	7.00BSC	
e	0.5BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	



9. Application Circuits (1)





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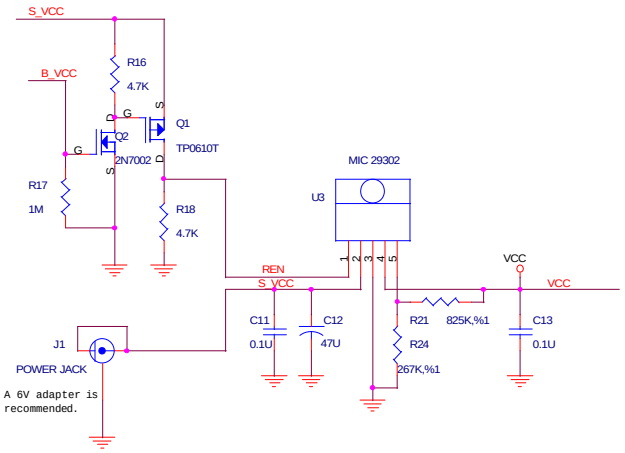
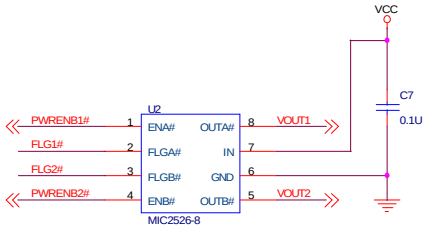
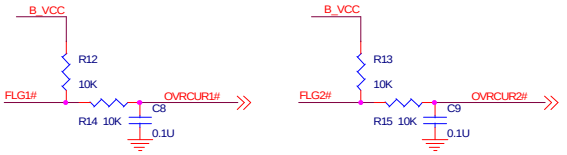
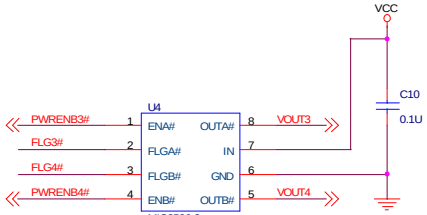
Date: Thursday, August 17, 2000	Sheet 1 of 4	

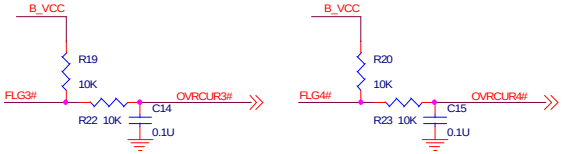
9. Application Circuits (2)

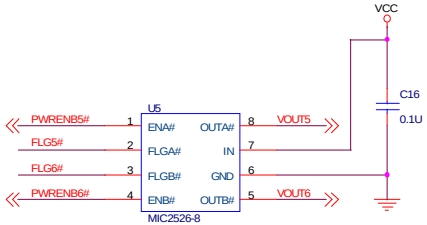


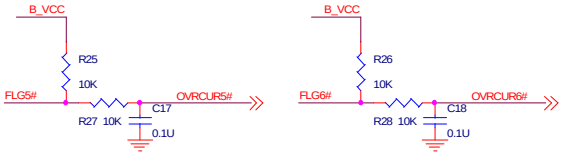


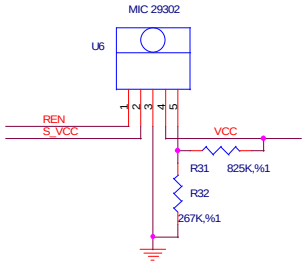


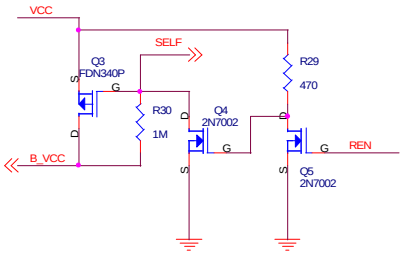


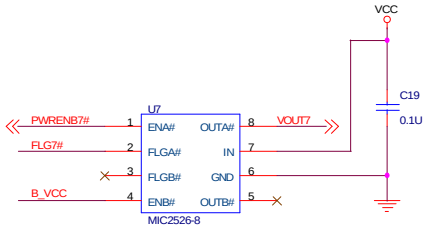


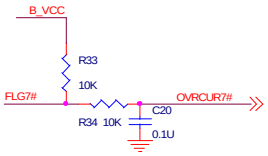












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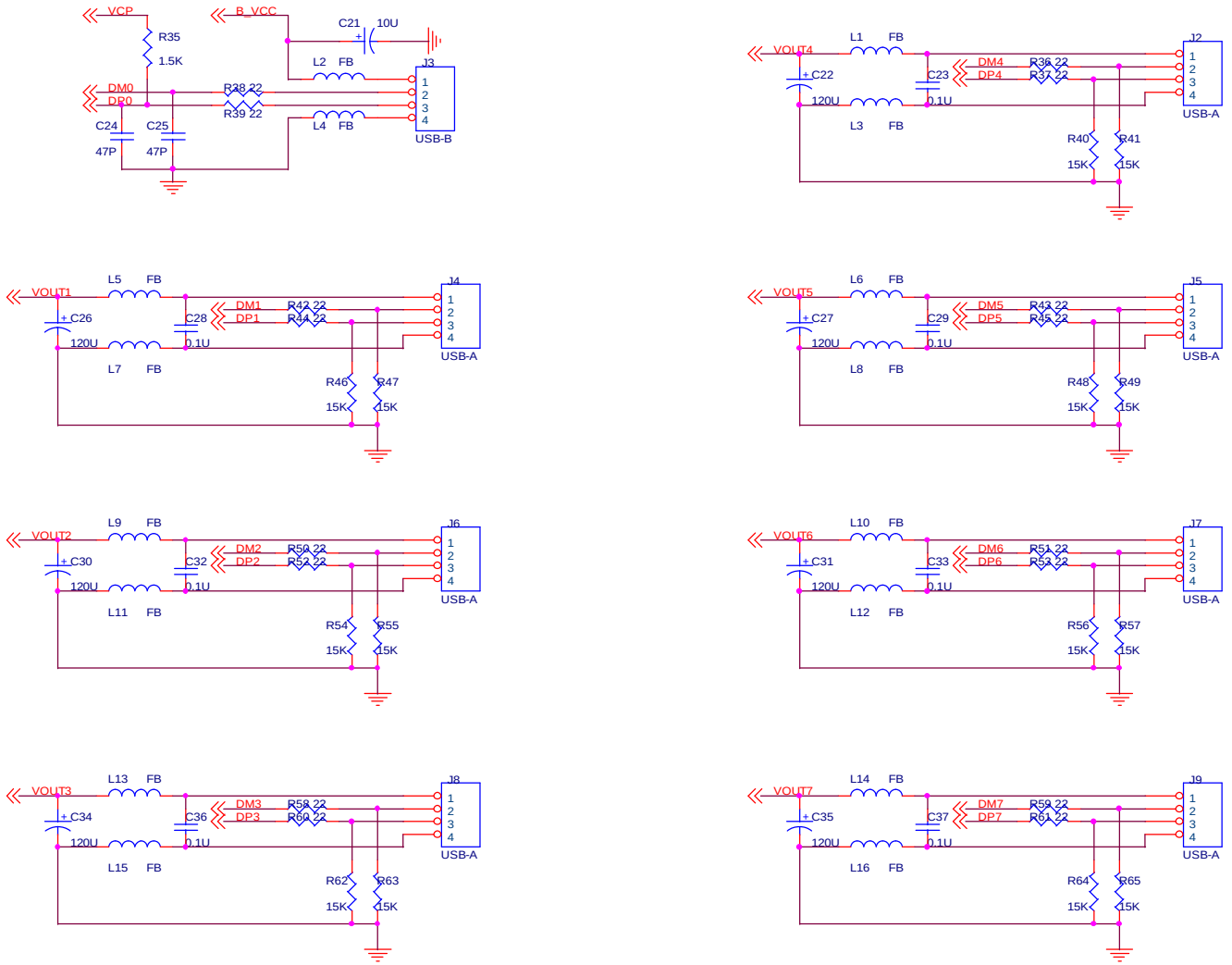
9. Application Circuits (3)



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9. Application Circuits (4)

Rev.	Description	Date
1.0	1. First Product Release	'00/04/05
1.1	1. Seperate 4-port and 7-port hubs into different schematic files. 2. Omit the ganged mode pull-up resistor on 'SUSPND' pin. 3. Add a 10K pull-up resistor to 'RESET' pin. 4. Connect pin 1 of U3 to B_VCC, then regulator will be enabled only when upstream port is plugged! A 1M pull-low resistor is also added to disable this pin when the upstream port is not plugged. 5. 'SELF' is directly connected to drain of Q4 to omit the external debounce RC circuit for this pin. 6. Q1 is replaced by a more popular and cheaper one -- FDN340P. 7. Some resistor values are increased to save the operating current.	'00/05/18
1.2	1. Change the pull-up voltage source for each LED from B_VCC to power switch output. 2. Remove the 47U output capacitor of MIC29302 to suppress inrush current. 3. Add R1, R6 and C6 for EMI suppressing. 4. Change C22, C26, C27, C30, C31, C34 and C35 from 100U to 120U for better behavior in droop test. 5. Add a 2-transistor circuit for regulator ENABLE pin. That will save several tens of mA operating current than direct connecting B_VCC to ENABLE pin. 6. Remove a redudant transistor in SELF-BUS power switching circuit. 7. Change MIC29512 to 2 paralell MIC29302 for better driving capability.	'00/08/17

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