

### Features

- broadcast quality 10 / 8-bit 24-tap poly-phase horizontal and vertical scalar for HDTV / SDTV video images
- high performance 2D scaling processor with separate control of horizontal and vertical scaling factors and pan positions
- support for arbitrary video formats up to 2048 by 2048
- support for multiplexed and non-multiplexed Y/C video
- flexible 4:2:2 or 4:4:4 YCbCr or RGB output
- field merge / separation can be inserted / removed from progressive images using interlaced I/O
- double banked control registers for 'on-the-fly' dynamic effects
- external 3:2 / 2:2 pull-down insertion and extraction
- programmable output matrix with 6dB gain range
- film rate features include 1080p24 and 1080PsF support
- fully programmable colour background generator
- flexible F,V,H output and TRS insertion
- seamless interface to GF9330 de-interlacer
- seamless interface to common SDRAM
- user configuration through dedicated serial interface
- 3.3V supply

### Description

The GF9320 Scaling Processor offers 10 / 8-bit broadcast quality scaling of video images up to 2048 by 2048 pixels. The GF9320 supports arbitrary display modes to fit custom applications. Dynamic zoom and pan effects allow for a variety of aspect ratio conversion

choices while a programmable colour background generator can be customized to appropriately match the image content. A fully programmable and flexible output matrix allows for colour difference over-sampling, gain and hue controls as well as YCbCr to RGB conversions to power nearly any display device on the market.

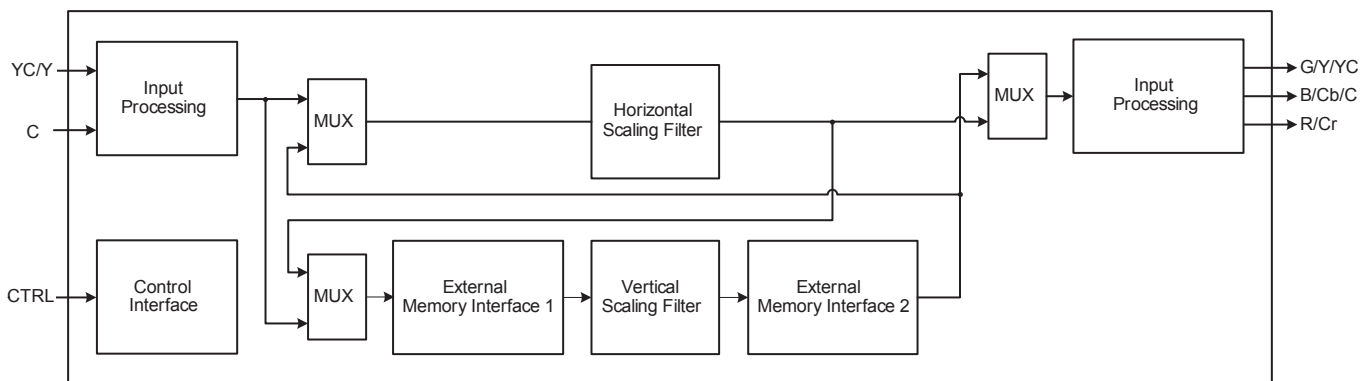
The GF9320 also includes a vertical interpolation filter to perform stand alone cost-sensitive de-interlacing. Broadcast quality de-interlacing is offered through a seamless interface to the GF9330 and GF9331 devices.

### Applications

- HDTV Up / Down Converters
- Production Equipment
- Video Walls
- Projection Systems
- Plasma Displays
- LCD TVs
- Home Theatre Systems
- HD DVD Players

### Ordering Information

Part Number	Package	Temp. Range
GF9320-CBW	352 pin TBGA	0°C to 70°C



**Block Diagram**



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# 1. Pin Description

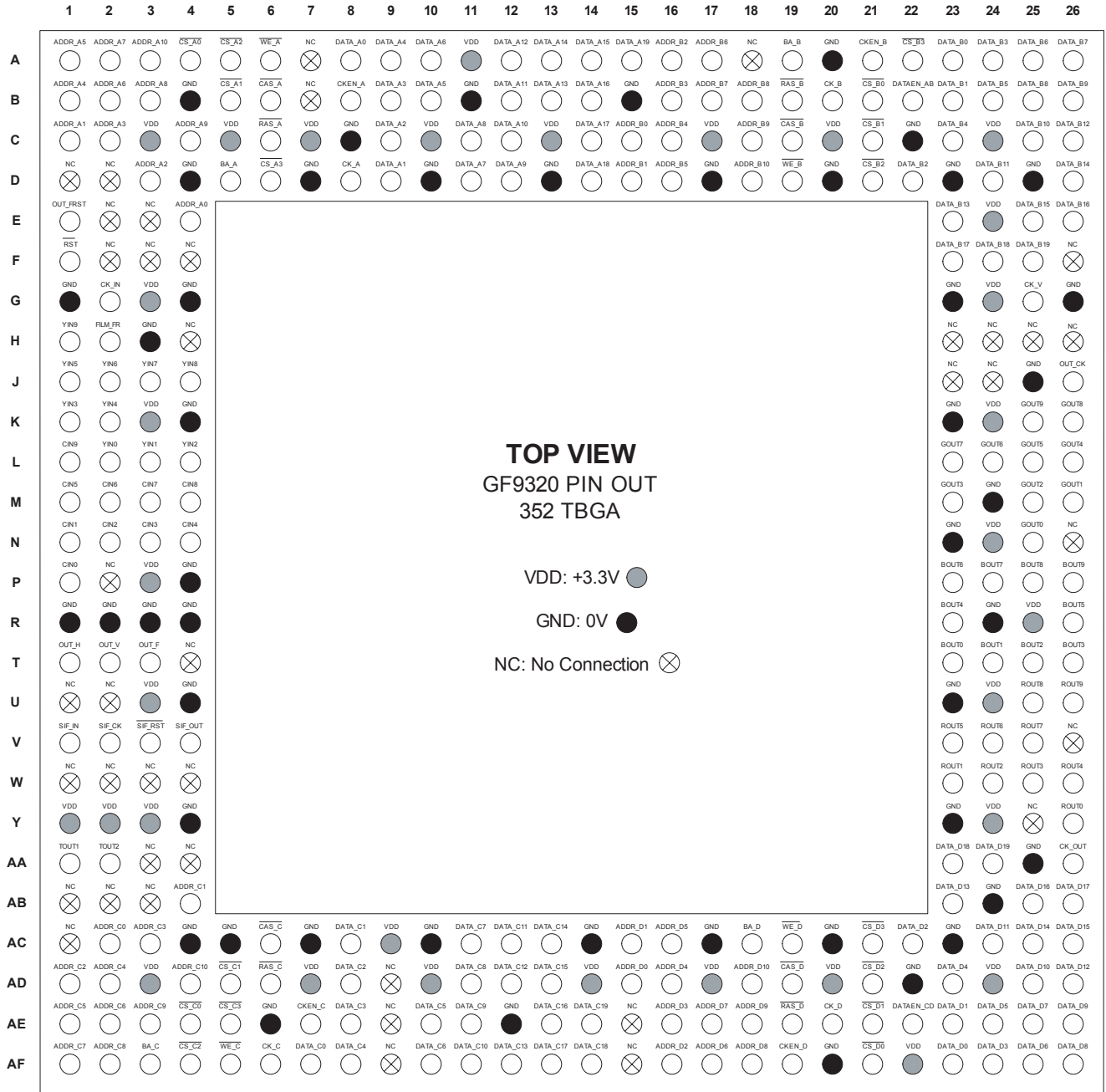


Figure 1-1: GF9320 Pin Out



Table 1-1: Pin Descriptions

Symbol	Pin Grid	Type	Description
YIN[9:0]	H1, J4, J3, J2, J1, K2, K1, L4, L3, L2	I	10-bit multiplexed signed luminance / signed offset colour difference data input. Note that either input must include TRS words.
CIN[9:0]	L1, M4, M3, M2, M1, N4, N3, N2, N1, P1	I	10-bit signed offset colour difference data input. Note that the input must include TRS words.
CK_IN	G2	I	Input clock. Note that it is equal Y data rate for separate Y and C inputs, and is equal to 2x Y data rate for multiplexed YC input.
CK_V	G25	I	Vertical processing clock. Note that it is usually the higher of CK_IN or CK_OUT.
CK_OUT	AA26	I	Output clock.
FILM_FR	H2	I	Input film sequence reset.
OUT_FRST	E1	I	Output frame reset.
GOUT[9:0]	K25, K26, L23, L24, L25, L26, M23, M25, M26, N25	O	10 / 8-bit unsigned green data output OR 10 / 8-bit unsigned luminance data output OR 10 / 8-bit multiplexed signed luminance / signed offset colour difference data output.
BOUT[9:0]	P26, P25, P24, P23, R26, R23, T26, T25, T24, T23	O	10 / 8-bit unsigned blue data output OR 10 / 8-bit signed offset (B-Y) data output OR 10/8-bit multiplexed signed offset colour difference data output.
ROUT[9:0]	U26, U25, V25, V24, V23, W26, W25, W24, W23, Y26	O	10 / 8-bit unsigned red data output OR 10 / 8-bit signed offset (R-Y) data output.
OUT_CK	J26	O	Output clock timed to clock output data.
OUT_F	T3	O	Output format frame / field signal. Note that the output is 3 clocks in advance of output video data.
OUT_V	T2	O	Output format vertical signal. Note that the output is 3 clocks in advance of output video data.
OUT_H	T1	O	Output format horizontal signal. Note that the output is 3 clocks in advance of output video data.
SIF_OUT	V4	O	Serial interface control data out.
SIF_IN	V1	I	Serial interface control data in.
SIF_CK	V2	I	Serial interface clock.
SIF_RST	V3	I	Serial interface reset.
RST	F1	I	Power-on reset.
DATA_A[19:0]	A15, D14, C14, B14, A14, A13, B13, A12, B12, C12, D12, C11, D11, A10, B10, A9, B9, C9, D9, A8	I/O	Data bus for memory array A.

**Table 1-1: Pin Descriptions (Continued)**

Symbol	Pin Grid	Type	Description
DATA_B[19:0]	F25, F24, F23, E26, E25, D26, E23, C26, D24, C25, B26, B25, A26, A25, B24, C23, A24, D22, B23, A23	I/O	Data bus for memory array B.
DATA_C[19:0]	AE14, AF14, AF13, AE13, AD13, AC13, AF12, AD12, AC12, AF11, AE11, AD11, AC11, AF10, AE10, AF8, AE8, AD8, AC8, AF7	I/O	Data bus for memory array C.
DATA_D[19:0]	AA24, AA23, AB26, AB25, AC26, AC25, AB23, AD26, AC24, AD25, AE26, AF26, AE25, AF25, AE24, AD23, AF24, AC22, AE23, AF23	I/O	Data bus for memory array D.
ADDR_A[10:0]	A3, C4, B3, A2, B2, A1, B1, C2, D3, C1, E4	O	Address bus for memory array A.
BA_A	D5	O	SDRAM bank select for memory array A.
ADDR_B[10:0]	D18, C18, B18, B17, A17, D16, C16, B16, A16, D15, C15	O	Address bus for memory array B.
BA_B	A19	O	SDRAM bank select pin for memory array B.
ADDR_C[10:0]	AD4, AE3, AF2, AF1, AE2, AE1, AD2, AC3, AD1, AB4, AC2	O	Address bus for memory array C.
BA_C	AF3	O	SDRAM bank select pin for memory array C.
ADDR_D[10:0]	AD18, AE18, AF18, AE17, AF17, AC16, AD16, AE16, AF16, AC15, AD15	O	Address bus for memory array D.
BA_D	AC18	O	SDRAM bank select pin for memory array D.
$\overline{\text{CS}}_A[3:0]$	D6, A5, B5, A4	O	Chip select for memory array A.
$\overline{\text{CS}}_B[3:0]$	A22, D21, C21, B21	O	Chip select for memory array B.
$\overline{\text{CS}}_C[3:0]$	AE5, AF4, AD5, AE4	O	Chip select for memory array C.
$\overline{\text{CS}}_D[3:0]$	AC21, AD21, AE21, AF21	O	Chip select for memory array D.
$\overline{\text{RAS}}_A$	C6	O	Row address strobe for memory array A.
$\overline{\text{RAS}}_B$	B19	O	Row address strobe for memory array B.
$\overline{\text{RAS}}_C$	AD6	O	Row address strobe for memory array C.
$\overline{\text{RAS}}_D$	AE19	O	Row address strobe for memory array D.
$\overline{\text{CAS}}_A$	B6	O	Column address strobe for memory array A.
$\overline{\text{CAS}}_B$	C19	O	Column address strobe for memory array B.
$\overline{\text{CAS}}_C$	AC6	O	Column address strobe for memory array C.



Table 1-1: Pin Descriptions (Continued)

Symbol	Pin Grid	Type	Description
$\overline{\text{CAS\_D}}$	AD19	O	Column address strobe for memory array D.
$\overline{\text{WE\_A}}$	A6	O	Write enable for memory array A.
$\overline{\text{WE\_B}}$	D19	O	Write enable for memory array B.
$\overline{\text{WE\_C}}$	AF5	O	Write enable for memory array C.
$\overline{\text{WE\_D}}$	AC19	O	Write enable for memory array D.
CK_A	D8	O	Clock for memory array A.
CK_B	B20	O	Clock for memory array B.
CK_C	AF6	O	Clock for memory array C.
CK_D	AE20	O	Clock for memory array D.
CKEN_A	B8	O	Clock enable for memory array A.
CKEN_B	A21	O	Clock enable for memory array B.
CKEN_C	AE7	O	Clock enable for memory array C.
CKEN_D	AF19	O	Clock enable for memory array D.
DATAEN_AB	B22	O	Data enable for memory arrays A and B.
DATAEN_CD	AE22	O	Data enable for memory arrays C and D.
VDD	K3, C10, A11, P3, C13, U3, C17, Y3, C20, AD3, G3, AD7, AC9, AD10, AD14, AD17, C24, AD20, AF22, AD24, E24, Y24, G24, K24, C5, N24, C3, U24, R25, C7, Y1, Y2	I	3.3V supply.
GND	R24, U23, N23, K23, G26, G23, Y23, D25, AC20, AF20, AC17, D23, AC14, AC10, AC7, AC5, AC4, D20, A20, Y4, D17, B15, U4, D13, P4, B11, D10, K4, D7, G4, B4, D4, AC23, C8, H3, J25, AE6, C22, AE12, M24, AD22, G1, AB24, AA25, R1, R2, R3, R4	I	Device ground.
NC	H26, W2, W3, J23, W4, T4, U1, U2, J24, A7, A18, AA3, AA4, W1, AB1, AB2, F26, AC1, AB3, N26, Y25, F2, V26, F3, P2, B7, D2, AD9, E3, H24, AE9, D1, AF9, E2, AE15, AF15, F4, H23, H25, H4, AA1, AA2		No connection.



## 2. Electrical Characteristics

**Table 2-1: Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Rated Value	Units
Power Supply Voltage	$V_{DD}$		-0.5 to +4.6	V
Input Voltage	$V_I$	$V_I < V_{DD} + 0.5\text{ V}$	-0.5 to +4.6	V
Output Voltage	$V_O$	$V_O < V_{DD} + 0.5\text{ V}$	-0.5 to +4.6	V
Output Current	$I_O$		40	mA
Operating Temperature	$T_A$		0 to +70	°C
Storage Temperature	$T_{STG}$		-65 to +150	°C

**Table 2-2: Recommend Operating Conditions**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	$V_{DD}$		3.0	3.3	3.6	V
High-Level Input Voltage	$V_{IH}$	TTL Interface	2.0	-	$V_{DD}$	V
Low-Level Input Voltage	$V_{IL}$	TTL Interface	0.0	-	0.8	V
Positive Trigger Voltage	$V_P$		1.5	-	2.7	V
Negative Trigger Voltage	$V_N$		0.6	-	1.4	V
Hysteresis Voltage	$V_H$		1.1	-	1.5	V
Input Rise Time	$t_{ri}$	Normal Input	0	-	200	ns
Input Fall Time	$t_{fi}$	Normal Input	0	-	200	ns



Table 2-3: DC Characteristics

<b>V<sub>DD</sub> = 3.0 to 3.6V, T<sub>A</sub> = 0 to 70°C, unless otherwise shown</b>						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Static Current Consumption	I <sub>DDs</sub>	V <sub>I</sub> = V <sub>DD</sub> or GND		10	200	μA
Input Leakage Current	I <sub>I</sub>	V <sub>I</sub> = V <sub>DD</sub> or GND		±10 <sup>-4</sup>	±10	μA
Low-Level Output Current	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V	12.0	-	-	mA
High-Level Output Current	I <sub>OH</sub>	V <sub>OH</sub> = 2.4V	-2.0	-	-	mA
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0 mA	-	-	0.1	V
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = 0 mA	V <sub>DD</sub> - 0.1	-	-	V
Off-State Output Current	I <sub>OZ</sub>	V <sub>O</sub> = V <sub>DD</sub> or GND	-	-	±10	μA
Output Short-Circuit Current	I <sub>OS</sub>	V <sub>O</sub> = GND	-	-	-250	mA

Table 2-4: Capacitance

<b>T<sub>A</sub> = 25°C; f = 1MHz</b>						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Capacitance	C <sub>I</sub>		4.0	-	6.4	pF
Output Capacitance	C <sub>O</sub>		4.0	-	6.0	pF
I/O Capacitance	C <sub>IO</sub>		4.0	-	6.0	pF

Table 2-5: Operating Current

<b>V<sub>DD</sub> = 3.0 to 3.6V, T<sub>A</sub> = 0 to 70°C, unless otherwise shown</b>						
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Current	I <sub>CC</sub>	CK_IN @ 90MHz CK_OUT @ 90MHz CK_V @ 88MHz	-	-	910	mA





Table 2-6: AC Characteristics - Setup &amp; Hold Times

<b>V<sub>DD</sub> = 3.0 to 3.6V, T<sub>A</sub> = 0 to 70°C, unless otherwise shown</b>						
Signal Name	Setup		Hold		Reference Clock	Units
	Min.	Max.	Min.	Max.		
YIN[9:0]	2	-	1	-	CK_IN	ns
CIN[9:0]	2	-	1	-	CK_IN	ns
FILM_FR	-	-	2	-	CK_IN	ns
SIF_IN	1	-	2	-	SIF_CK	ns
SIF_RST	1	-	2	-	SIF_CK	ns
OUT_FRST	1	-	2	-	CK_OUT	ns
DATA_A	2	-	0	-	CK_A	ns
DATA_B	2	-	0	-	CK_B	ns
DATA_C	2	-	0	-	CK_C	ns
DATA_D	2	-	0	-	CK_D	ns

Table 2-7: AC Characteristics - Pulse Signal

<b>V<sub>DD</sub> = 3.0 to 3.6V, T<sub>A</sub> = 0 to 70°C, unless otherwise shown</b>			
Signal Name	Pulse Width		Units
	Min.	Max.	
$\overline{\text{RST}}$	110 <sup>a</sup>		μs

a. The minimum pulse width is for 64Mb SDRAMs. If 16Mb is used then 10μs width can be used.

**Table 2-8: Output Signal Timing Specifications**

Signal Name	CLK to Valid Output Delay		Reference Clock
	Min. (ns)	Max. (ns)	
OUT_CK	1.81	3.97	CK_OUT
GOUT[9:0]	0.15	3	OUT_CK
BOUT[9:0]	0.15	3	OUT_CK
ROUT[9:0]	0.15	3	OUT_CK
ADDR_A, $\overline{\text{RAS}}_A$ , $\overline{\text{CAS}}_A$ , $\overline{\text{WE}}_A$ , CKEN_A, DATA_A	1.25	6	CK_A
ADDR_B, $\overline{\text{RAS}}_B$ , $\overline{\text{CAS}}_B$ , $\overline{\text{WE}}_B$ , CKEN_B, DATA_B	1.25	6	CK_B
ADDR_C, $\overline{\text{RAS}}_C$ , $\overline{\text{CAS}}_C$ , $\overline{\text{WE}}_C$ , CKEN_C, DATA_C	1.25	6	CK_C
ADDR_D, $\overline{\text{RAS}}_D$ , $\overline{\text{CAS}}_D$ , $\overline{\text{WE}}_D$ , CKEN_D, DATA_D	1.25	6	CK_D

**Table 2-9: Clock Frequency**

Clock Name	Frequency	
	Min. (MHz)	Max. (MHz)
CK_IN	1	90
CK_V	1	88
CK_OUT	1	90
SIF_CK	-	90



## 3. Detailed Device Description

### 3.1 Device Overview

A system level block diagram is shown in the “[Block Diagram](#)” on page 1.

2D scaling is performed by cascading two 1D-scaling filters.

If the number of horizontal input samples is greater than the number of horizontal output samples (i.e. down sampling), then it is advantageous to perform horizontal resizing first. Otherwise, horizontal resizing is performed last. This minimizes the number of operations required, reduces the intermediate image size and thus lowers the SDRAM requirements.

In addition, the SDRAMs are used for field merge or separation operations to perform simple frame rate conversions (e.g. 30 ↔ 60 and 48 ↔ 60) for film applications. This minimizes the on chip memory required to perform 2D format conversion for low-cost, high-quality format conversion.

The GF9320 has 2 fields / frames of delay depending on the selected operating mode.

Processing is performed simultaneously on 3 fields / frames. Input processing is performed on field / frame N, vertical processing is performed on field / frame (N-1) and output processing is performed on field / frame (N-2).

The input processor decodes the input TRS to determine input video timing information. An area of the input video is selected according to the downloaded parameters. The input video is resized horizontally if down sampling is indicated.

The video is passed to picture memory control #1 and stored in SDRAM. Field / frame (N-1) is read out of picture memory #1, processed vertically, and stored in picture memory #2. To process the video vertically the read address to picture memory #1 transposes the video data while the write address to picture memory #2 transposes the video data back. This transpose operation allows the vertical processing to be done as rows instead of columns.

Field / frame (N-2) is read out of picture memory #2 and resized horizontally if up sampling is indicated.

The flexible output processor can be selected to perform 4:2:2 to 4:4:4 colour difference over sampling, YCbCr to RGB conversion, colour background insertion and output TRS insertion.



## 3.2 Serial Interface Control

The serial interface download control parameters are grouped into 5 sets as given in [Table 3-1: Serial Interface Download Groups](#). All parameters may be downloaded at once or each set can be downloaded individually. This grouping allows for quick downloading of dynamic parameters (e.g. zoom, pan, gain, etc.) and only requires that the static parameters be downloaded once. Details of individual control parameters are provided in [Table 3-2: Serial Interface Download Parameters](#).

**Table 3-1: Serial Interface Download Groups**

Name	CMD ID	No. of Bytes	Number of Bits	Description	Word
All Parameters <sup>a</sup>	0 00000000 <sup>b</sup>	147	1176	A download of all parameters.	AP[1175:0]
I/O Format Parameters	1 00100000 <sup>b</sup>	11	7 + 14 + 66 + 1 (fill) = 88	Input and static output parameters. These parameters tend to remain fixed once the input and output format is selected.	IO[87:0]
Scaling Parameters	2 01000000 <sup>b</sup>	19	149 + 3 (fill) = 152	Resizing parameters. These parameters change with zoom, pan, and crop controls.	RS[151:0]
Dynamic Output Parameters	3 01100000 <sup>b</sup>	20	157 + 3 (fill) = 160	Dynamic output parameters. These parameters change with gain, H position, line advance, etc...	OD[159:0]
Horizontal Filter Coefficients	4 10000000 <sup>b</sup>	43	344 + 0 (fill) = 344	Horizontal filter.	HF[343:0]
Vertical Filter Coefficients	5 10100000 <sup>b</sup>	54	428 + 4 (fill) = 432	Vertical filter.	VF[431:0]

a. The GF9320 download parameters are grouped into 5 sets.

b. Each group will be extended with zeros to make an integer number of bytes. In each group the LSB is sent first. So, for instance, the I/O format parameter group sends 1 zero followed by the PROC\_8\_BITS bit followed by the OUT\_8\_BITS bit. A download of all parameters (CMD ID = 0) sends the word:

AP[1175:0] = IO[87:0] | RS[151:0] | OD[159:0] | HF[343:0] | VF[431:0]

where "|" represents concatenation.

As with all other words the LSB of AP[1175:0] is sent first. The CMD\_ID word is listed above in binary form from MSB to LSB. As with all other words the CMD\_ID is sent LSB first. For example, a download of the dynamic output parameters (CMD\_ID=3) sends 5 zeros followed by 2 ones followed by 1 zero followed by OD0 followed by OD1 followed by OD2....OD159.

Note that all CMD\_IDs have 5 zeros as the 5 least significant bits so that each download command starts with 5 zeros.

**Table 3-2: Serial Interface Download Parameters**

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
I/O Format Parameters	88 Total				
Input Format Parameters	7 Sub-total				
IN_PROGRESSIVE	1	Indicates that the input is progressive. 0 - Interlaced 1 - Progressive	IO[87]	Input Control	0
IN_TOP_ACT_FLD	1	Used for interlaced formats only. Indicates which field contains the first active line in a frame. (i.e. which field is on top) 0 - Field 0 is on top 1 - Field 1 is on top	IO[86]	Input Control	0
IN_TOP_ACT_LONGER	1	Used for interlaced formats only. Indicates if the top field is one line longer than the bottom field. 0 - Top and Bottom fields contain the same number of active lines 1 - Top field has one more active line	IO[85]	Input Control	0
IN_YC_MUXED	1	Indicates if the input bus is one 10-bit bus for muxed Y&C data. 0 - Two 10-bit buses for Y and C <sub>b</sub> C <sub>r</sub> 1 - Y & C Muxed data on a 10-bit bus	IO[84]	Input Control	0
IN_FILM_RATE	2	Input film frame rate. Used for film inputs only. 00 - Input is from film with 3:2 pull-down 01 - Input is from film with 2:2 pull-down 10 - Input is at film rate (24/25 Hz) 11 - Not from film	IO[83:82]	Input Control	0
IN_REFR_LEFT	1	This indicates a left memory array refresh is required and normally indicates that the input is from film. 0 - No refresh 1 - Refresh	IO[81]	Memory Control	0



Table 3-2: Serial Interface Download Parameters (Continued)

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
Memory Configuration	14 Sub-total				
MEM_CONFIG_LEFT	2	Indicates the number of SDRAMs per array in the left bank excluding chips needed for LSBs if necessary. (i.e. 8-bit processing) 00 - 4 chips 01 - 3 chips 10 - 2 chips 11 - 1 chip	IO[80:79]	Memory Control	0
MODE_16_LEFT	1	Maximum number of left bank SDRAM memory rows used to store a horizontal active line. 0 - 8 memory rows 1 - 16 memory rows	IO[78]	Memory Control	0
MEM_CONFIG_RIGHT	2	Indicates the number of SDRAMs per array in the right bank excluding chips needed for LSBs if necessary. (i.e. 8 bit processing) 00 - 4 chips 01 - 3 chips 10 - 2 chips 11 - 1 chip	IO[77:76]	Memory Control	0
MODE_16_RIGHT	1	Maximum number of right bank SDRAM memory rows used to store a horizontal active line. 0 - 8 memory rows 1 - 16 memory rows	IO[75]	Memory Control	0
PIX2READ	7	Number of pixels to be pre-read. Vertical processing requires pre-reading samples so that no hits occur while processing a column of data.	IO[74:68]	Memory Control	0
OUT_REFR_RIGHT	1	This indicates a right memory array refresh is required and normally indicates that the input is from film. 0 - No refresh 1 - Refresh	IO[67]	Memory Control	0



Table 3-2: Serial Interface Download Parameters (Continued)

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
Static Output Format Parameters		67 Sub-total			
OUT_HLEN_TOT	12	The total number of samples per line. (e.g. 2200)	IO[66:55]	Output Timing	0
OUT_VLEN_TOT	12	The total number of output lines in a frame. (e.g. 1125)	IO[54:43]	Output Timing	0
OUT_HLEN_ACT	11	The number of active samples per line minus 1. (e.g. 1919 implies 1920 active samples)	IO[42:32]	Output Timing	0
OUT_VLEN_ACT	11	The number of active output lines minus 1. (e.g. 1079 implies 1080 active lines)	IO[31:21]	Output Timing	0
OUT_PROGRESSIVE	1	Indicates that the output is progressive. 0 - Interlaced 1 - Progressive	IO[20]	Output Timing / Input Control	0
OUT_TOP_ACT_FLD	1	Used for interlaced formats only. Indicates which field contains the first active line in a frame. (i.e. which field is on top) 0 - Field 0 is on top 1 - Field 1 is on top	IO[19]	Output Timing	0
OUT_TOP_ACT_LONGER	1	Used for interlaced formats only. Indicates if the top field is one line longer than the bottom field. 0 - Both fields have the same number of active lines 1 - Top field has one more active line	IO[18]	Output Timing	0
OUT_VACT_POS	8	The position of the first active output line relative to the start of the frame. For interlaced inputs this implies field 0.	IO[17:10]	Output Timing	0
OUT_FLD_LONGER	1	Used for interlaced formats only. Indicates which field is longer. Interlaced formats contain an odd number of lines. So one field contains more lines. 0 - Field 0 is longer 1 - Field 1 is longer	IO[9]	Output Timing	0
OUT_REF	1	0 - Input TRS 1 - Output Reset pin on GF9320 (OUT_FRST)	IO[8]	Output Timing	0



Table 3-2: Serial Interface Download Parameters (Continued)

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
OUT_FILM_RATE	2	Output film frame rate. 00 - Output has a 3:2 pull-down sequence 01 - Output has a 2:2 pull-down sequence 10 - Output is at a film rate (24/25 Hz) 11 - Output is not to a film rate or sequence	IO[7:6]	Output Timing / Input Control	0
OUT_MODE	2	Indicates output port configuration. 00 - 4:4:4 GBR Triple output 01 - 4:4:4 YC <sub>b</sub> C <sub>r</sub> Triple output 10 - 4:2:2 YC <sub>b</sub> C <sub>r</sub> Muxed single output 11 - 4:2:2 YC <sub>b</sub> C <sub>r</sub> Muxed dual output	IO[5:4]	Output	0
OUT_TRS_ON	1	Indicates if TRS is inserted into the output. 0 - TRS not inserted 1 - TRS inserted	IO[3]	Output	0
OUT_8_BITS	1	Indicates that the output is rounded to 8 bits. 0 - 10-bit output 1 - 8-bit output	IO[2]	Output	0
PROC_8_BITS	1	Indicates that H&V processing is rounded to 8-bits. 0 - 10-bit processing (Requires LSB memory) 1 - 8-bit processing	IO[1]	Int. Filters	0
IO_FILL	1	Not used.	IO[0]		





**Table 3-2: Serial Interface Download Parameters (Continued)**

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
Resizing Parameters		152 Total			
H_PROC_FIRST	1	Indicates horizontal processing is performed first. 0 - Horizontal processing last (H_ZOOM_RATIO < 524288) 1 - Horizontal processing first (H_ZOOM_RATIO >= 524288)	RS[151]	Glue Logic (Mux) / Mem Control	1 2
H_FLT_DEC	1	Horizontal filter decimate. 0 - Non-decimate mode 1 - Decimate mode	RS[150]	H Control / HBL Filter	1/3 1/3
H_ZOOM_RATIO	22	Horizontal zoom ratio.  $\frac{IN\_HLIVE \cdot 524288}{OUT\_HLIVE}$ if H_FLT_DEC = 0 $\frac{IN\_HLIVE \cdot 524288}{OUT\_HLIVE \cdot 2}$ if H_FLT_DEC = 1	RS[149:128]	H Control	1/3
IN_HSTART_PHASE	7	Indicates the starting horizontal phase to be used for resampling.	RS[127:121]	H Control	1/3
IN_HSTART	11	Indicates the first sample to be used for resampling.	RS[120:110]	Input Timing / H Control / Mem Control	1 1/3 2
IN_HSTOP	11	Indicates the last sample to be used for resampling.	RS[109:99]	Input Timing / H Control / Mem Control	1 1/3 2
OUT_HSTART	11	Indicates the placement of the first output sample with live data. This value must be even.	RS[98:88]	Output Timing / H Control / Mem Control	3 1/3 2
OUT_HSTOP	11	Indicates the placement of the last output sample with live data. This value must be odd.	RS[87:77]	Output Timing / H Control / Mem Control	3 1/3 2
V_FLT_DEC	1	Vertical filter decimate. 0 - Non-decimate mode 1 - Decimate mode	RS[76]	VBL Filter	2



**Table 3-2: Serial Interface Download Parameters (Continued)**

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
V_ZOOM_RATIO	22	Vertical zoom ratio. $\frac{IN\_VLIVE \cdot 524288}{OUT\_VLIVE}$ if V_FLT_DEC = 0 $\frac{IN\_VLIVE \cdot 524288}{OUT\_VLIVE \cdot 2}$ if V_FLT_VLIVE = 1	RS[75:54]	V Control	2
IN_VSTART_PHASE	7	Indicates the starting vertical phase to be used for resampling.	RS[53:47]	V Control	2
IN_VSTART	11	Indicates the first line to be used for resampling.	RS[46:36]	Input Timing / V Control	1 2
IN_VSTOP	11	Indicates the last line to be used for resampling.	RS[35:25]	Input Timing / V Control	1 2
OUT_VSTART	11	Indicates the placement of the first output line with live data.	RS[24:14]	Output Timing / V Control	3 2
OUT_VSTOP	11	Indicates the placement of the last output line with live data.	RS[13:3]	Output Timing / V Control	3 2
RS_FILL	3	Not used.	RS[2:0]		
Dynamic Output Parameters <sup>a</sup>	160 Total				
Matrix Coefficients	117 Sub-total	The matrix coefficient format is ±2.10. (i.e. 1 sign bit, 2 integer bits and 10 fractional bits)			
G1	13	Matrix coefficient. $G = G1*Y + G2*C_b + G3*C_r$	OD[159:147]	Output	1
G2	13	Matrix coefficient. $G = G1*Y + G2*C_b + G3*C_r$	OD[146:134]	Output	1
G3	13	Matrix coefficient. $G = G1*Y + G2*C_b + G3*C_r$	OD[133:121]	Output	1
B1	13	Matrix coefficient. $B = B1*Y + B2*C_b + B3*C_r$	OD[120:108]	Output	1
B2	13	Matrix coefficient. $B = B1*Y + B2*C_b + B3*C_r$	OD[107:95]	Output	1
B3	13	Matrix coefficient. $B = B1*Y + B2*C_b + B3*C_r$	OD[94:82]	Output	1
R1	13	Matrix coefficient. $R = R1*Y + R2*C_b + R3*C_r$	OD[81:69]	Output	1



**Table 3-2: Serial Interface Download Parameters (Continued)**

Parameter Name	No. Of Bits	Description	Word Position	Used By	Time Frame
R2	13	Matrix coefficient. $R = R1*Y + R2*C_b + R3*C_r$	OD[68:56]	Output	1
R3	13	Matrix coefficient. $R = R1*Y + R2*C_b + R3*C_r$	OD[55:43]	Output	1
Background Colour		24 Sub-total			
Y_BKGD	8	Background colour for Y. Unsigned integer.	OD[42:35]	Output	1
CB_BKGD	8	Background colour for $C_b$ . Signed integer.	OD[34:27]	Output	1
CR_BKGD	8	Background colour for $C_r$ . Signed integer.	OD[26:19]	Output	1
Output Timing		19 Sub-total			
LINE_ADV	4	Line advance with respect to input timing.	OD[18:15]	Output Timing	0 <sup>a</sup>
H_POS	12	Horizontal position with respect to input timing.	OD[14:3]	Output Timing	0 <sup>a</sup>
OD_FILL	3	Not used.	OD[2:0]		
Filter Coefficients		776 Total			
Horizontal Filter		344 Sub-total			
H_Y_FLT_COEF HYBANK: 12 12 11 10 10 9 9 9 9 8 8 = 107 2 filters * (107 bits) = 214	214	Horizontal Y filter coefficients. Center coefficient is $\pm 1.10$ . (i.e. 1 sign bit, 1 integer bit and 10 fractional bits)	HY[343:130] (See footnote <sup>b</sup> )	H Y Filter	1
H_C_FLT_COEF HCBANK: 12 11 9 9 8 8 8 = 65 2 filters * (65 bits) = 130	130	Horizontal C filter coefficients. Center coefficient is $\pm 1.10$ . (i.e. 1 sign bit, 1 integer bit and 10 fractional bits)	HY[129:0] (See footnote <sup>b</sup> )	H C Filter	1
Vertical Filter		432 Sub-total			
V_Y_FLT_COEF HYBANK: 12 12 11 10 10 9 9 9 9 8 8 = 107 2 filters * (107 bits) = 214	214	Vertical Y filter coefficients. Center coefficient is $\pm 1.10$ . (i.e. 1 sign bit, 1 integer bit and 10 fractional bits)	VY[431:218] (See footnote <sup>c</sup> )	V Y Filter	1
V_C_FLT_COEF HCBANK: 12 12 11 10 10 9 9 9 9 8 8 = 107 2 filters * (107 bits) = 214	214	Vertical C filter coefficients. Center coefficient is $\pm 1.10$ . (i.e. 1 sign bit, 1 integer bit and 10 fractional bits)	VY[217:4] (See footnote <sup>c</sup> )	V C Filter	1
VYF_FILL	4	Not used.	VY[3:0]		



a. The resizing parameters, dynamic output parameters, and the filter coefficients are adjustable (dynamic). The I/O Format parameters are static, i.e. once an input and output format is selected the I/O format parameters tend to remain fixed.

**b. HORIZONTAL COEFFICIENT DOWNLOAD FORMAT:**

HF[343:0] = HYBANK1[106:0] | HYBANK0[106:0] | HCBANK1[64:0] | HCBANK0[64:0]

**IN NON-DECIMATE MODE (H\_FLT\_DEC = 0):**

HYBANK0 contains the coefficients for a 21-tap symmetric FIR filter and HCBANK0 contains the coefficients for a 13-tap symmetric FIR filter. HYBANK1 and HCBANK1 are not used when H\_FLT\_DEC is 0 and should contain 0s.

HYBANK0[106:0] = HYT0[11:0] | HYT1[11:0] | HYT2[10:0] | HYT3[9:0] | HYT4[9:0] | HYT5[8:0] | HYT6[8:0] | HYT7[8:0] | HYT8[8:0] | HYT9[7:0] | HYT10[7:0]

HYBANK1[106:0] = 0

HCBANK0[64:0] = HCT0[11:0] | HCT1[10:0] | HCT2[8:0] | HCT3[8:0] | HCT4[7:0] | HCT5[7:0] | HCT6[7:0]

HCBANK1[64:0] = 0

**IN DECIMATE MODE (H\_FLT\_DEC = 1):**

HYBANK0 and HYBANK1 contain the coefficients for a 41-tap symmetric decimation filter while HCBANK0 and HCBANK1 contain the coefficients for a 25-tap symmetric decimation filter. BANK0s contain the center tap (tap 0) and all odd taps (e.g. 1, 3, 5....) while the BANK1s contain a zero and all even taps (e.g. 2, 4, 6....).

HYBANK0[106:0] = HYT0[11:0] | HYT1[11:0] | HYT3[10:0] | HYT5[9:0] | HYT7[9:0] | HYT9[8:0] | HYT11[8:0] | HYT13[8:0] | HYT15[8:0] | HYT17[7:0] | HYT19[7:0]

HYBANK1[106:0] = "000000000000" | HYT2[11:0] | HYT4[10:0] | HYT6[9:0] | HYT8[9:0] | HYT10[8:0] | HYT12[8:0] | HYT14[8:0] | HYT16[8:0] | HYT18[7:0] | HYT20[7:0]

HCBANK0[64:0] = HCT0[11:0] | HCT1[10:0] | HCT3[8:0] | HCT5[8:0] | HCT7[7:0] | HCT9[7:0] | HCT11[7:0]

HCBANK1[64:0] = "000000000000" | HCT2[10:0] | HCT4[8:0] | HCT6[8:0] | HCT8[7:0] | HCT10[7:0] | HCT12[7:0]

Further information on the horizontal filter coefficients is given in FIR Filter Parameters ([3.4.2.2 FIR Filter Parameters](#)).

**c. VERTICAL COEFFICIENT DOWNLOAD FORMAT:**

VF[431:0] = VYBANK1[106:0] | VYBANK0[106:0] | VCBANK1[106:0] | VCBANK0[106:0] | "0000"

**IN NON-DECIMATE MODE (V\_FLT\_DEC = 0):**

VYBANK0 and VCBANK0 both contain the coefficients for a 21-tap symmetric FIR filter. VYBANK1 and VCBANK1 are not used when V\_FLT\_DEC is 0 and should contain 0s.

VYBANK0[106:0] = VYT0[11:0] | VYT1[11:0] | VYT2[10:0] | VYT3[9:0] | VYT4[9:0] | VYT5[8:0] | VYT6[8:0] | VYT7[8:0] | VYT8[8:0] | VYT9[7:0] | VYT10[7:0]

VYBANK1[106:0] = 0

VCBANK0[106:0] = VCT0[11:0] | VCT1[11:0] | VCT2[10:0] | VCT3[9:0] | VCT4[9:0] | VCT5[8:0] | VCT6[8:0] | VCT7[8:0] | VCT8[8:0] | VCT9[7:0] | VCT10[7:0]

VCBANK1[106:0] = 0

**IN DECIMATE MODE (V\_FLT\_DEC = 1):**

VYBANK0 and VYBANK1 together contain the coefficients for a 41-tap symmetric decimation filter while VCBANK0 and VCBANK1 together also contain the coefficients for a 41-tap symmetric decimation filter. BANK0s contain the center tap (tap 0) and all odd taps (e.g. 1, 3, 5....19) while the BANK1s contain a zero and all even taps (e.g. 2, 4, 6....20).

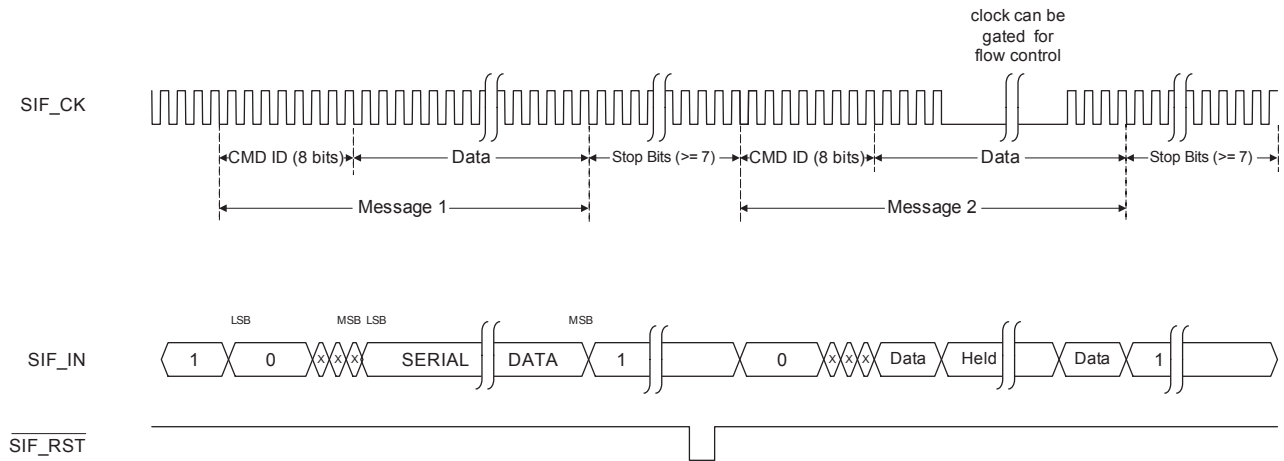
VYBANK0[106:0] = VYT0[11:0] | VYT1[11:0] | VYT3[10:0] | VYT5[9:0] | VYT7[9:0] | VYT9[8:0] | VYT11[8:0] | VYT13[8:0] | VYT15[8:0] | VYT17[7:0] | VYT19[7:0]

VYBANK1[106:0] = "000000000000" | VYT2[11:0] | VYT4[10:0] | VYT6[9:0] | VYT8[9:0] | VYT10[8:0] | VYT12[8:0] | VYT14[8:0] | VYT16[8:0] | VYT18[7:0] | VYT20[7:0]

VCBANK0[106:0] = VCT0[11:0] | VCT1[11:0] | VCT3[10:0] | VCT5[9:0] | VCT7[9:0] | VCT9[8:0] | VCT11[8:0] | VCT13[8:0] | VCT15[8:0] | VCT17[7:0] | VCT19[7:0]

VCBANK1[106:0] = "000000000000" | VCT2[11:0] | VCT4[10:0] | VCT6[9:0] | VCT8[9:0] | VCT10[8:0] | VCT12[8:0] | VCT14[8:0] | VCT16[8:0] | VCT18[7:0] | VCT20[7:0]

The GF9320 parameters are downloaded using a 3-pin serial interface. The serial interface consists of a clock, data and a reset as shown in [Figure 3-1: Serial Interface Download Signal Specification](#). The serial interface reset (SIF\_RST) is provided to re-synchronise the download operation in the event that it is interrupted.



NOTES:

1) SIF\_IN: Serial Data Input. Must be held high (logic 1) if no message is being sent and SIF\_CLK is running. First byte sent is the CMD\_ID. All data including CMD\_ID is sent LSB first. Valid choices for CMD\_ID are:

- LSB ... MSB
- 01234567
- 0 (00000000) : A download of all parameters (1176 data bits)
- 1 (00000100): A download of the I/O parameters (88 data bits)
- 2 (00000010): A download of the resizing parameters (152 data bits)
- 3 (00000110): A download of the Dynamic Output parameters (160 data bits)
- 4 (00000001): A download of the Horizontal Filter coefficients (344 data bits)
- 5 (00000101): A download of the Vertical Filter coefficients (432 data bits)

2) SIF\_CLK: Serial Clock. All data from SIF\_IN is clocked on the positive edge of SIF\_CLK. SIF\_CLK may be held low to pause transmission (i.e. implement flow control).

3) SIF\_RST: Message Reset. Active low and asynchronous. Used to recover from a transmission error or message abort. Can be asserted between each message to ensure correct initialization of the download, but is not necessary in general as long as the correct message format (as indicated above) is followed.

Figure 3-1: Serial Interface Download Signal Specification

### 3.3 Input Processing

The input processor decodes the input TRS from the incoming video stream. This provides input video timing information to the GF9320. An area of the input video data is selected for scaling according to the downloaded parameters (i.e. IN\_HSTART, IN\_HSTOP, IN\_VSTART, and IN\_VSTOP). This operation is called the windowing operation. Based on the input field / frame timing and the I/O format parameters a memory enable signal is generated by the input controller. This signal controls the field / frame switching of the SDRAM memory controller. Also, a frame-reset signal is sent to the output controller for use in internal lock mode (OUT\_REF=0). The frame reset signal and the field / frame switch point is based on input TRS F-bit in interlaced modes (non-film). Otherwise, (i.e. progressive and all film modes) the frame reset signal and the field / frame switch point is based on one line after input TRS V-bit. Note that in film modes the frame reset signal and field / frame switch point vary according the input and output frame rates.



### 3.4 Scaling Processor

At the heart of the GF9320 is the scaling processor. It is here where the raw input image selected from the input video is translated into a raw output image of selected size according to user controlled scaling parameters. As described in [3.1 Device Overview](#), general 2D scaling is performed by cascading two 1D-scaling filters. This section describes both the horizontal and vertical scaling filters. A block diagram of the horizontal resizing filter is shown in [Figure 3-2: Horizontal Scaling Filter](#). A block diagram of the vertical resizing filter is shown [Figure 3-3: Vertical Scaling Filter](#).

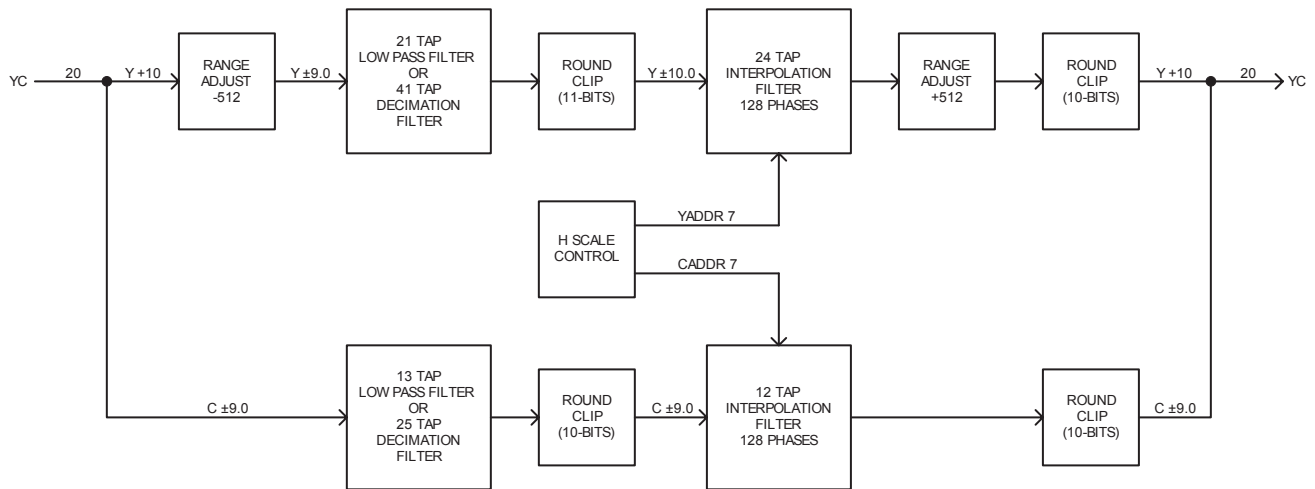


Figure 3-2: Horizontal Scaling Filter

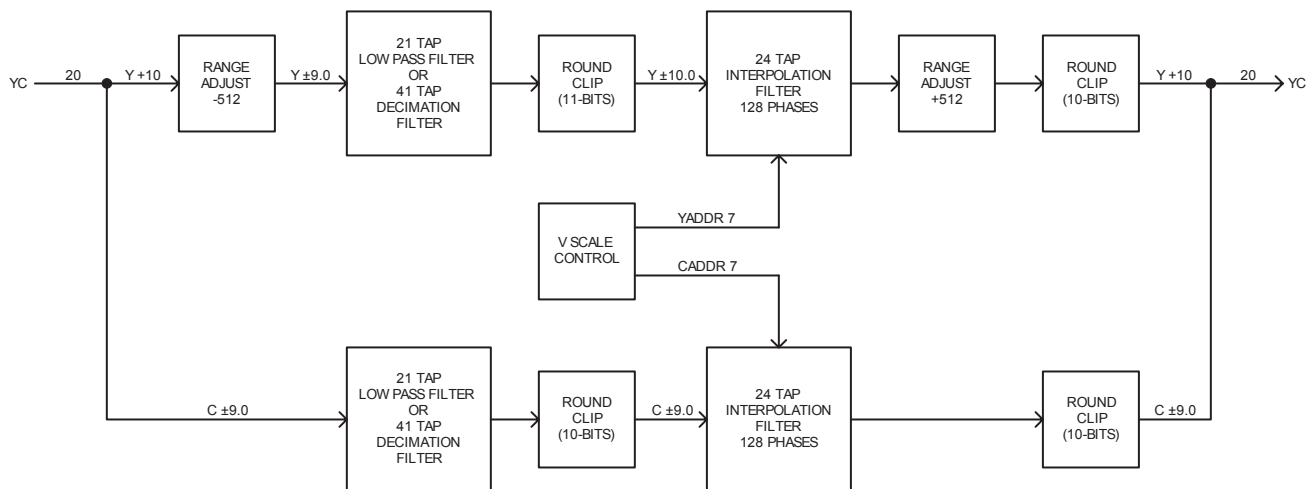


Figure 3-3: Vertical Scaling Filter



### 3.4.1 Scalar Processing

General 1D scaling is performed by cascading an FIR filter with an interpolation filter. The FIR filter is needed to band limit the input signal when the output Nyquist frequency is less than the input Nyquist frequency. The interpolation filter is used to resample the input signal to the new output rate.

#### 3.4.1.1 FIR Filter

The purpose of the FIR filters is to band limit or shape the input signal. Each filter is user programmable, with the coefficients derived depending on the required frequency response. The FIR filter can be used in one of two modes: decimate and non-decimate.

Decimate mode can be used when the output rate is half the input rate. The advantage to using decimate mode is that the number of taps is approximately doubled by using two input clocks to compute one output sample. In non-decimate mode the filter is 21 taps (13 for horizontal colour difference due to the 4:2:2 input video structure). In decimate mode the filter is 41 taps (25 for horizontal colour difference).

Vertically the same modes are available however due to the 4:2:2 sampling structure both luma and colour difference have equal numbers of taps, i.e. 41 taps for decimate and 21 taps for non-decimate.

The filter operation is described by:

$$\begin{aligned}
 HY_O(n) \cdot 1024 = & \begin{cases} \sum_{k=1}^{k=10} HYT\langle 2k-1\_k \rangle \cdot [HY_I(n-k) + HY_I(n+k)] & H\_FLT\_DEC = 0 \\ HYT0\_0 \cdot HY_I(n) + \sum_{k=1}^{k=10} HYT\langle 2k-1\_k \rangle \cdot [HY_I(n-2k+1) + HY_I(n+2k-1)] + \\ \sum_{k=1}^{k=10} HYT\langle 2k \rangle \cdot [HY_I(n-2k) + HY_I(n+2k)] & H\_FLT\_DEC = 1 \end{cases} \\
 HC_O(n) \cdot 1024 = & \begin{cases} \sum_{k=1}^{k=6} HCT\langle 2k-1\_k \rangle \cdot [HC_I(n-k) + HC_I(n+k)] & H\_FLT\_DEC = 0 \\ HCT0\_0 \cdot HC_I(n) + \sum_{k=1}^{k=6} HCT\langle 2k-1\_k \rangle \cdot [HC_I(n-2k+1) + HC_I(n+2k-1)] + \\ \sum_{k=1}^{k=6} HCT\langle 2k \rangle \cdot [HC_I(n-2k) + HC_I(n+2k)] & H\_FLT\_DEC = 1 \end{cases}
 \end{aligned}$$



$$\begin{aligned}
 VY_O(n) \cdot 1024 = & \begin{cases} \begin{aligned} & k = 10 \\ & VYT0\_0 \cdot VY_I(n) + \sum_{k=1}^{10} VYT\langle 2k-1\_k \rangle \cdot [VY_I(n-k) + VY_I(n+k)] \end{aligned} & V\_FLT\_DEC = 0 \\ \\ \begin{aligned} & k = 10 \\ & VYT0\_0 \cdot VY_I(n) + \sum_{k=1}^{10} VYT\langle 2k-1\_k \rangle \cdot [VY_I(n-2k+1) + VY_I(n+2k-1)] + \\ & \sum_{k=1}^{10} VYT\langle 2k \rangle \cdot [VY_I(n-2k) + VY_I(n+2k)] \end{aligned} & V\_FLT\_DEC = 1 \end{cases} \\
 \\
 VC_O(n) \cdot 1024 = & \begin{cases} \begin{aligned} & k = 10 \\ & VCT0\_0 \cdot VC_I(n) + \sum_{k=1}^{10} VCT\langle 2k-1\_k \rangle \cdot [VC_I(n-k) + VC_I(n+k)] \end{aligned} & V\_FLT\_DEC = 0 \\ \\ \begin{aligned} & k = 10 \\ & VCT0\_0 \cdot VC_I(n) + \sum_{k=1}^{10} VCT\langle 2k-1\_k \rangle \cdot [VC_I(n-2k+1) + VC_I(n+2k-1)] + \\ & \sum_{k=1}^{10} VCT\langle 2k \rangle \cdot [VC_I(n-2k) + VC_I(n+2k)] \end{aligned} & V\_FLT\_DEC = 1 \end{cases}
 \end{aligned}$$

where  $HY_I(n)$ ,  $HC_I(n)$ ,  $VY_I(n)$  and  $VC_I(n)$  are the FIR filter inputs,

$HY_O(n)$ ,  $HC_O(n)$ ,  $VY_O(n)$  and  $VC_O(n)$  are the FIR filter outputs,

$HYT$ ,  $HCT$ ,  $VYT$ , and  $VCT$  are the filter coefficients as given in [Table 3-3: Horizontal Filter Coefficients](#) and [Table 3-4: Vertical Filter Coefficients](#), and

1024 is the DC gain of the filter.

In non-decimate mode only one bank of coefficients are used (Bank 0), but in decimate mode both banks of coefficients are used (Bank 0 and Bank 1).

### 3.4.1.2 Interpolation Filter

After FIR filtering the video data is passed to the interpolation filter where the rate conversion is performed. The interpolation filter is a polyphase filter that allows the output phase to be adjusted every clock cycle. The interpolation filter contains 128 phases (64 phases for horizontal colour difference). The phase selection allows generation of an output anywhere between two inputs with 1/128 input pixel resolution (1/64 for horizontal colour difference). The scaling control unit takes as input the scaling ratio (input / output), and starting phase (starting position of the first output pixel with respect to the input). With these parameters, the scaling control chooses the correct phasing sequence for the interpolator, determines which input samples should be held and for how long (up sampling), which interpolator outputs should be discarded (down sampling), and generates the new output.





### 3.4.2 Resizing Parameters

In order to understand how to program the GF9320 to perform the necessary conversions an explanation of the window parameters, the zoom parameters and the filter parameters is necessary.

#### 3.4.2.1 Window Parameters

Figure 3-4: Input Window Definition - Progressive through Figure 3-7: Output Window Definition - Interlaced show how the GF9320 places a window over the input and output active video. This window is selected by using offsets from the active video area (HSTART, HSTOP, VSTART, VSTOP). Note that VSTART and VSTOP for interlaced video refers to field based offsets. The windowed portion is referred to as the live video and can cover the entire active video or just a portion of it. The size of the windowed portion is HLIVE by VLIVE pixels where:

$$HLIVE = HSTOP - HSTART + 1$$

$$VLIVE = VSTOP - VSTART + 1$$

For interlaced video one field may have one more active line than the other. This means that VLIVE is longer for that field. Also, in interlaced film modes VSTART and VSTOP are still field-based offsets but VLIVE is frame based since the fields are merged and processed as a frame.

The input video window is determined by IN\_HSTART, IN\_HSTOP, IN\_VSTART, and IN\_VSTOP. The size of the input windowed portion is IN\_HLIVE by IN\_VLIVE pixels.

The output video window is determined by OUT\_HSTART, OUT\_HSTOP, OUT\_VSTART, and OUT\_VSTOP. The size of the output windowed portion is OUT\_HLIVE by OUT\_VLIVE pixels.

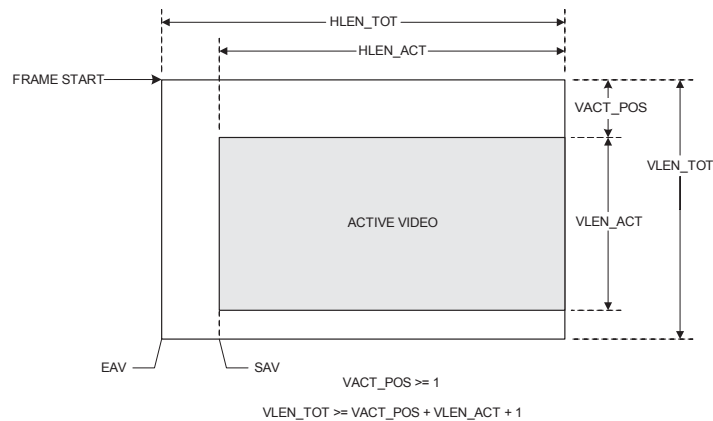


Figure 3-4: Input Window Definition - Progressive

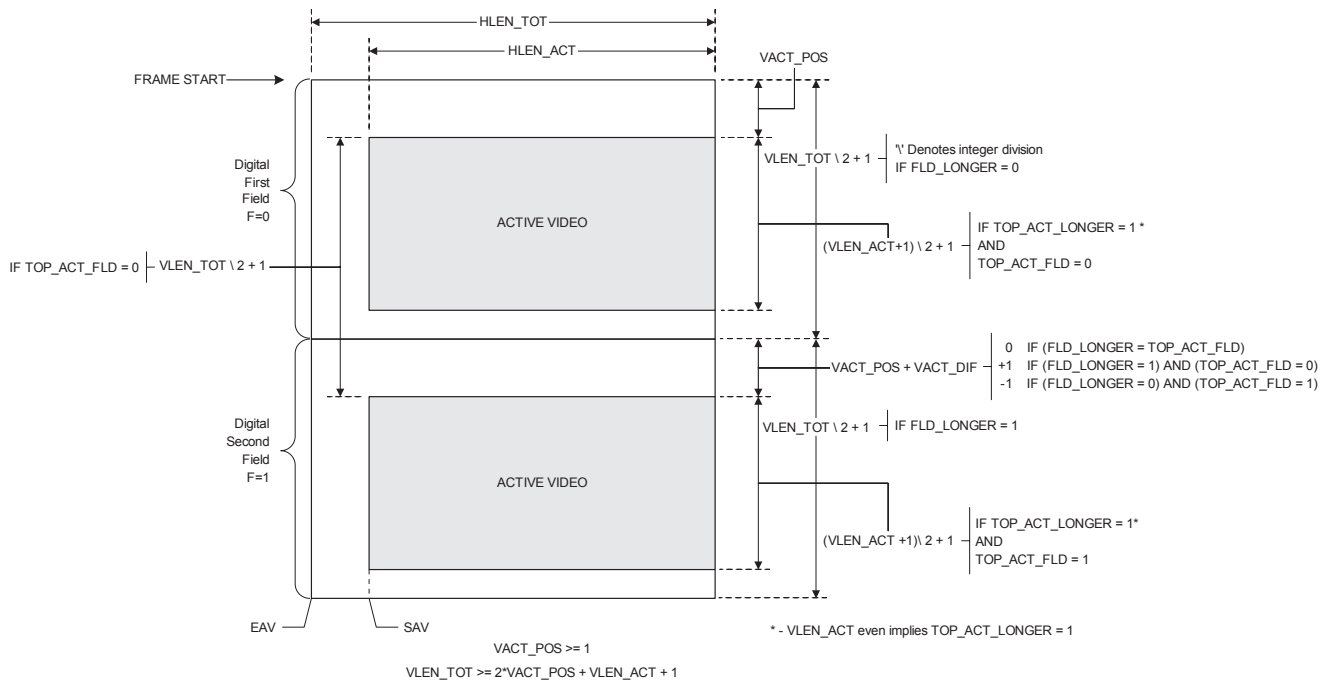


Figure 3-5: Input Window Definition - Interlaced

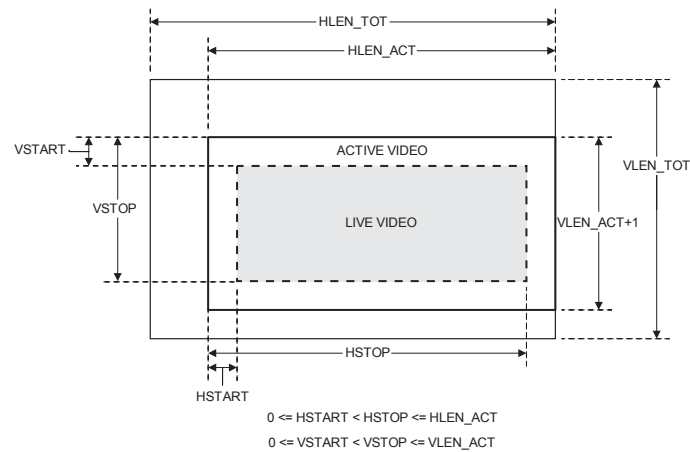


Figure 3-6: Output Window Definition - Progressive

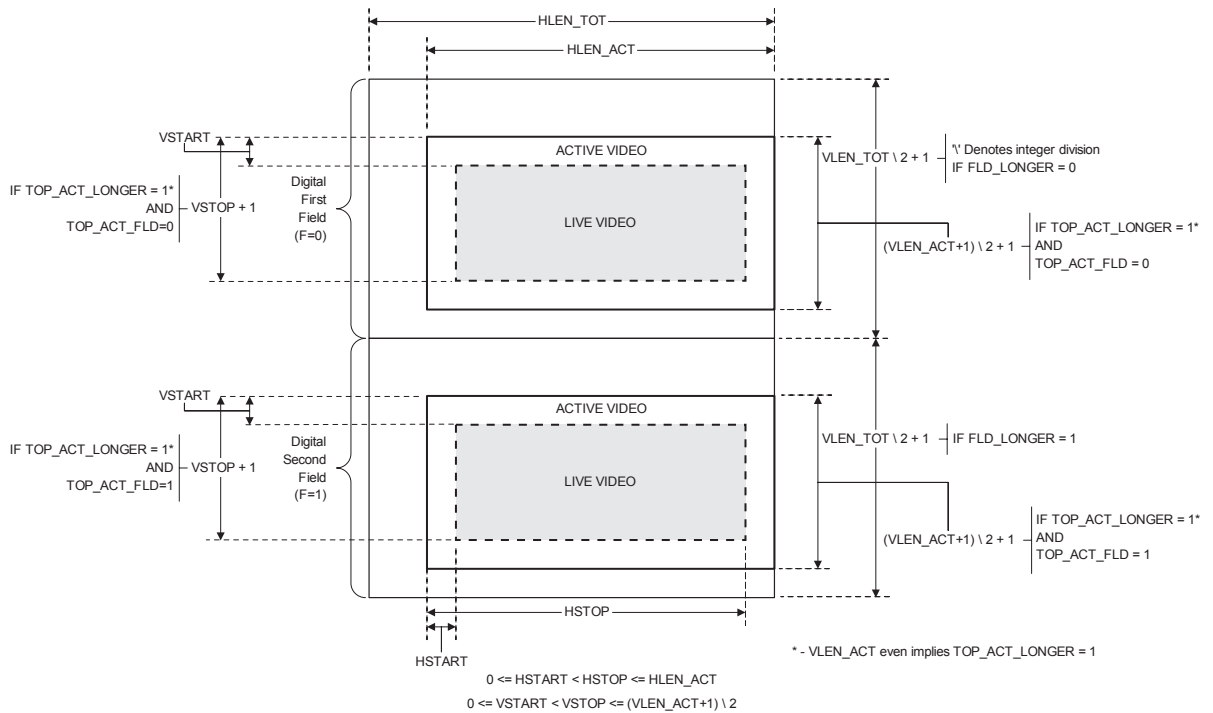


Figure 3-7: Output Window Definition - Interlaced

### 3.4.2.2 FIR Filter Parameters

The FIR filter shape is programmable by downloading the filter coefficients. The horizontal filter coefficients and download positions are given in [Table 3-3: Horizontal Filter Coefficients](#). The vertical filter coefficients are given in [Table 3-4: Vertical Filter Coefficients](#). The overall gain of the FIR filter is 1024, but the range of coefficients is larger to permit implementation of enhancement filters. Note that the coefficients change meaning depending on the filter structure (i.e. if the filter is in decimate mode or not). The filter structure is determined by the FLT\_DEC parameter. If H\_FLT\_DEC is 1, then the horizontal FIR filter is configured in decimate mode. If H\_FLT\_DEC is 0, then the horizontal FIR filter is configured in non-decimate mode. If V\_FLT\_DEC is 1, then the vertical FIR filter is configured in decimate mode. If V\_FLT\_DEC is 0, then the vertical FIR filter is configured in non-decimate mode.



Table 3-3: Horizontal Filter Coefficients

Parameter	No. of Bits	Range	Word Position
twelve_zeros	12	[0, 0]	HF[343:332]
HYT2	12	[-2048, 2047]	HF[331:320]
HYT4	11	[-1024, 1023]	HF[319:309]
HYT6	10	[-512, 511]	HF[308:299]
HYT8	10	[-512, 511]	HF[298:289]
HYT10	9	[-256, 255]	HF[288:280]
HYT12	9	[-256, 255]	HF[279:271]
HYT14	9	[-256, 255]	HF[270:262]
HYT16	9	[-256, 255]	HF[261:253]
HYT18	8	[-128, 127]	HF[252:245]
HYT20	8	[-128, 127]	HF[244:237]
HYT0_0	12	[-2048, 2047]	HF[236:225]
HYT1_1	12	[-2048, 2047]	HF[224:213]
HYT3_2	11	[-1024, 1023]	HF[212:202]
HYT5_3	10	[-512, 511]	HF[201:192]
HYT7_4	10	[-512, 511]	HF[191:182]
HYT9_5	9	[-256, 255]	HF[181:173]
HYT11_6	9	[-256, 255]	HF[172:164]
HYT13_7	9	[-256, 255]	HF[163:155]
HYT15_8	9	[-256, 255]	HF[154:146]
HYT17_9	8	[-128, 127]	HF[145:138]
HYT19_10	8	[-128, 127]	HF[137:130]
twelve_zeros	12	[0, 0]	HF[129:118]
HCT2	11	[-1024, 1023]	HF[117:107]
HCT4	9	[-256, 255]	HF[106:98]
HCT6	9	[-256, 255]	HF[97:89]
HCT8	8	[-128, 127]	HF[88:81]
HCT10	8	[-128, 127]	HF[80:73]
HCT12	8	[-128, 127]	HF[72:65]
HCT0_0	12	[-2048, 2047]	HF[64:53]
HCT1_1	11	[-1024, 1023]	HF[52:42]
HCT3_2	9	[-256, 255]	HF[41:33]

**Table 3-3: Horizontal Filter Coefficients (Continued)**

Parameter	No. of Bits	Range	Word Position
HCT5_3	9	[-256, 255]	HF[32:24]
HCT7_4	8	[-128, 127]	HF[23:16]
HCT9_5	8	[-128, 127]	HF[15:8]
HCT11_6	8	[-128, 127]	HF[7:0]

**Table 3-4: Vertical Filter Coefficients**

Parameter	No. of Bits	Range	Word Position
twelve_zeros	12	[0, 0]	VF[431:420]
VYT2	12	[-2048, 2047]	VF[419:408]
VYT4	11	[-1024, 1023]	VF[407:397]
VYT6	10	[-512, 511]	VF[396:387]
VYT8	10	[-512, 511]	VF[386:377]
VYT10	9	[-256, 255]	VF[376:368]
VYT12	9	[-256, 255]	VF[367:359]
VYT14	9	[-256, 255]	VF[358:350]
VYT16	9	[-256, 255]	VF[349:341]
VYT18	8	[-128, 127]	VF[340:333]
VYT20	8	[-128, 127]	VF[332:325]
VYT0_0	12	[-2048, 2047]	VF[324:313]
VYT1_1	12	[-2048, 2047]	VF[312:301]
VYT3_2	11	[-1024, 1023]	VF[300:290]
VYT5_3	10	[-512, 511]	VF[289:280]
VYT7_4	10	[-512, 511]	VF[279:270]
VYT9_5	9	[-256, 255]	VF[269:261]
VYT11_6	9	[-256, 255]	VF[260:252]
VYT13_7	9	[-256, 255]	VF[251:243]
VYT15_8	9	[-256, 255]	VF[242:234]
VYT17_9	8	[-128, 127]	VF[233:226]
VYT19_10	8	[-128, 127]	VF[225:218]
twelve_zeros	12	[0, 0]	VF[217:206]
VCT2	12	[-2048, 2047]	VF[205:194]
VCT4	11	[-1024, 1023]	VF[193:183]

**Table 3-4: Vertical Filter Coefficients (Continued)**

Parameter	No. of Bits	Range	Word Position
VCT6	10	[-512, 511]	VF[182:173]
VCT8	10	[-512, 511]	VF[172:163]
VCT10	9	[-256, 255]	VF[162:154]
VCT12	9	[-256, 255]	VF[153:145]
VCT14	9	[-256, 255]	VF[144:136]
VCT16	9	[-256, 255]	VF[135:127]
VCT18	8	[-128, 127]	VF[126:119]
VCT20	8	[-128, 127]	VF[118:111]
VCT0_0	12	[-2048, 2047]	VF[110:99]
VCT1_1	12	[-2048, 2047]	VF[98:87]
VCT3_2	11	[-1024, 1023]	VF[86:76]
VCT5_3	10	[-512, 511]	VF[75:66]
VCT7_4	10	[-512, 511]	VF[65:56]
VCT9_5	9	[-256, 255]	VF[55:47]
VCT11_6	9	[-256, 255]	VF[46:38]
VCT13_7	9	[-256, 255]	VF[37:29]
VCT15_8	9	[-256, 255]	VF[28:20]
VCT17_9	8	[-128, 127]	VF[19:12]
VCT19_10	8	[-128, 127]	VF[11:4]
fill	4	[0, 0]	VF[3:0]

### 3.4.2.3 Zoom Parameters

The zoom parameters (IN\_HSTART\_PHASE, IN\_VSTART\_PHASE, H\_ZOOM\_RATIO, and V\_ZOOM\_RATIO) specify the precise conversion from the input live video to the output live video. IN\_HSTART\_PHASE and IN\_VSTART\_PHASE allows for starting the interpolator with sub-pixel accuracy. This allows for maintaining the true center of picture when zooming and panning. The zoom ratio is approximately:

$$\begin{aligned}
 H\_ZOOM\_RATIO &= \begin{cases} \frac{IN\_HLIVE \cdot 524288}{OUT\_VLIVE} & H\_FLT\_DEC = 0 \\ \frac{IN\_HLIVE \cdot 524288}{OUT\_HLIVE \cdot 2} & H\_FLT\_DEC = 1 \end{cases} \\
 V\_ZOOM\_RATIO &= \begin{cases} \frac{IN\_VLIVE \cdot 524288}{OUT\_VLIVE} & V\_FLT\_DEC = 0 \\ \frac{IN\_VLIVE \cdot 524288}{OUT\_VLIVE \cdot 2} & V\_FLT\_DEC = 1 \end{cases}
 \end{aligned}$$



The above equations hold only approximately because the zoom ratio must be adjusted to maintain the true center of picture.

When using the GF9320 there is a preventable condition whereby certain memory configurations cause artifacts in the output image. It is dependent upon the vertical parameters of the output video and the number of SDRAMs employed in the right memory bank as follows:

$$\text{OUT\_VLIVE modulo } (64 * N) = (64 * N) - 3 \text{ or } (64 * N) - 1$$

Where N is the number of memories in each array of the right bank, MEM\_CONFIG\_RIGHT, and

$$\text{OUT\_VLIVE} = \text{OUT\_VSTOP} - \text{OUT\_VSTART} + 1$$

Artifacts can be avoided by monitoring for the condition. When detected, add or subtract one (1) from the OUT\_VSTOP value while maintaining the condition:

$$0 \leq \text{OUT\_VSTART} < \text{OUT\_VSTOP}$$

Note that both fields must be checked for this condition when the output is interlaced with one field longer.

### 3.4.3 Dynamic Zoom and Pan Considerations

The GF9320 is designed to perform frame accurate zooming and panning. Some of the downloaded zoom and pan parameters are used by multiple blocks within the GF9320. These blocks operate on the video data at different time frames. For instance, the input control block operates on the video data on frame / field (N) while the vertical scaling block operates on the video data on frame / field (N-1). Both these blocks need the IN\_VSTART parameter. So, the IN\_VSTART parameter must be used by the scaling block one field / frame later than the input block. Registering the IN\_VSTART parameter on the field / frame boundary before the scaling block uses it does this.

While most dynamic zoom and pan situations are taken care of automatically by the GF9320, some dynamic zoom and pan conditions require special downloading.

#### 3.4.3.1 H\_PROC\_FIRST Switching

The H\_PROC\_FIRST download bit is special because it actually changes the configuration of the GF9320. In particular, changing the H\_PROC\_FIRST bit from 1 to 0 makes the horizontal filter switch from operating on field / frame (N) to operating on field / frame (N-2) and vice versa. Note that changing the H\_PROC\_FIRST bit from 1 to 0 is changing from down sampling to up sampling. In order to handle this special case smoothly, a 1:1 horizontal zoom factor must be downloaded.



The recommended sequence for switching from H\_PROC\_FIRST equal to 1 to 0 (i.e. down sampling to up sampling) is:

1. Keep H\_PROC\_FIRST equal to 1 and download H\_ZOOM\_RATIO equal to 524,288 (down sampling).
2. Wait at least 2 frames / fields.
3. Change H\_PROC\_FIRST to 0 and download H\_ZOOM\_RATIO equal to 524,287 (up sampling).
4. Change to the desired H\_ZOOM\_RATIO.

The recommended sequence for switching from H\_PROC\_FIRST equal to 0 to 1 (i.e. up sampling to down sampling) is:

1. Keep H\_PROC\_FIRST equal to 0 and download a H\_ZOOM\_RATIO equal to 524,287 (up sampling).
2. Change H\_PROC\_FIRST to 1 and download H\_ZOOM\_RATIO equal to 524,288 (down sampling).
3. Change to the desired H\_ZOOM\_RATIO.

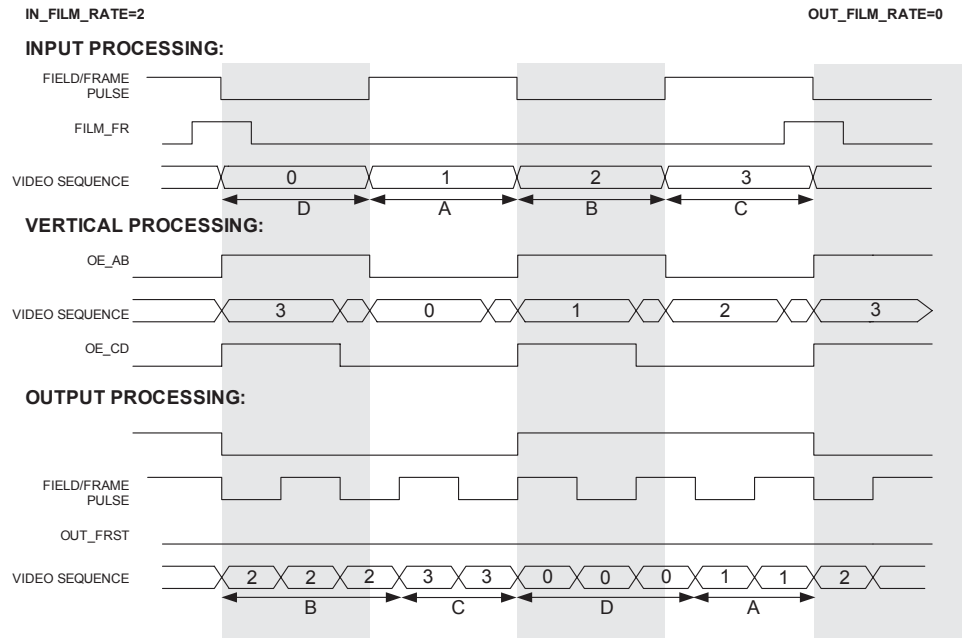
#### 3.4.3.2 V\_FLT\_DEC Switching

The vertical filter operates on field / frame (N-1), but the vertical filter coefficients operate on field / frame (N). When the V\_FLT\_DEC is switched from 0 to 1 or vice versa, the vertical filter coefficients must be delayed by one field / frame so that they operate on the same time frame. This is necessary because the filter coefficients are used differently in decimation mode and a non-decimation filter would be used in decimation mode and vice versa. This would most directly affect the DC gain of the filter that may be perceived as a brightness change in the output video. The horizontal coefficients do not need to be delayed when switching H\_FLT\_DEC because the horizontal filter and the horizontal coefficients operate on the same frame / field (N). Even though H\_FLT\_DEC is switched, down sampling (H\_PROC\_FIRST=1) is indicated. Delaying the vertical filter coefficients may not be necessary depending on the application.

#### 3.4.3.3 Pseudo Synchronous Film Mode Conversions

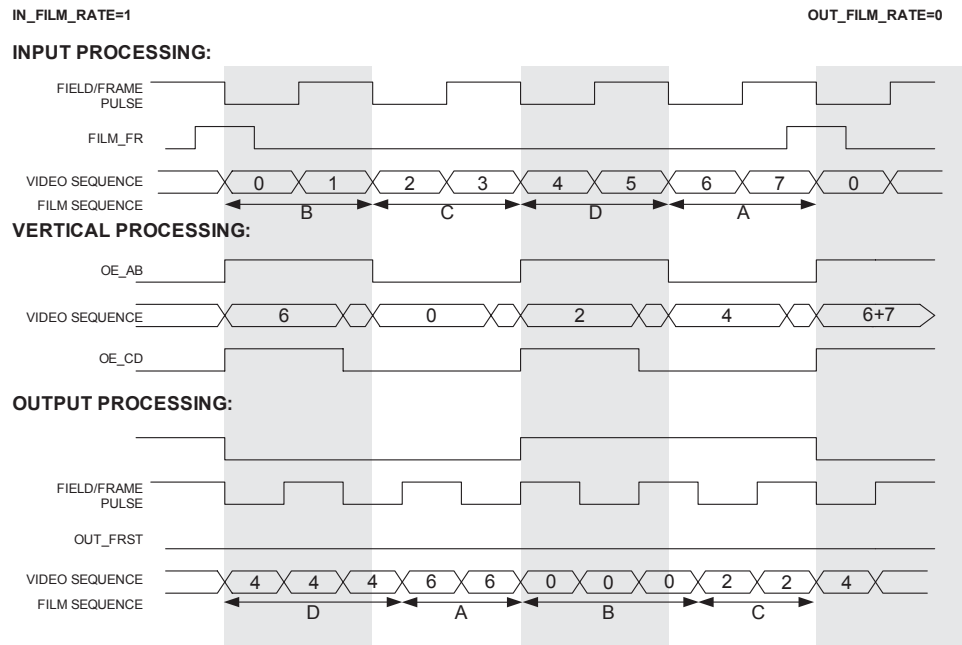
This section applies to any film mode conversion when the input frame rate or the output film rate is 3:2 pull-down, but the input rate is not (i.e. 48→60, 24→60). In these cases the zoom and pan update rate is restricted to every other film frame as shown in [Figure 3-8: 24/24/60 Download Restrictions](#) and [Figure 3-9: 48/24/60 Download Restrictions](#). This is because the output circuit must be updated on an output field / frame boundary.





Do not download in the shaded regions (OE\_AB=1). If the GF9320 is downloaded in the shaded region, the output circuit will be updated in the middle of an output field/frame and will cause one field/frame of the output to be invalid.

**Figure 3-8: 24/24/60 Download Restrictions**



Do not download in the shaded regions (OE\_AB=1). If the GF9320 is downloaded in the shaded region, the output circuit will be updated in the middle of an output field/frame and will cause one field/frame of the output to be invalid.

**Figure 3-9: 48/24/60 Download Restrictions**



### 3.5 SDRAM Memory Interface

#### 3.5.1 Memory Interface Description

To achieve high quality scaling of images in two dimensions, separate processing has to be done in the horizontal and vertical dimensions using one dimensional filter banks. Hence, the input image has to be transposed before and after vertical processing and uses SDRAMs to achieve real-time transposition of digital video images using high quality filters.

The SDRAM controller within the GF9320 acts as the master controller of the memory arrays. To perform a transpose operation the memory controller writes the entire image from one field into the image buffer and then reads it out during the next field. Further, during film mode processing, the controller can put two consecutive image fields together and read them out in the next frame as a single progressive frame. The latter technique is used for processing film material with 3:2 pull-down. We can also separate even and odd fields from a progressive frame to create film material with 3:2 pull-down. The memory organization for transposing images at high data rates is shown in [Figure 3-10: Memory Interface](#).

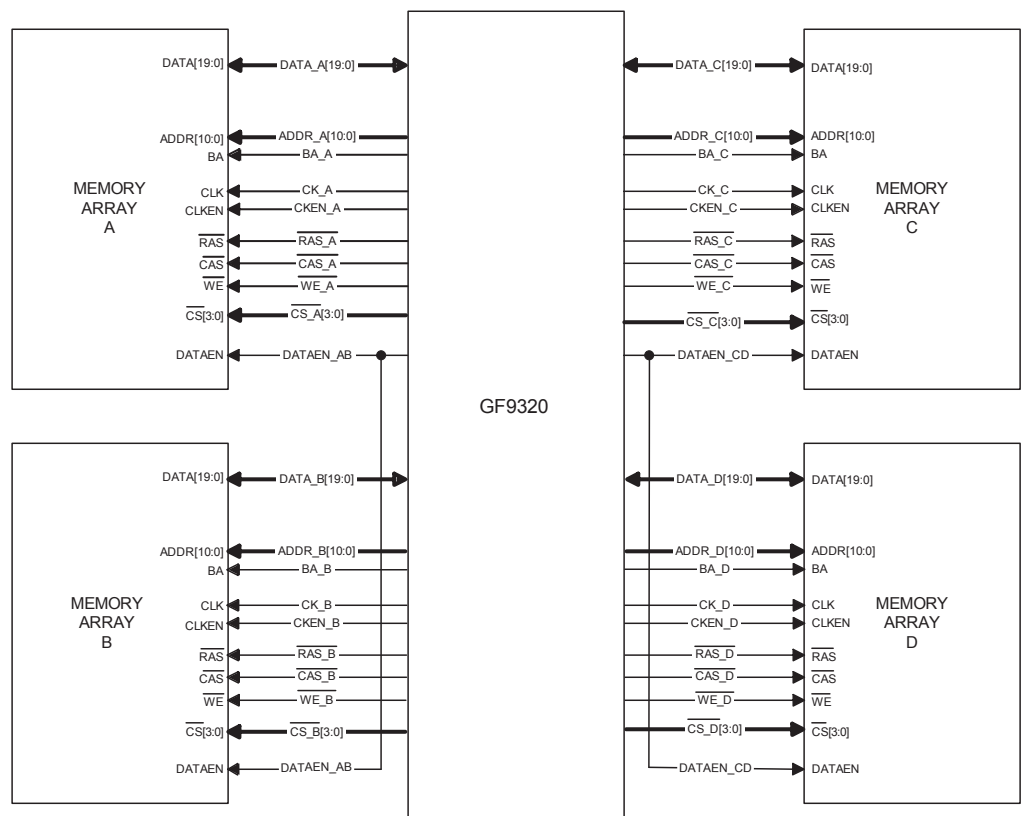
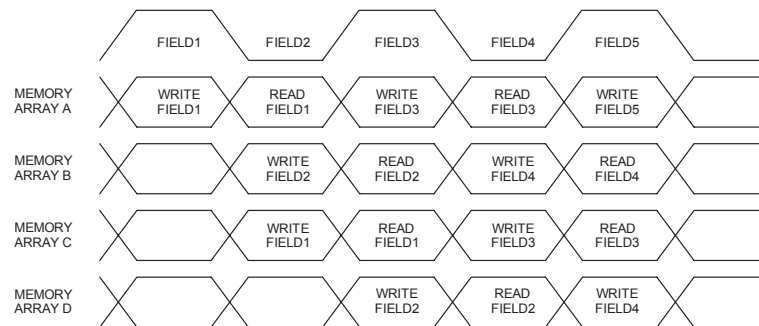


Figure 3-10: Memory Interface



The memory organization consists of four arrays of memories communicating with the GF9320. Each array can contain anywhere between one to five SDRAMs based on format conversion mode. Memory array A and B compose the left bank while memory array C and D compose the right bank. To achieve high bandwidth, the memory arrays are arranged in an interleaved fashion. That is, when one field is written into memory array A, the other field will be read out of memory array B. The sequence of read / write operations that takes place in non-film applications is shown in Figure 3-11: Timing Diagram of Data between GF9320 and SDRAMs for non-film Modes.



**Figure 3-11: Timing Diagram of Data between GF9320 and SDRAMs for non-film Modes**

The data from an odd field is written into memory array A during Field3. At the same time data from the previous (even) field will be read out as a transposed image from memory array B. The horizontal rows of data read out from memory array B will then be processed (vertical processing) within the GF9320 and written into memory array D. Simultaneously, the vertically processed image data from two fields back which was written into memory array C will be read out. When the image is read out from memory array C, it went through another image transposition so that the image is back to its original orientation. Effectively, there is a two field / frame delay when processing non-film material.

The GF9320 experiences significantly more processing time in the vertical processing section due to the bandwidth limitations of the SDRAMs. For some conversions the processing time might exceed the available time. This condition can be circumvented by either increasing the number of memories in the array or by increasing the processing clock rate.

During vertical processing, the GF9320 pre-reads (number of pixels = PIX2READ) into its internal FIFO, before the beginning of every scan line so that it can supply the pixels from the FIFO into the one-dimensional filter in an uninterrupted way. The number of pixels to be pre-read is chosen based on several I/O parameters so that it is high enough to supply data continuously to the filter but low enough to complete the vertical processing in the available time.



The PIX2READ parameter is calculated by:

$$\text{PIX2READ} = \text{MIN} \left\{ \text{MAX} \left( 8 + \text{CEIL} \left[ \frac{\text{IN\_VLEN\_ACT}}{64 \times (4 - \text{MEM\_CONFIG\_LEFT})} \right], 10 \right), 127 \right\}$$

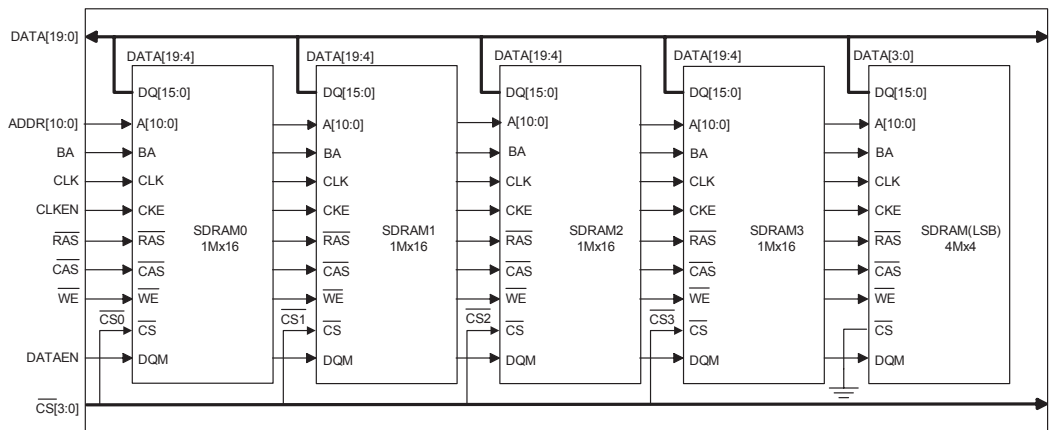
Where IN\_VLEN\_ACT is the total number of active lines per frame,

CEIL(x) is the smallest integer larger than x;

$$\text{MAX}(a,b) = \begin{cases} a & \text{if } a \geq b \\ b & \text{if } a < b \end{cases}$$

$$\text{MAX}(a,b) = \begin{cases} a & \text{if } a \geq b \\ b & \text{if } a < b \end{cases}$$

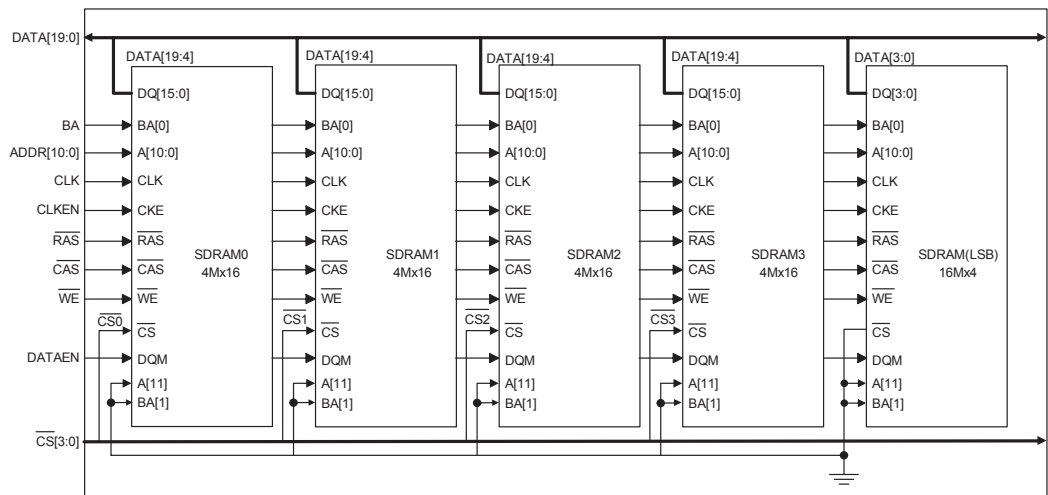
80Mbits or 5 x 16Mbit SDRAMs are required to store 2048 x 2048 x 20 bits (maximum image size). As illustrated in [Figure 3-12: Architecture of Memory Array with four 1Mx16 and one 4Mx4 SDRAMs](#), the memory array has a 20-bit data bus path, supported by blocks of four 1Mx16 SDRAMs and one 4Mx4 used in parallel, sharing a common address / control bus. 1Mx16 SDRAMs store the upper significant bits of luminance Y[10:2] and colour difference C[10:2]. 4Mx4 SDRAM stores the lower significant bits Y[1:0] and C[1:0].



**Figure 3-12: Architecture of Memory Array with four 1Mx16 and one 4Mx4 SDRAMs**



All elements in the array can be simultaneously selected for command execution by activating the chip select signals or commands can be directed to a particular element in the array by activating the chip select signal for that element and deactivating the chip select signal for the others. [Figure 3-13: Memory Array Architecture with Four 4MX16 and One 16MX4 SDRAMs](#) shows the pin connections (and slightly different addressing requirements) needed for more common 64M SDRAMs within a memory array. The number of memories for a given format conversion remains the same independent of memory (16M or 64M) being used.



**Figure 3-13: Memory Array Architecture with Four 4MX16 and One 16MX4 SDRAMs**

To reduce system cost, the memory array architecture is made scalable. That is, when transposing smaller image sizes or when processing 8-bit images, a lesser number of SDRAMs per memory array are required.

[Table 3-5: Minimum SDRAM Configurations for Mode 8 \(default mode\)](#) shows the memory requirements for various format conversions.

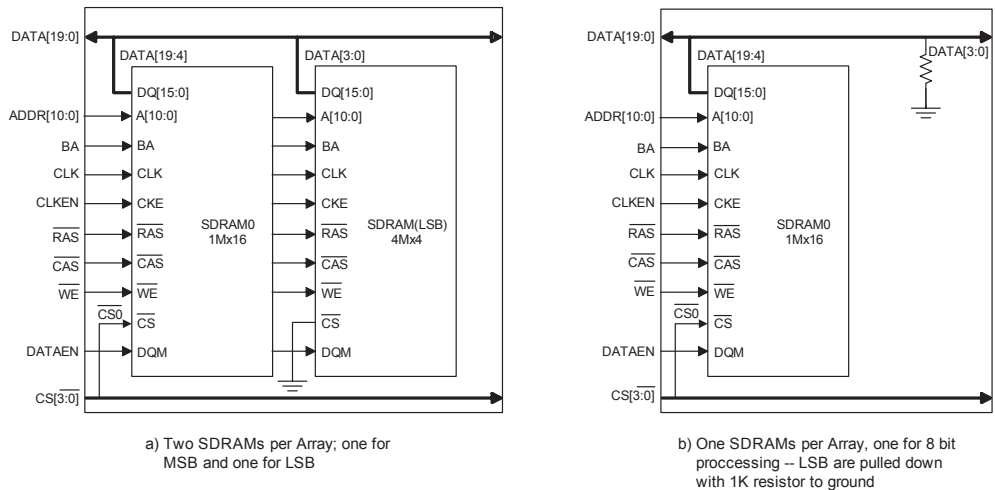


**Table 3-5: Minimum SDRAM Configurations for Mode 8 (default mode)**

Image Width (max) x max (Input Image Height, Output Image Height) <sup>a</sup>	Number of SDRAMs required / ARRAY		Download Parameters			
	[Y, C] 10-bits	[Y, C] 8-bits	MDL <sup>b</sup>	MCL <sup>c</sup>	MDR <sup>d</sup>	MCR <sup>e</sup>
2048 x 2048	4 (1Mx16) and 1 (4Mx4)	4 (1Mx16)	0	00	0	00
2048 x 1536	3 (1Mx16) and 1 (4Mx4)	3 (1Mx16)	0	01	0	01
2048 x 1024	2 (1Mx16) and 1 (4Mx4)	2 (1Mx16)	0	10	0	10
2048 x 512	1 (1Mx16) and 1 (4Mx4)	1 (1Mx16)	0	11	0	11

- a. max(a, b) = a when a >= b, else b when a < b.
- b.MDL stands for the parameter MODE\_16\_LEFT.
- c.MCL stands for the parameter MEM\_CONFIG\_LEFT.
- d.MDR stands for the parameter MODE\_16\_RIGHT.
- e.MCR stands for the parameter MEM\_CONFIG\_RIGHT.

**Figure 3-14: Architecture of Memory Array with Lesser Number of SDRAMs per Array** shows the memory array architecture when the number of memories is reduced to 2 SDRAMs and one SDRAM (8 bit processing) per memory array.



**Figure 3-14: Architecture of Memory Array with Lesser Number of SDRAMs per Array**



### 3.5.2 SDRAM Specifications

The speed grade of the SDRAM is chosen depending on the processing clock frequency. For example, if the processing clock is running at 74.25MHz, SDRAM with a speed grade of -10 or 100MHz should be selected.

### 3.5.3 Special Processing

#### 3.5.3.1 Model 16

To further decrease the memory requirements at the expense of processing time an additional mode is available. [Table 3-6: Minimum SDRAM Configurations for Mode 16](#) summarizes the memory requirements for various format conversions in this mode.

**Table 3-6: Minimum SDRAM Configurations for Mode 16**

Image Width (max) x max (Input Image Height, Output Image Height) <sup>a</sup>	Number of SDRAMs required / ARRAY		Download Parameters			
	[Y, C] 10-bits	[Y, C] 8-bits	MDL <sup>b</sup>	MCL <sup>c</sup>	MDR <sup>d</sup>	MCR <sup>e</sup>
1024 x 2048	2 (1Mx16) and 1 (4Mx4)	2 (1Mx16)	1	10	1	10
1024 x 1024	1 (1Mx16) and 1 (4Mx4)	1 (1Mx16)	1	11	1	11

a.max (a, b) = a when a >= b, else b when a < b.

b.MDL stands for the parameter MODE\_16\_LEFT.

c.MCL stands for the parameter MEM\_CONFIG\_LEFT.

d.MDR stands for the parameter MODE\_16\_RIGHT.

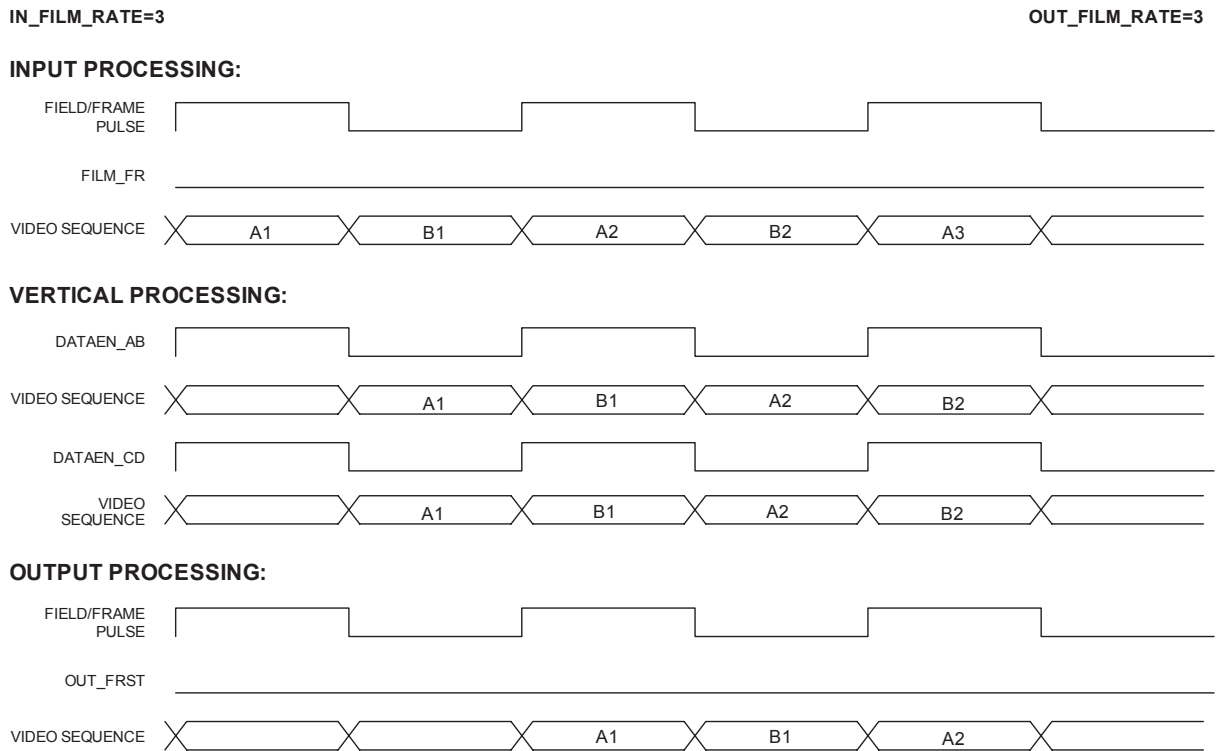
e.MCR stands for the parameter MEM\_CONFIG\_RIGHT.

### 3.5.4 Film Processing

During film processing the GF9320 uses the external signals FILM\_FR and OUT\_FRST to encode or decode the 3:2 pull-down sequence. The timing of these signals for different modes (film and non-film) is shown in [Figure 3-15: 60/60/60 Processing](#) through [Figure 3-40: 24p/24p/48p Processing](#). When the input video is from a film material with 3:2 pull-down, the GF9320 processes the image vertically after combining the even and odd fields to achieve better quality resizing. Duplicate fields in the input sequence are rejected by not writing into the memory. Note that in film modes memory switching does not occur at every field / frame boundary. It depends on the input and output film formats. For example, when the input is video with 3:2 pull-down, the left array of memories switch only after even and odd fields have been put together. The switching point is shown in the timing diagram by DATAEN\_AB and DATAEN\_CD signals that are, respectively, the output enable signals for left and right arrays. The GF9320 achieves 3:2 pull-down at the output by separately reading out the even and odd fields.



The film sequences shown in [Figure 3-15: 60/60/60 Processing](#) through [Figure 3-40: 24p/24p/48p Processing](#) are not the only film frame sequences that the GF9320 can generate. Note that an X through an input video sequence through [Figure 3-16: 30i/24p/24i Processing](#) to [Figure 3-34: 48p/24p/24p Processing](#) denotes a discarded frame when performing 3:2 pulldown compensation. Other input / output film sequences are possible. The input control uses the rising edge of FILM\_FR to set the input film sequence and the film frame reset sent to the output controller. The first TRS V-bit after the rising edge of FILM\_FR marks the beginning of a 3:2 (starting with 3) or 2:2 film sequences.



**Figure 3-15: 60/60/60 Processing**

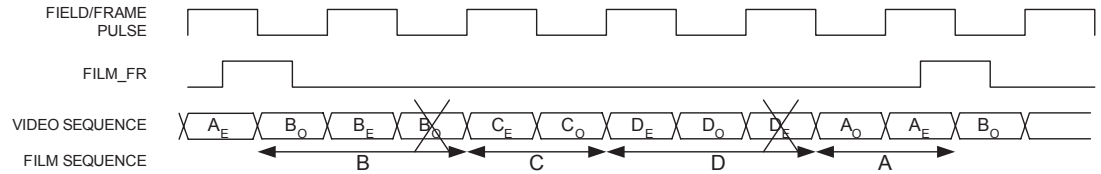




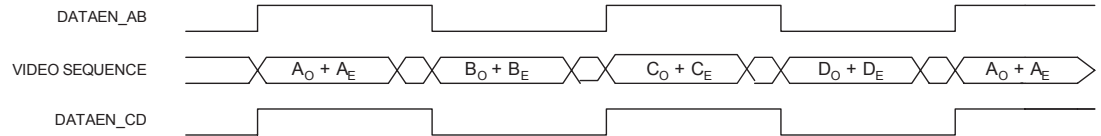
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=0

OUT\_FILM\_RATE=1  
OUT\_PROGRESSIVE=0

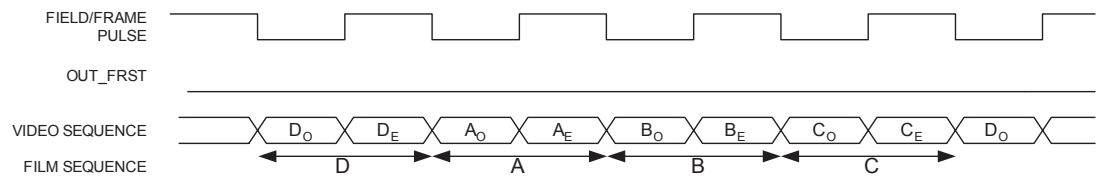
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

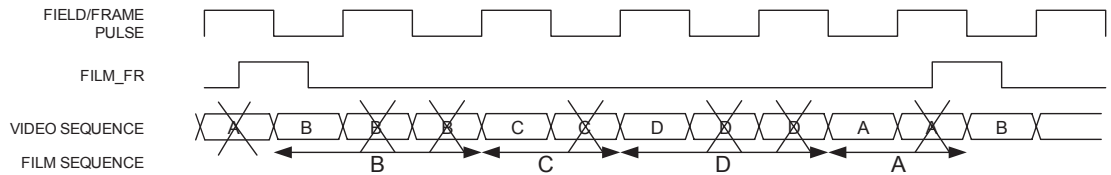


**Figure 3-16: 30i/24p/24i Processing**

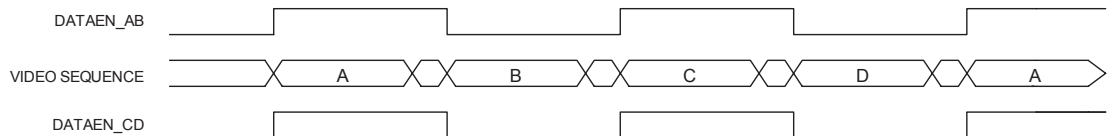
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=2  
OUT\_PROGRESSIVE=1

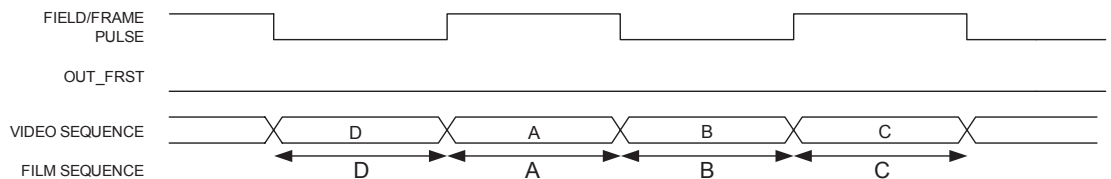
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



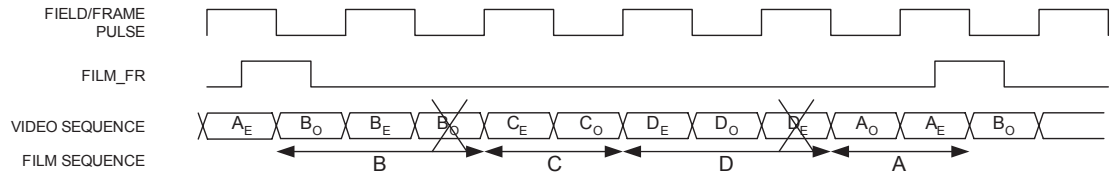
**Figure 3-17: 60p/24p/24p Processing**



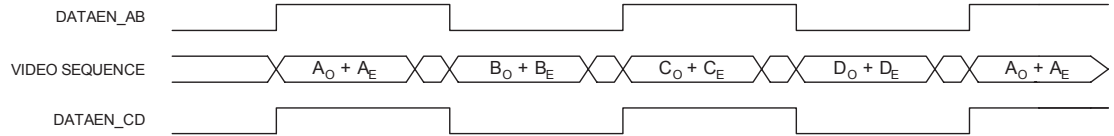
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=0

OUT\_FILM\_RATE=2  
OUT\_PROGRESSIVE=1

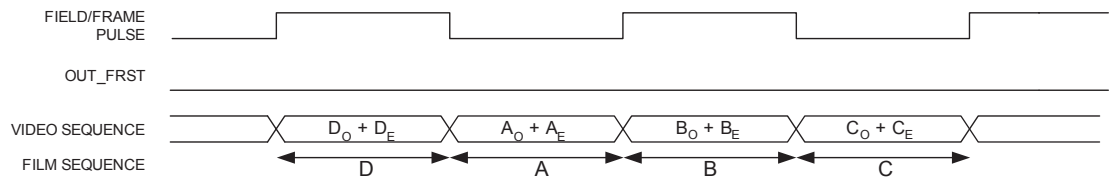
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

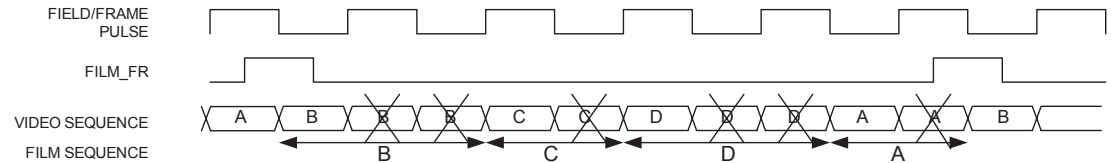


**Figure 3-18: 30i/24p/24p Processing**

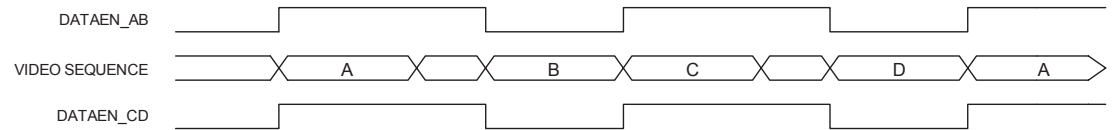
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=0

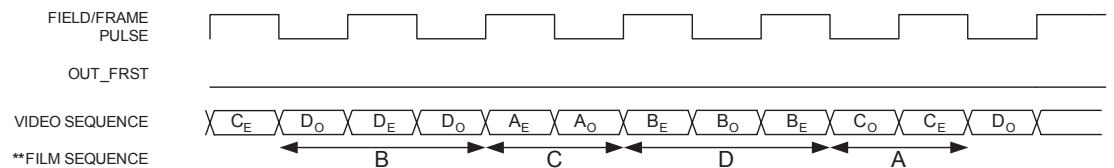
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



\*\*FILM SEQUENCE  
\*\* Film sequence is not maintained in the output.

**Figure 3-19: 60p/24p/30i Processing**

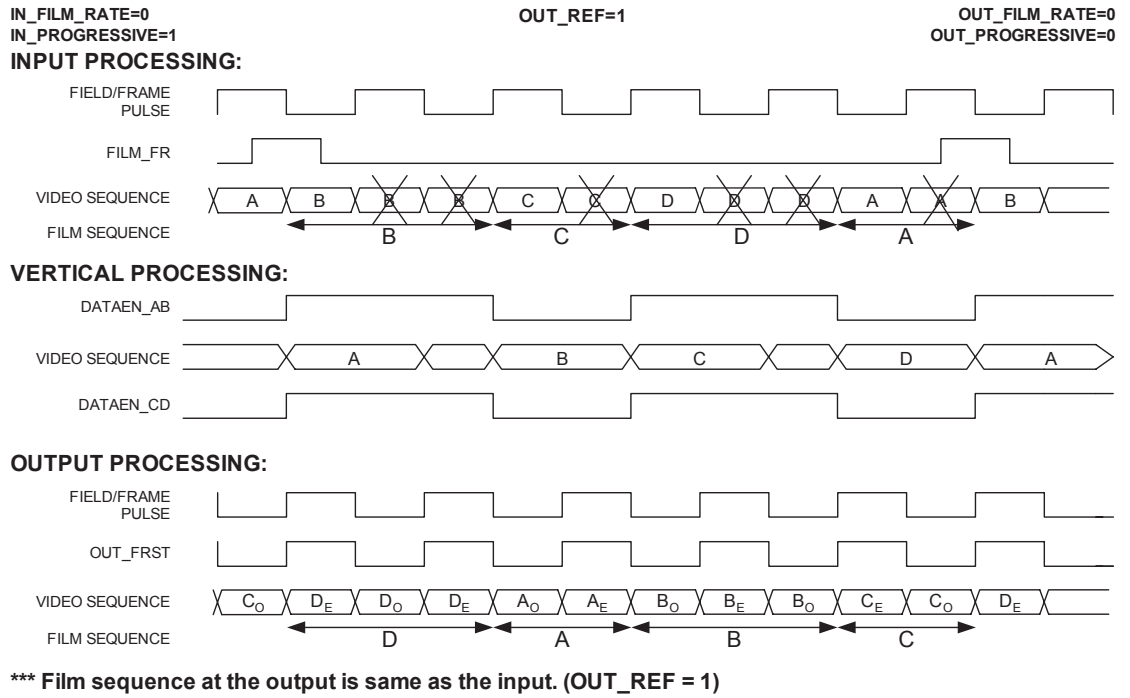


Figure 3-20: 60p/24p/30i (OUT\_REF=1) Processing

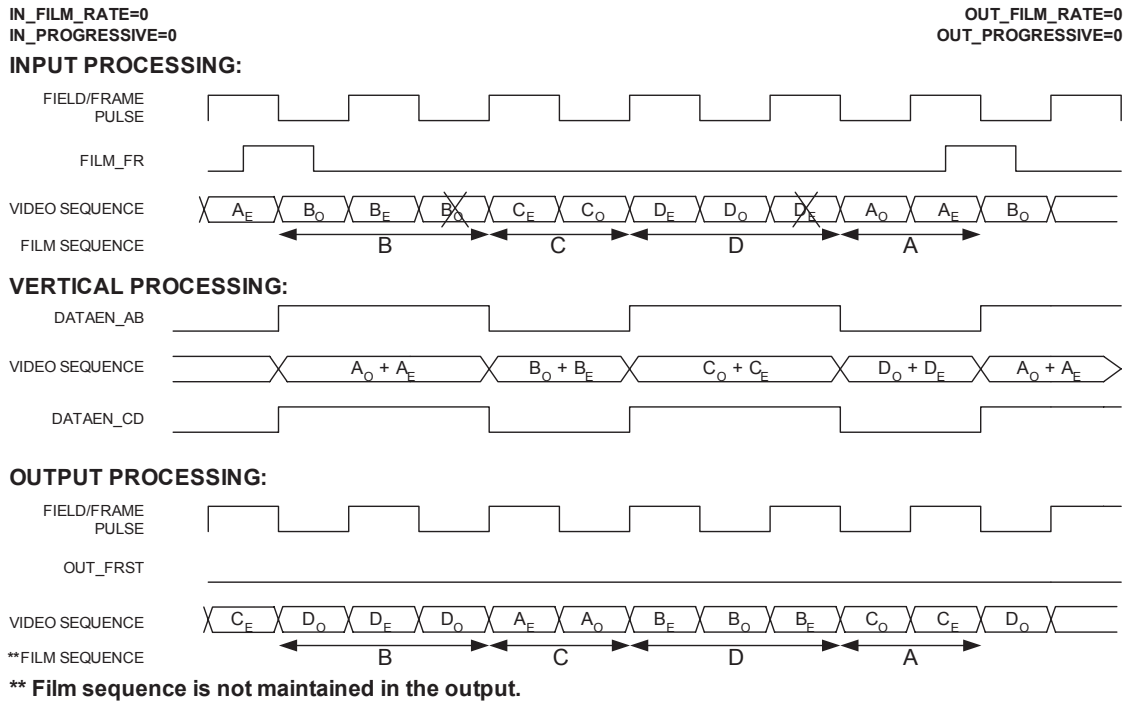


Figure 3-21: 30i/24p/30i Processing

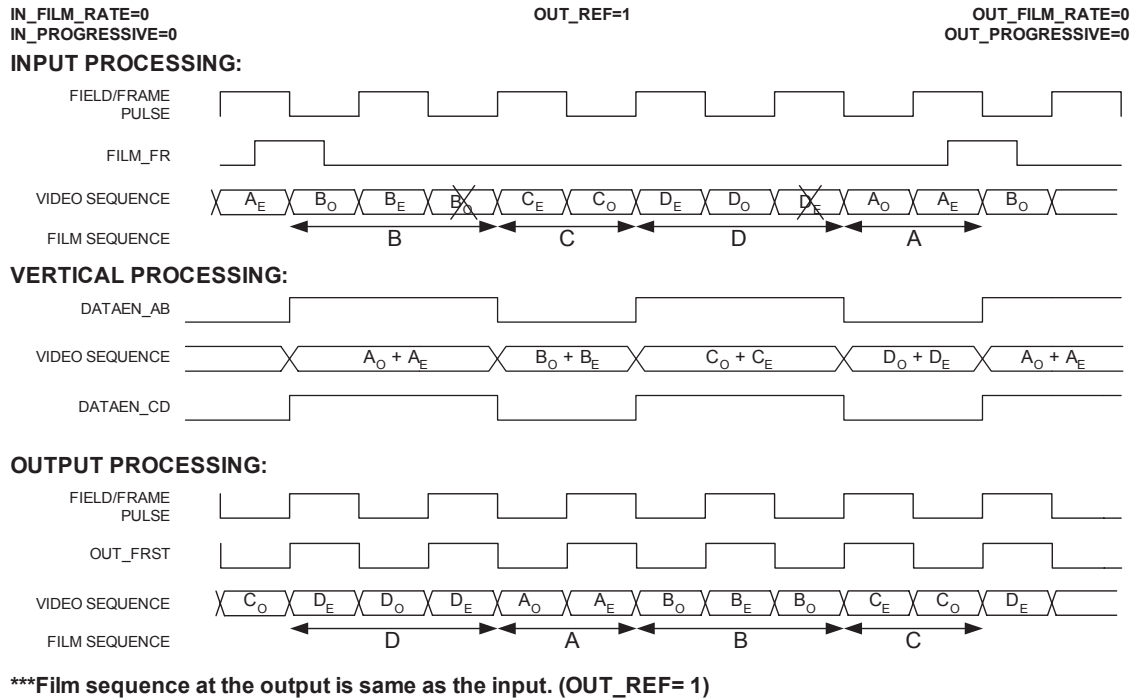


Figure 3-22: 30i/24p/30i (OUT\_REF=1) Processing

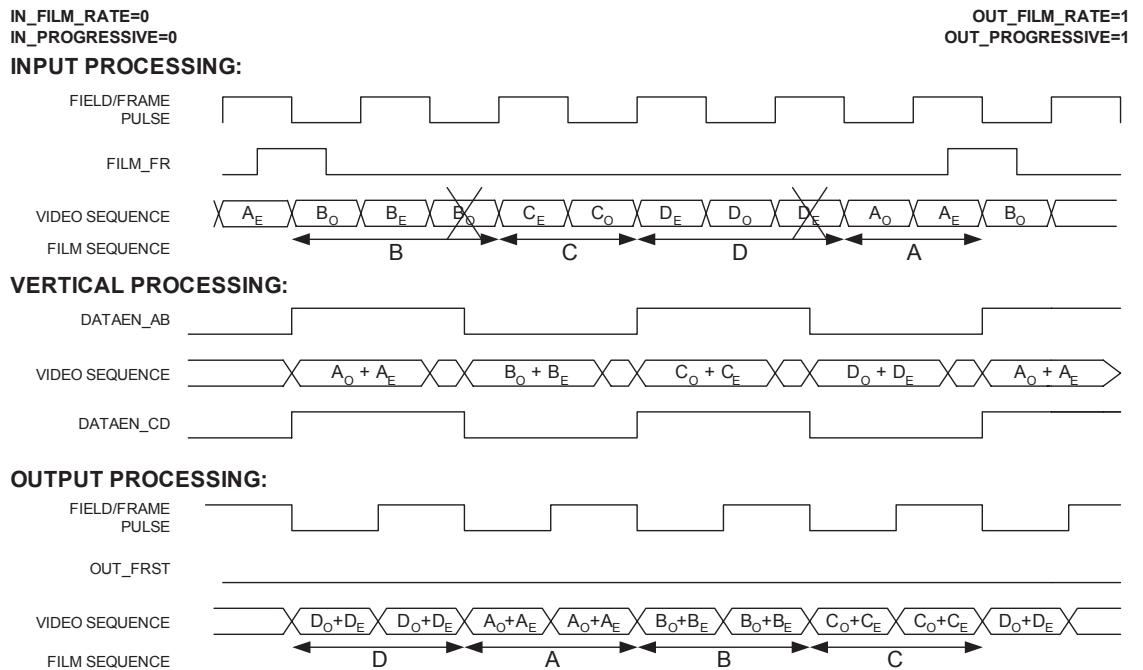


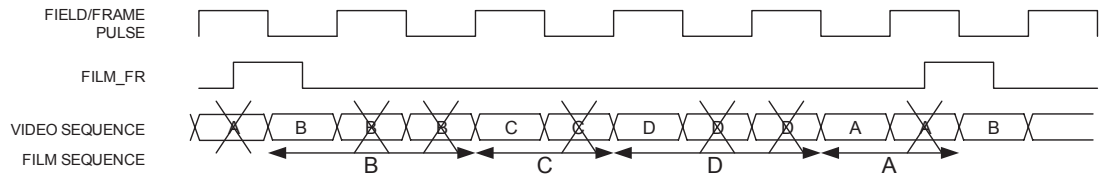
Figure 3-23: 30i/24p/48p Processing



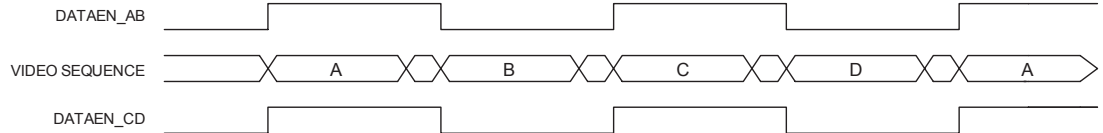
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=1  
OUT\_PROGRESSIVE=1

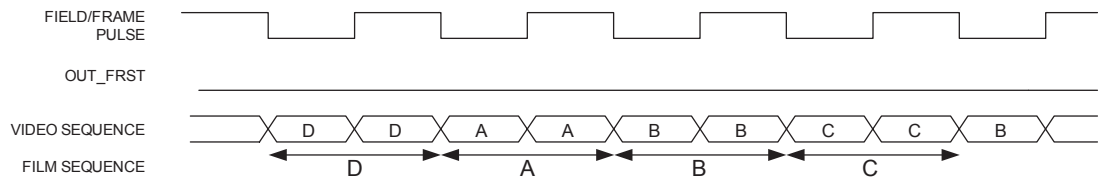
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

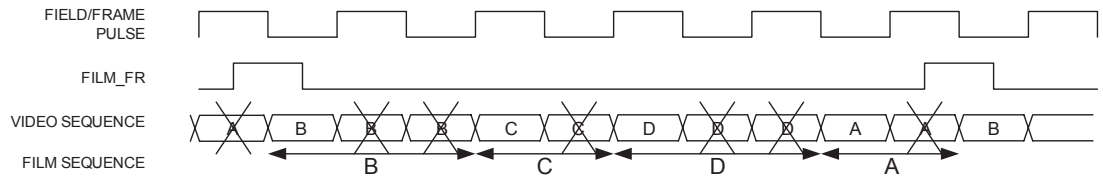


**Figure 3-24: 60p/24p/48p Processing**

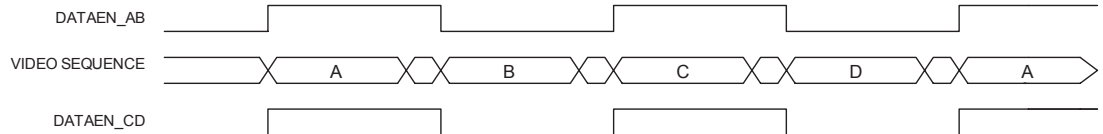
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=2  
OUT\_PROGRESSIVE=0

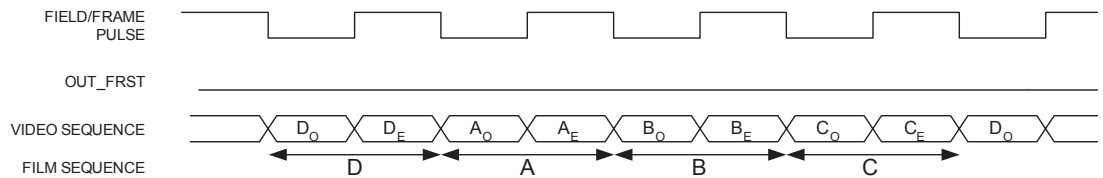
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



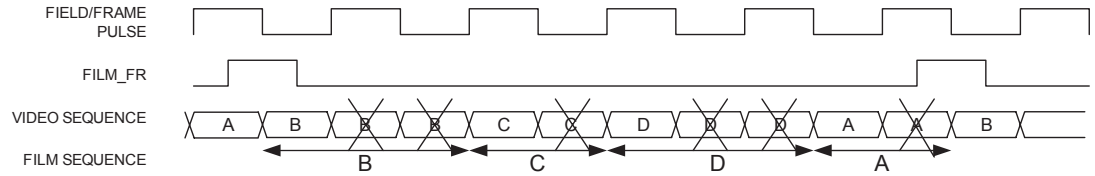
**Figure 3-25: 60p/24p/24i Processing**



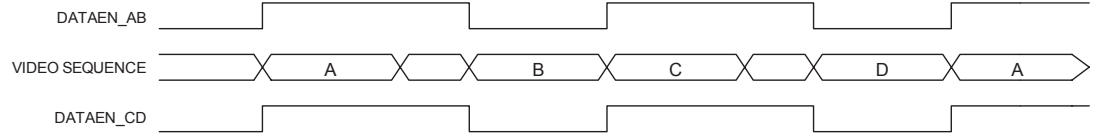
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=1

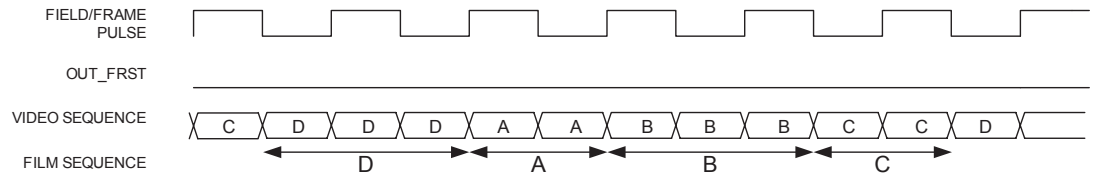
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

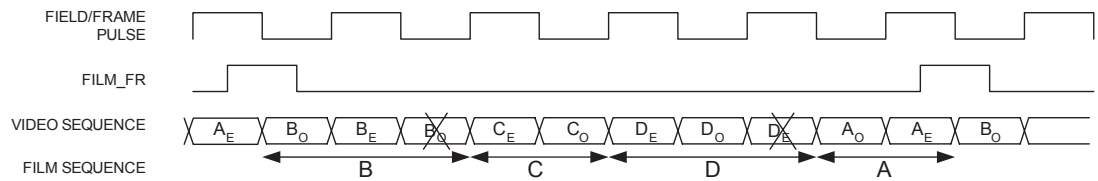


**Figure 3-26: 60p/24p/60p Processing**

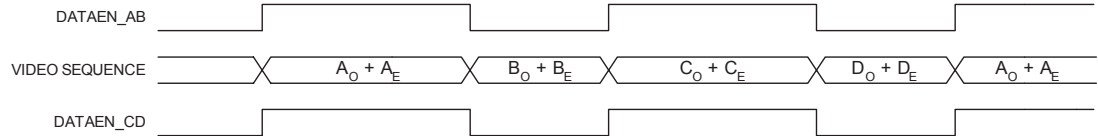
IN\_FILM\_RATE=0  
IN\_PROGRESSIVE=0

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=1

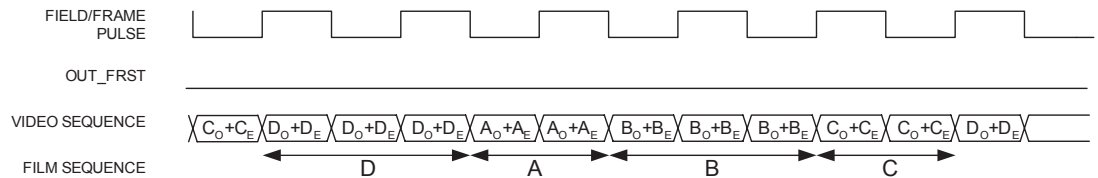
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



**Figure 3-27: 30i/24p/60p Processing**

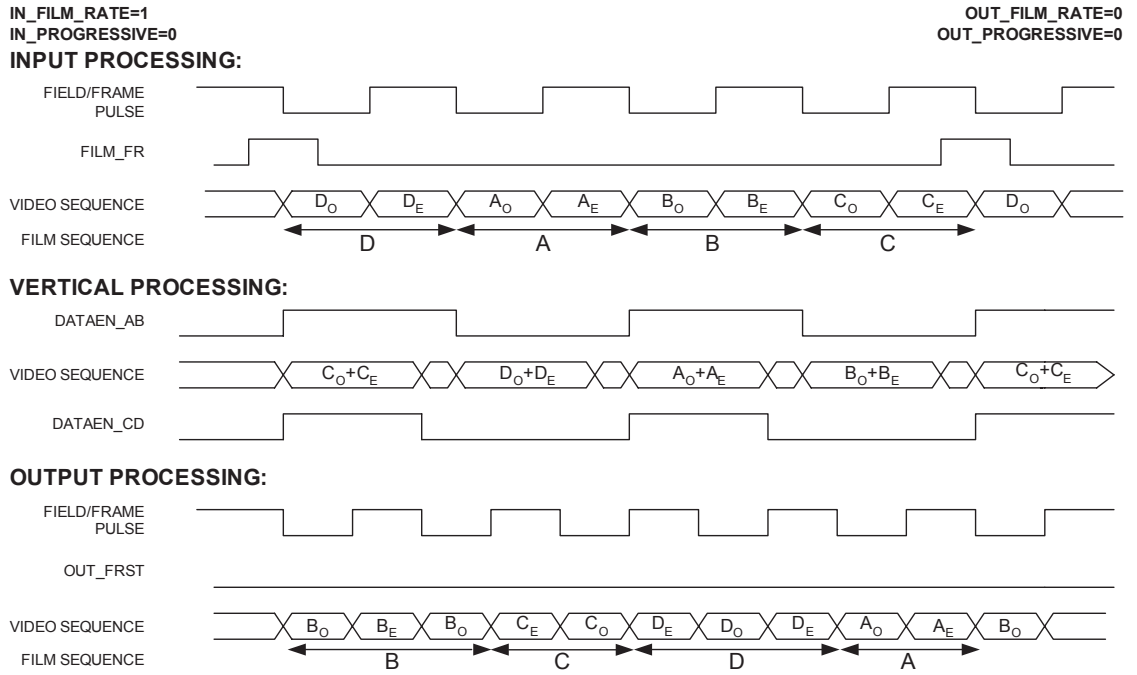


Figure 3-28: 24i/24p/30i Processing

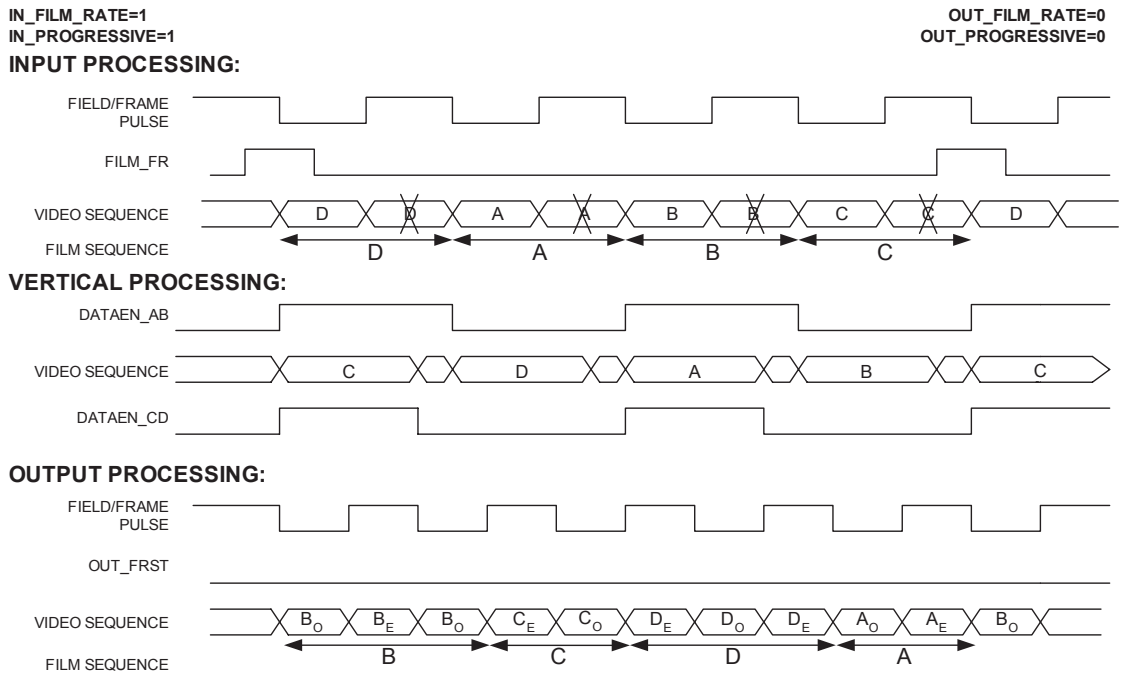


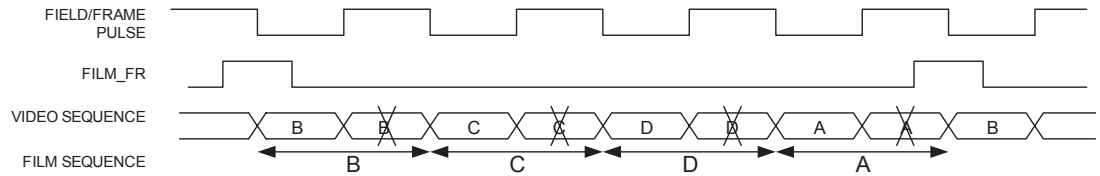
Figure 3-29: 48p/24p/30i Processing



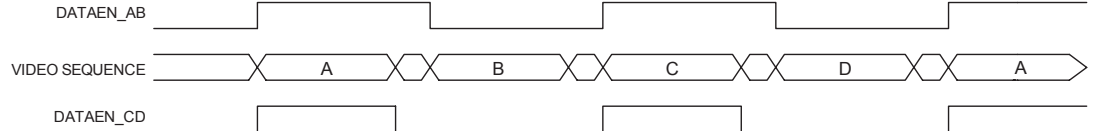
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=1

INPUT PROCESSING:



VERTICAL PROCESSING:



OUTPUT PROCESSING:

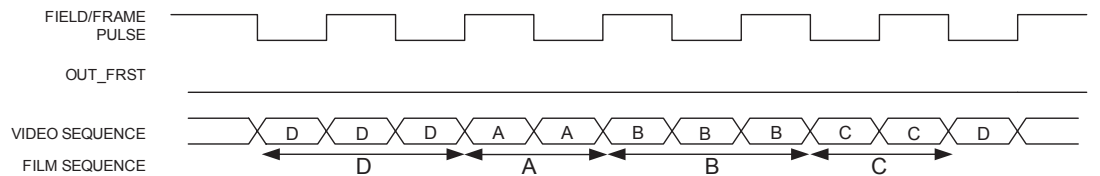
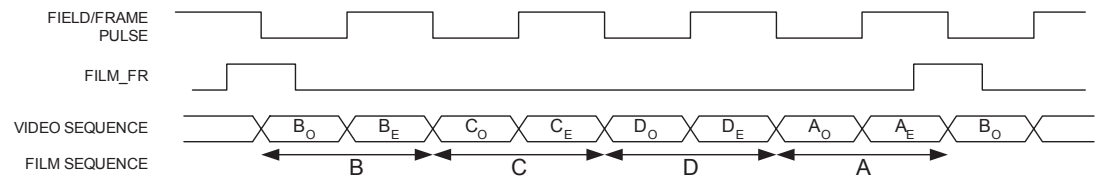


Figure 3-30: 48p/24p/60p Processing

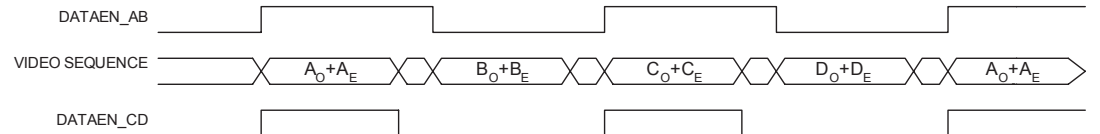
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=0

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=1

INPUT PROCESSING:



VERTICAL PROCESSING:



OUTPUT PROCESSING:

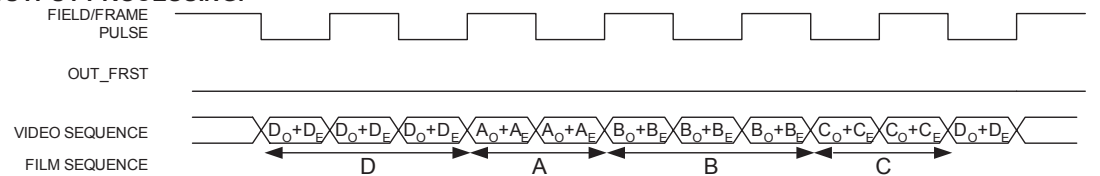


Figure 3-31: 24i/24p/60p Processing

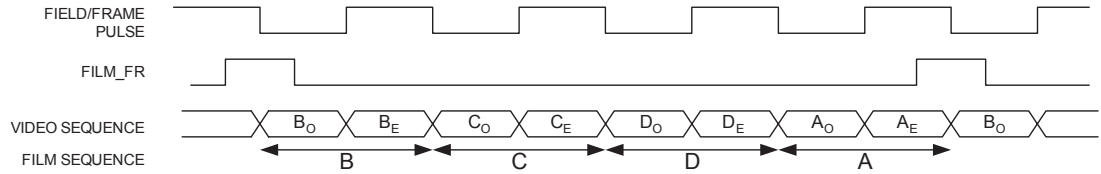




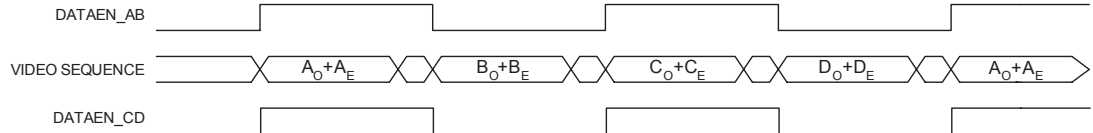
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=0

OUT\_FILM\_RATE=1  
OUT\_PROGRESSIVE=0

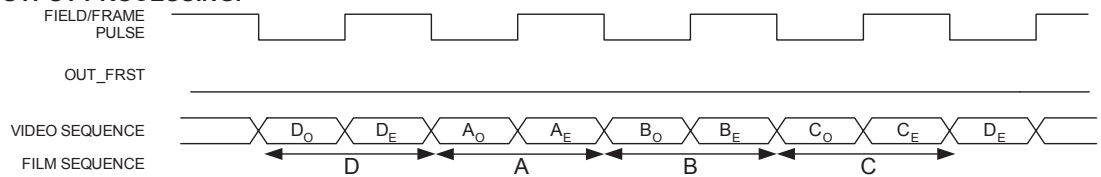
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

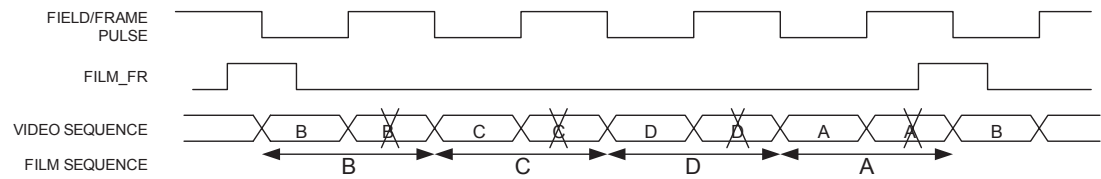


**Figure 3-32: 24i/24p/24i Processing**

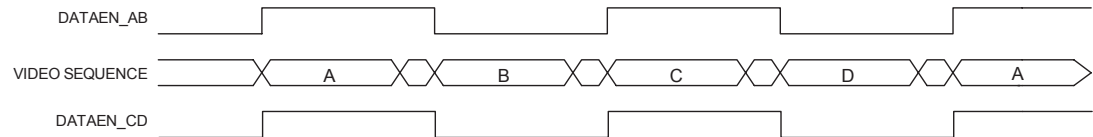
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=1  
OUT\_PROGRESSIVE=0

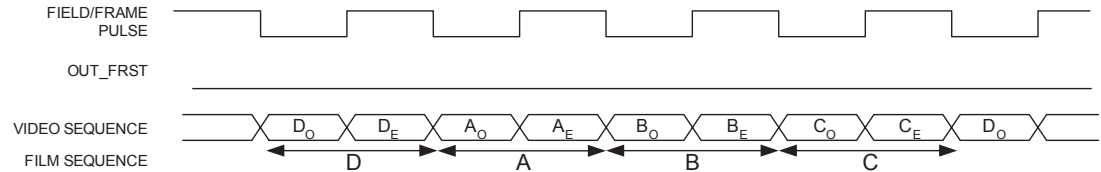
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



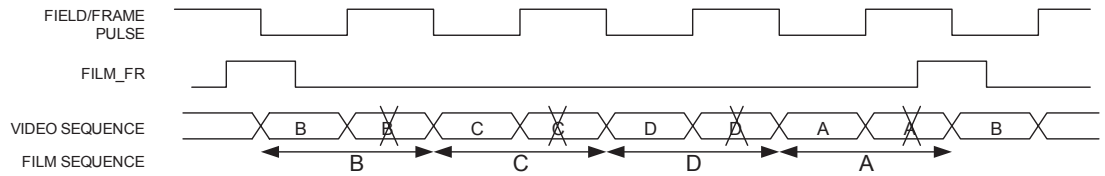
**Figure 3-33: 48p/24p/24i Processing**



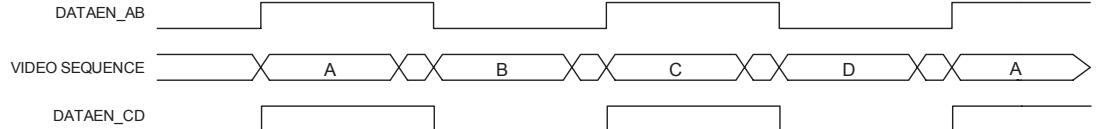
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=2  
OUT\_PROGRESSIVE=1

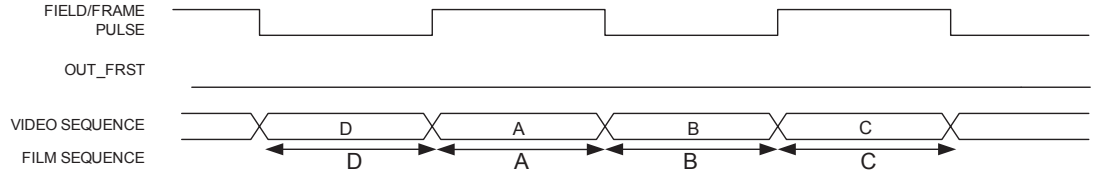
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

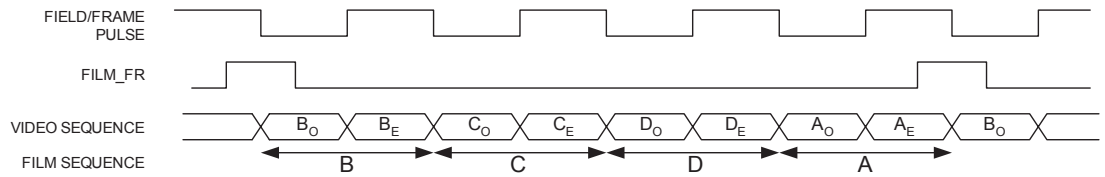


**Figure 3-34: 48p/24p/24p Processing**

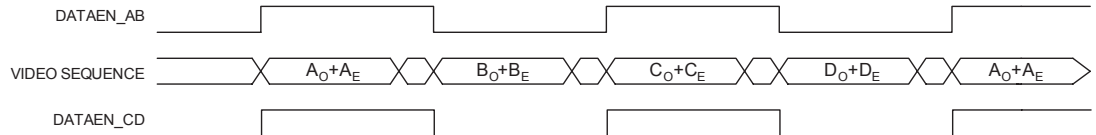
IN\_FILM\_RATE=1  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=2  
OUT\_PROGRESSIVE=1

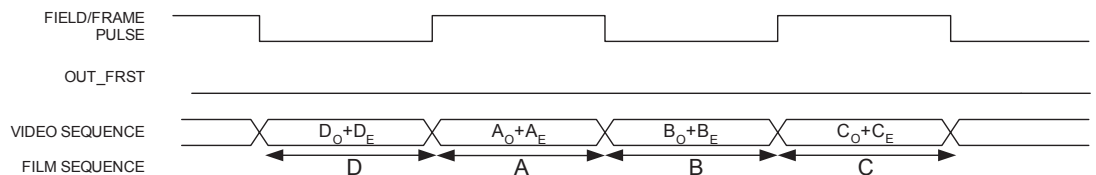
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



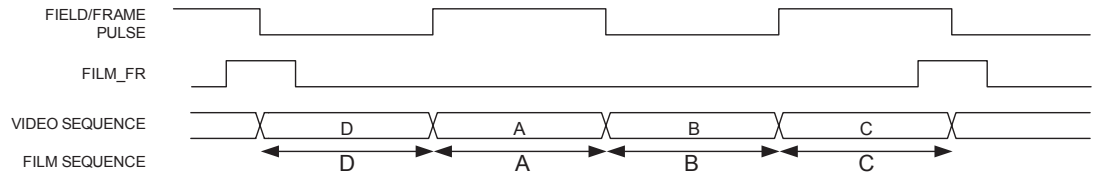
**Figure 3-35: 24i/24p/24p Processing**



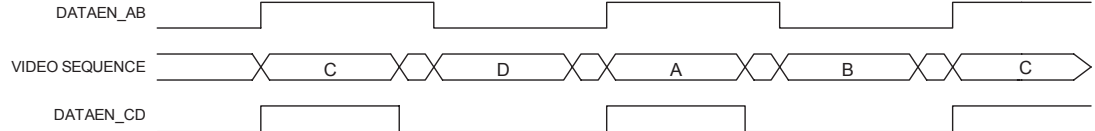
IN\_FILM\_RATE=2  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=0  
OUT\_PROGRESSIVE=0

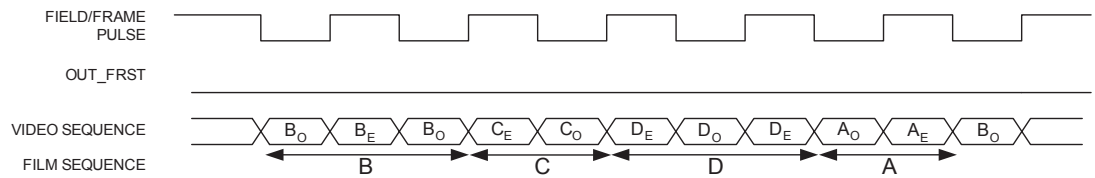
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**

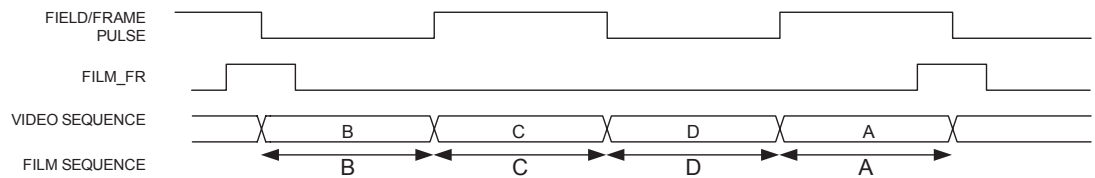


**Figure 3-36: 24p/24p/30i Processing**

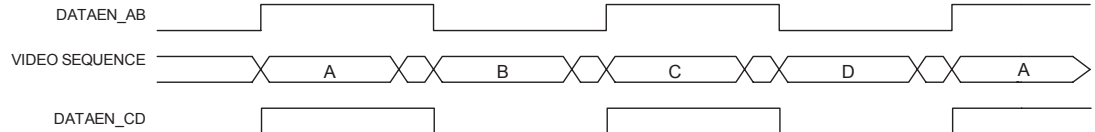
IN\_FILM\_RATE=2  
IN\_PROGRESSIVE=1

OUT\_FILM\_RATE=1  
OUT\_PROGRESSIVE=0

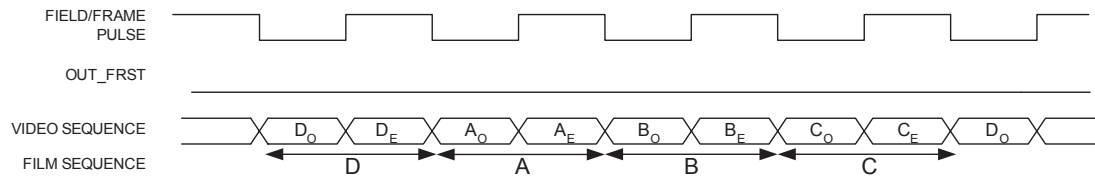
**INPUT PROCESSING:**



**VERTICAL PROCESSING:**



**OUTPUT PROCESSING:**



**Figure 3-37: 24p/24p/24i Processing**

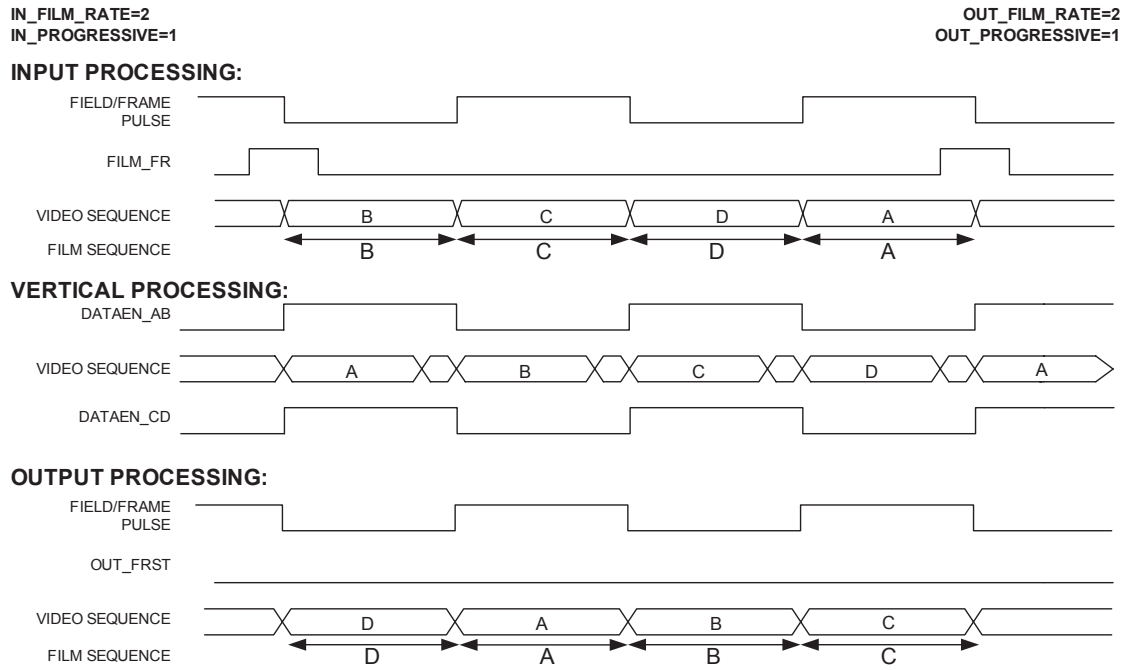


Figure 3-38: 24p/24p/24p Processing

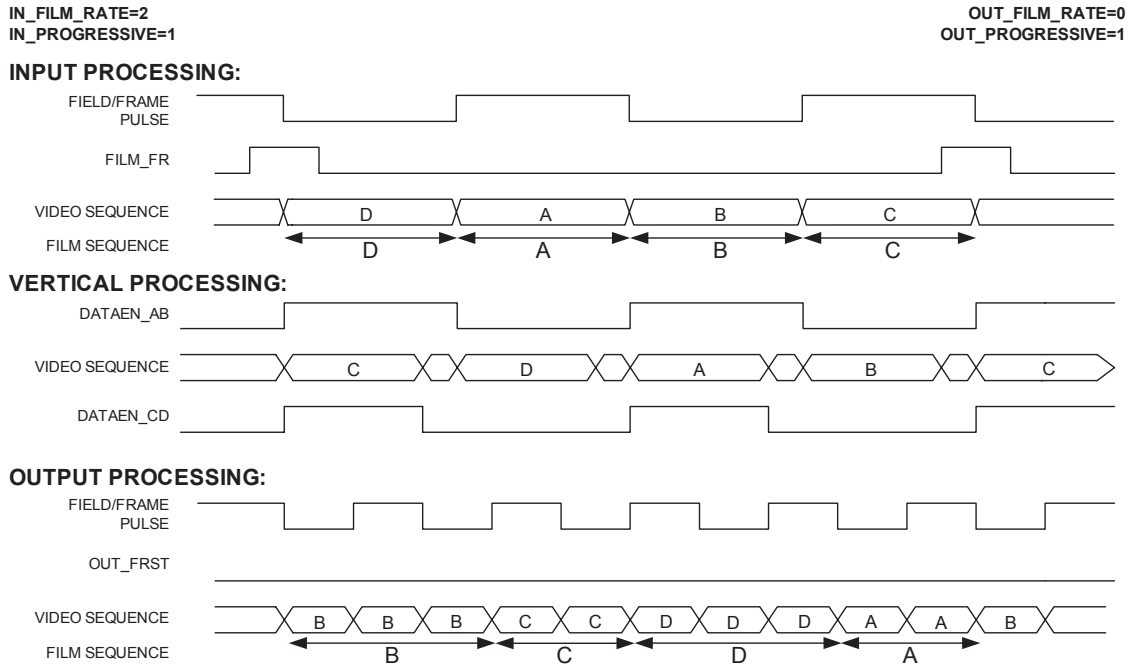
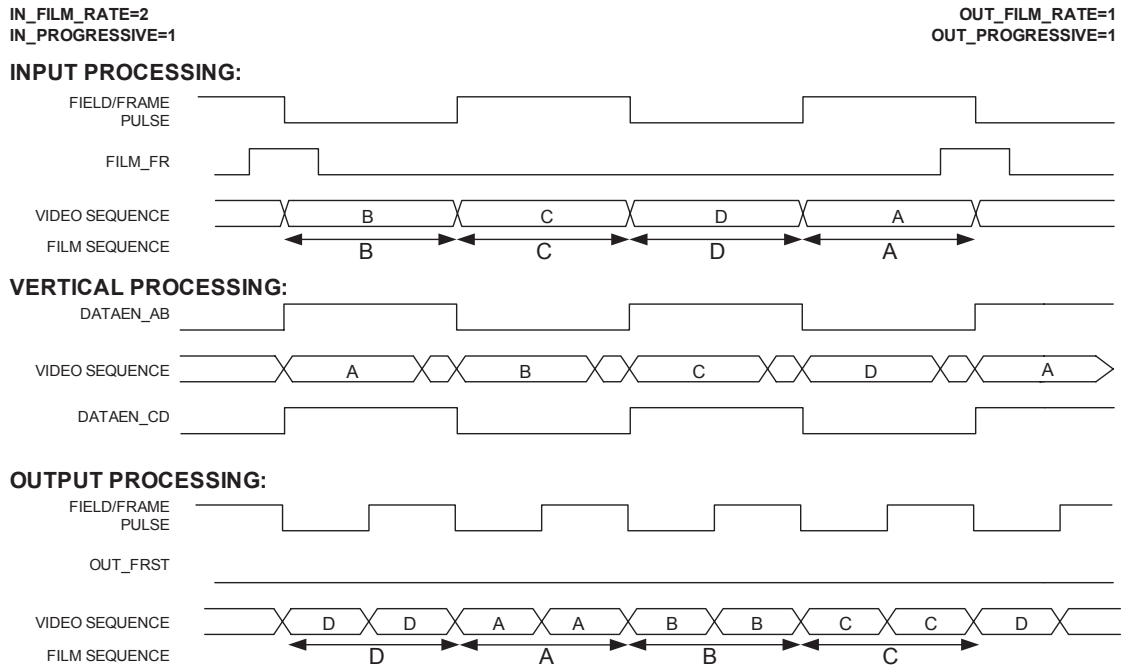


Figure 3-39: 24p/24p/60p Processing



**Figure 3-40: 24p/24p/48p Processing**

During film processing there is a possibility that for some conversions the GF9320 could violate the refresh period (64 ms) of the SDRAM. If a violation is found (IN\_REFR\_LEFT or OUT\_REFR\_RIGHT = '1'), then the appropriate (left / right) refresh bit should be activated in the download stream of parameters to the GF9320. Alternatively, [Table 3-7: Input and Output Formats Requiring Refresh](#) can be used to determine which input and output formats require refresh bits to be active.

**Table 3-7: Input and Output Formats Requiring Refresh**

Input Format IN_REFR_LEFT=1	Output Format OUT_REFR_RIGHT=1
24p/25p	24p/25p
48p/50p	
30i/60p with 3:2 pull-down	



### 3.5.5 Processing Delay

Processing delay for video through the GF9320 depends on the conversion. [Table 3-8: Processing Delay for Various Conversions](#) shows the processing delay for different film and non-film modes.

**Table 3-8: Processing Delay for Various Conversions**

Conversion	Delay (Input Frames / Fields)
<b>[frame / field modes - 60Hz V processing]</b>	
Note: All other frame rates are identical with appropriate time scaling	
30i → 30i	1/30 seconds (2 fields)
30i → 60p	1/30 seconds (2 fields)
60p → 30i	1/30 seconds (2 frames)
60p → 60p	1/30 seconds (2 frames)
<b>[2:2 modes - 30Hz V processing]</b>	
30i → 30p	1/15 seconds (4 fields)
60p → 30p	1/15 seconds (4 frames)
30p → 30i	1/15 seconds (2 frames)
30p → 60p	1/15 seconds (2 frames)
30i → 30i	1/15 seconds (4 fields)
30i → 60p	1/15 seconds (4 fields)
<b>[3:2 modes - 24Hz V processing]</b>	
30i → 30i	1/10-1/12 seconds (5-6 fields)
30i → 60p	1/10-1/12 seconds (5-6 fields)
30i → 24p	3/40-1/12 seconds (4.5-5 fields)
30i → 24i	3/40-1/12 seconds (4.5-5 fields)
60p → 24p	3/40-1/12 seconds (4.5-5 fields)
60p → 24i	3/40-1/12 seconds (4.5-5 fields)
24i → 30i	3/40-1/12 seconds (3.6-4 fields)
24i → 60p	3/40-1/12 seconds (3.6-4 fields)
24p → 30i	3/40-1/12 seconds (1.8-2 frames)
24p → 60p	3/40-1/12 seconds (1.8-2 frames)



### 3.5.6 Pin Descriptions

The GF9320 uses the transpose memory bus interface signals to communicate with external memory (SDRAMs). The GF9320 is the master device on the bus interface and it controls the timing of the address and data flow. Each signal in the bus interface is described as follows:

#### 3.5.6.1 Address Bus

##### **ADDR\_A[10:0], ADDR\_B[10:0], ADDR\_C[10:0], ADDR\_D[10:0]**

The address bus is shared by all the memories in the array. The address bus bit BA\_A (Bank Select) selects which bank is to be active in memory array. BA\_A low selects bank A and BA\_A high selects bank B within the memory. During a bank activate command cycle, ADDR\_A[10:0] defines the row address when sampled at the rising clock edge. During a read / write cycle, ADDR\_A[9:0] defines the column address when sampled at the rising clock edge. In addition to the column address ADDR\_A10 is used to invoke auto-precharge operation.

Similarly, ADDR\_B[10:0], ADDR\_C[10:0], ADDR\_D[10:0] form the address bus of memory arrays B, C and D respectively.

#### 3.5.6.2 Data Bus

##### **DATA\_A[19:0], DATA\_B[19:0], DATA\_C[19:0], DATA\_D[19:0]**

The data bus is bi-directional. Valid data is driven on the data bus by the GF9320 during write cycle, which is accepted back by the GF9320 during the read cycles. These cycles involve transfers of bursts of data between the SDRAM core and registers of GF9320. Luminance data Y[9:2] are available on DATA\_A/B/C/D[19:12] while least significant bits Y[1:0] are available on DATA\_A/B/C/D[3:2]. Colour difference data C[9:2] are available on DATA\_A/B/C/D[11:4] while least significant bits C[1:0] are available on DATA\_A/B/C/D[1:0].

#### 3.5.6.3 Command Bus

##### **[RAS\_A, CAS\_A, WE\_A], [RAS\_B, CAS\_B, WE\_B], [RAS\_C, CAS\_C, WE\_C], [RAS\_D, CAS\_D, WE\_D]**

These bus signals are asserted by the GF9320 when commands have to be executed on the SDRAM memory array A. Similarly, [RAS\_B, CAS\_B, WE\_B], [RAS\_C, CAS\_C, WE\_C] and [RAS\_D, CAS\_D, WE\_D] are asserted to execute commands on memory array B, C and D respectively. These signals are considered valid only if the respective  $\overline{CS}$  pin is low during the active edge of the clock.

**CKEN\_A, CKEN\_B, CKEN\_C, CKEN\_D**

CKEN\_A, CKEN\_B, CKEN\_C and CKEN\_D are used to drive memory arrays A, B, C and D respectively. CKEN input suspends data (i.e. read data remains valid and write data is inhibited) during an active read or write. The GF9320 activates CKEN\_A and CKEN\_B signals during field / frame write cycle to drop pixels. CKEN\_C and CKEN\_D are activated during field / frame read cycle to hold pixel values. These signals are considered valid only if the respective  $\overline{CS}$  pin is low during the active edge of the clock.

 **$\overline{CS\_A}[3:0]$ ,  $\overline{CS\_B}[3:0]$ ,  $\overline{CS\_C}[3:0]$ ,  $\overline{CS\_D}[3:0]$** 

The  $\overline{CS\_A}[3:0]$  signals from the GF9320 allows selection of individual or multiple SDRAMs within the memory array A. The appropriate SDRAM(s) is selected when the respective  $\overline{CS\_A}[3:0]$  pin is active low on the rising edge of clock.  $\overline{CS\_B}[3:0]$ ,  $\overline{CS\_C}[3:0]$  and  $\overline{CS\_D}[3:0]$  select SDRAMs within memory arrays B, C and D respectively.

**DATAEN\_AB, DATAEN\_CD**

These signals are driven by the GF9320 only during start-up to prevent data contention. When sampled high, it places the data bus buffers within the SDRAM in a high impedance state. After successful initialization, DATAEN\_AB and DATAEN\_CD stay low until the next power-up reset. DATAEN\_AB is shared by memories in banks A and B, while DATAEN\_CD is shared by memories in banks C and D.

**CK\_A, CK\_B, CK\_C, CK\_D**

CK\_A, CK\_B, CK\_C and CK\_D are clock signals, which drive the SDRAMs clock pins in memory array A, B, C and D respectively.



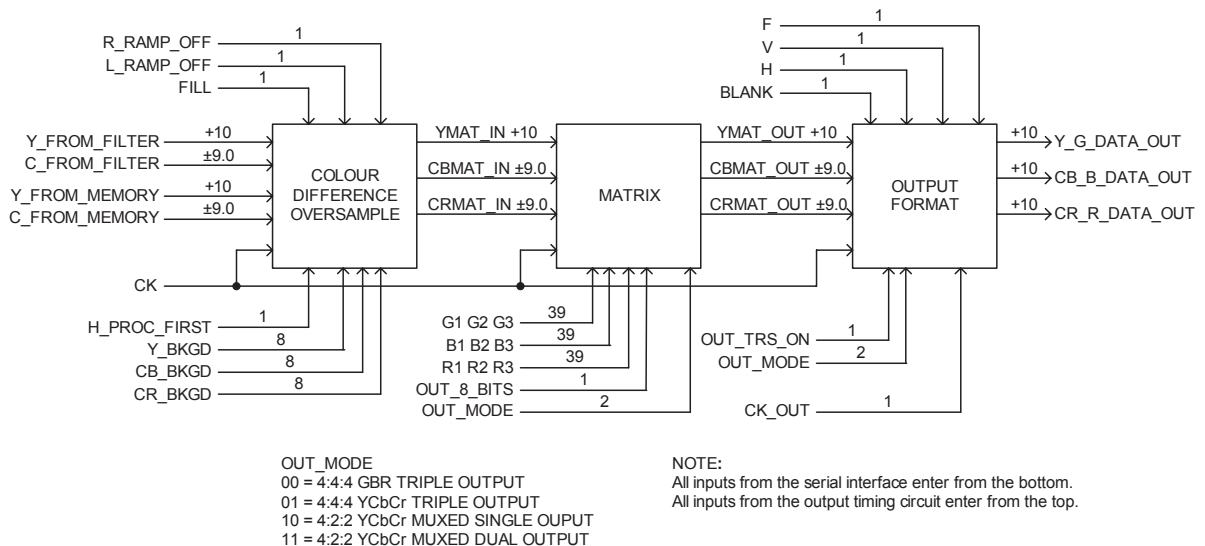


### 3.6 Output Processor

A block diagram of the output processor is shown in [Figure 3-41: Output Processor Block Diagram](#). The output processor consists of three major functions:

1. Colour difference over-sample
2. Matrix conversion
3. Output format

The colour difference over-sample function is necessary for colour matrix conversion and to provide a 4:4:4 output. The colour difference over-sample block also performs colour background insertion and horizontal edge shaping. Horizontal edge shaping is done to eliminate overshoot on edges when the scaled output does not fill the entire output raster. That is, when OUT\_HSTART is greater than 0 for left edge shaping and when OUT\_HSTOP is less than OUT\_HLEN\_ACT for right edge shaping. A programmable flat matte colour background is inserted into the output non-live video. Note that the colour background is inserted prior to the matrix conversion. This means that the downloaded background colour is in the input colour space coordinates.



**Figure 3-41: Output Processor Block Diagram**

The matrix block performs the following operations:

$$YMAT_{OUT} = \frac{G1 \cdot (YMAT_{IN} - 64) + G2 \cdot CBMAT_{IN} + G3 \cdot CRMAT_{IN}}{1024} + 64$$

$$PBMAT_{OUT} = \frac{B1 \cdot (YMAT_{IN} - 64) + B2 \cdot CBMAT_{IN} + B3 \cdot CRMAT_{IN}}{1024} + C_{OFFSET}$$



$$\text{PRMAT}_{\text{OUT}} = \frac{\text{R1} \cdot (\text{YMAT}_{\text{IN}} - 64) + \text{R2} \cdot \text{CBMAT}_{\text{IN}} + \text{R3} \cdot \text{CRMAT}_{\text{IN}}}{1024} + \text{C}_{\text{OFFSET}}$$

where  $\text{YMAT}_{\text{IN}}$ ,  $\text{CBMAT}_{\text{IN}}$  and  $\text{CRMAT}_{\text{IN}}$  are the inputs to the matrix;  
 $\text{YMAT}_{\text{OUT}}$ ,  $\text{CBMAT}_{\text{OUT}}$  and  $\text{CRMAT}_{\text{OUT}}$  are the outputs of the matrix; and  
 $G1$ ,  $G2$ ,  $G3$ ,  $B1$ ,  $B2$ ,  $B3$ ,  $R1$ ,  $R2$  and  $R3$  are the matrix coefficients;  
 $\text{C}_{\text{OFFSET}}$  is given by

$$\text{C}_{\text{OFFSET}} = \begin{cases} 64 & \text{OUT\_MODE} = 0 \\ 512 & \text{otherwise} \end{cases}$$

and 1024 is the gain of the matrix.

The matrix coefficients provide +6dB of range for gain adjustments. The  $\text{C}_b$  and  $\text{C}_r$  components at the input to the matrix are in 2's complement format. The B and R components at the output of the matrix are unsigned in GBR output mode ( $\text{OUT\_MODE}=0$ ) and are offset binary in  $\text{YCbCr}$  output mode ( $\text{OUT\_MODE}=1, 2$  or  $3$ ). The matrix coefficients are completely programmable and are downloaded as described in the [3.2 Serial Interface Control](#).

The output format block formats the data into one, two or three channels according to the  $\text{OUT\_MODE}$  parameter and inserts the output format TRS. If TRS is enabled, the data is clipped to 4 and 1019 for 10-bits or 1 and 254 for 8-bits.

## 3.7 Output Timing Control

The output timing and control block determines the output video data timing. This block contains horizontal and vertical counters based on the output format parameters. The output timing is adjusted relative to the reference by using the  $\text{LINE\_ADV}$  and  $\text{H\_POS}$  parameters. The output reference is either the input TRS (if  $\text{OUT\_REF} = 0$ ) or the  $\text{OUT\_FRST}$  pin on the GF9320 (if  $\text{OUT\_REF} = 1$ ). This provides for internal or external lock capability. The  $\text{LINE\_ADV}$  parameter advances the output video data by  $\text{LINE\_ADV}$  output lines. The  $\text{H\_POS}$  parameter delays the output video data by  $\text{H\_POS}$  samples. The range of  $\text{H\_POS}$  is one output line or  $\text{OUT\_HLEN\_TOT}$  samples.

Only limited ranges of input / output timing relationships are available by using the GF9320. In general, there are 2 fields / frames of delay through the GF9320. It is not possible for the GF9320 to have an output timing relationship such that the last active output line occurs after the SDRAM field / frame switch point.



# 4. Package Dimensions

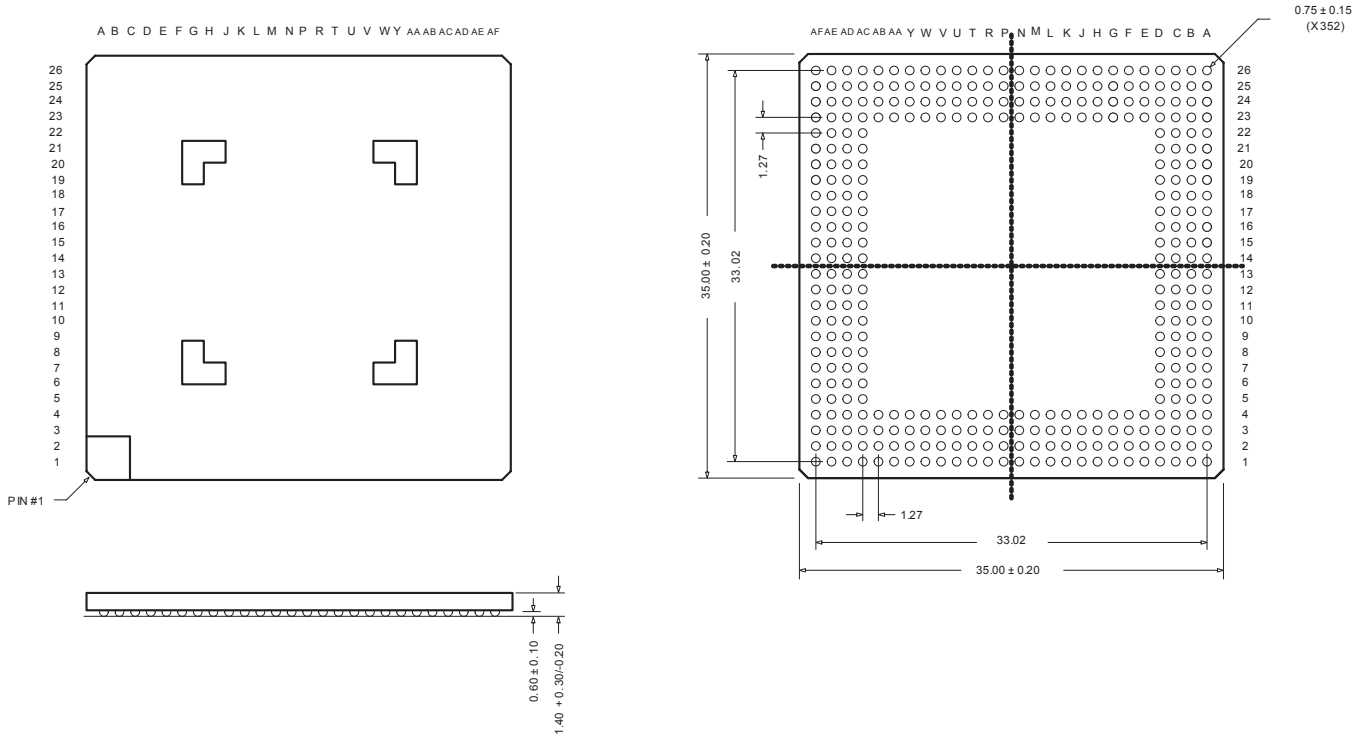


Figure 4-1: Package Dimensions



## 5. Revision History

Version	ECR	Date	Changes and / or Modifications
7	134925	November 2004	Corrections to address pins: ADDR_A[10:0], ADDR_B[10:0], ADDR_C[10:0], ADDR_D[10:0], BA_A, BA_B, BA_C and BA_D.
6	133502	June 2004	Changed BOUT description. Changed template.
5		November 2002	Add OUT_VLIVE issue and workaround - Change $\overline{\text{RST}}$ , $\overline{\text{SIF\_RST}}$ , $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ pin descriptions to active low. Make same changes throughout DS. -Make 60I->30i changes for consistency.
4		May 2002	Updating GF9320.
3		September 2001	Remove all "Preliminary & Confidential" water marks & references with the document.
2		July 2001	Correction required for both Figure 15 and the table titled "Output Signal Timing Specification".
1		June 2001	Correction to figure on page 2 & other improvements.
0		June 2001	Creating Preliminary Data Sheet.

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### GENNUM CORPORATION

Mailing Address: P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3

Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946

Shipping Address: 970 Fraser Drive, Burlington, Ontario, Canada L7L 5P5

### GENNUM JAPAN CORPORATION

Shinjuku Green Tower Building 27F, 6-14-1, Nishi Shinjuku, Shinjuku-ku,  
Tokyo, 160-0023 Japan

Tel. +81 (03) 3349-5501, Fax. +81 (03) 3349-5505

### GENNUM UK LIMITED

25 Long Garden Walk, Farnham, Surrey, England GU9 7HX

TEL. +44 (0)1252 747 000 FAX +44 (0)1252 726 523

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