Dual-Slot PCMCIA/CardBus Power Controllers

Features

- **Fully Integrated V_{CC} and V_{PP} Switching for Dual-Slot PC Card™ Interface**
- **Low $r_{DS(on)}$ (180-mΩ 5V V_{CC} Switch and 3.3V V_{CC} Switch)**
- **3.3V Low-Voltage Mode**
- **Meets PC Card Standards**
- **12V Supply Can Be Disabled Except During 12V Flash Programming**
- **Short Circuit and Thermal Protection**
- **28 Pin SSOP**
- **Compatible With 3.3V, 5V, and 12V PC Cards**
- **Break-Before-Make Switching**

Application

- **Notebook PC**
- **Electronic Dictionary**
- **Personal Digital Assistance**
- **Digital still Camera**

Description

The G576 PC Card power-interface switch provides an integrated power-management solution for dual-slot PC Cards. All of the discrete power MOSFETs, a logic section, current limiting, and thermal protection for PC Card control are combined on a single integrated circuit. The circuit allows the distribution of 3.3V, 5V, and/or 12V card power, and is compatible with many PCMCIA controllers. The current-limiting feature eliminates the need for fuses, which reduces component count and improves reliability. Current-limit reporting can help the user isolate a system fault to the PC Card.

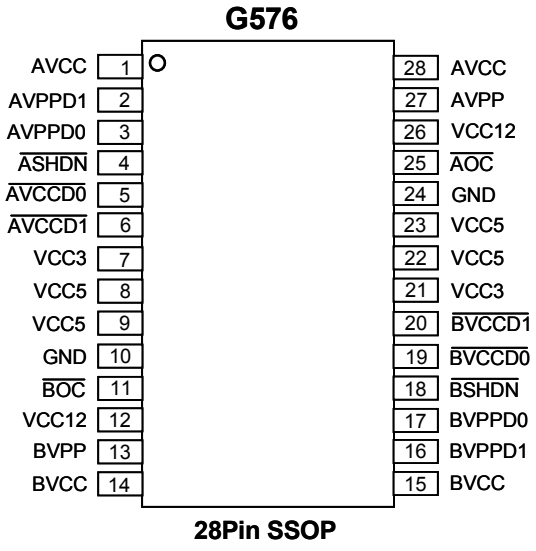
The G576 features a 3.3V low voltage mode that allows for 3.3V switching without the need for 5V. Bias power can be derived from either the 3.3V or 5V inputs. This facilitates low-power system designs such as sleep mode and pager mode where only 3.3V is available.

End equipment for the G576 includes notebook computers, desktop computers, personal digital assistants (PDAs), digital cameras and bar-code scanners.

Ordering Information

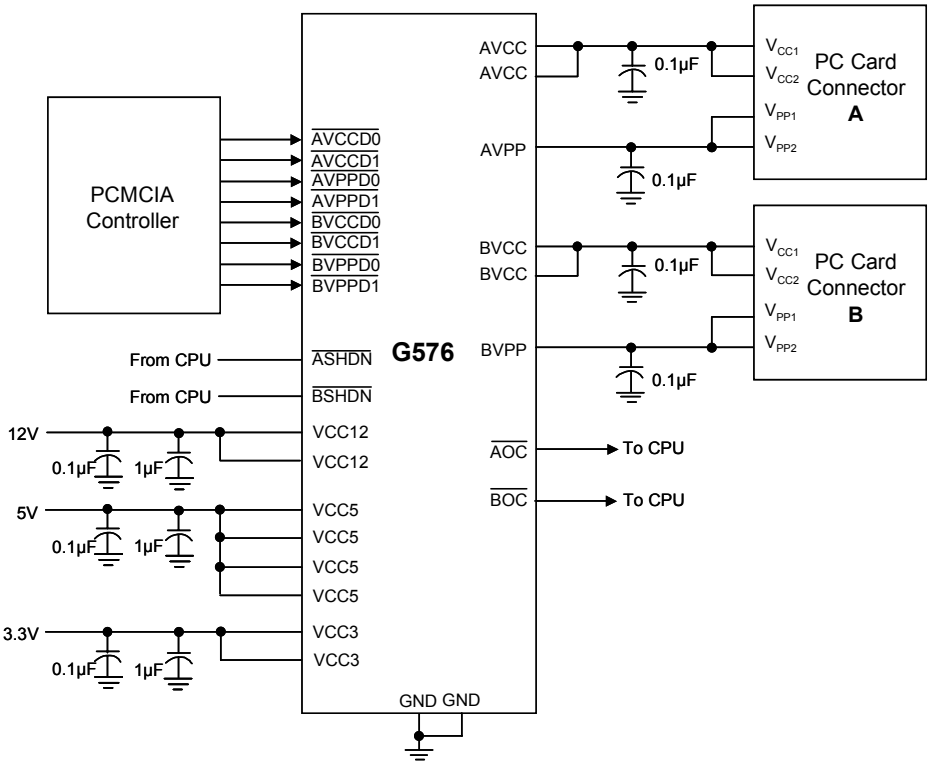
PART NUMBER	TEMP. RANGE	PACKAGE
G576	-40°C to +85°C	28-SSOP

Pin Configuration



28Pin SSOP

Typical PC-card Power-distribution application



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AVCC	1,28	O	Switched output that delivers 0V, 3.3V, 5V, or high impedance to card
AVPPD1	2	I	Logic input that controls voltage of AVPP (see control-logic table)
AVPPD0	3	I	Logic input that controls voltage of AVPP (see control-logic table)
$\overline{\text{ASHDN}}$	4	I	Logic input that shuts down AVPP/AVCC and sets AVPP/AVCC to high-impedance state
$\overline{\text{AVCCD0}}$	5	I	Logic input that controls voltage of AVCC (see control-logic table)
$\overline{\text{AVCCD1}}$	6	I	Logic input that controls voltage of AVCC (see control-logic table)
VCC3	7,21	I	3.3V V_{CC} input for card power and/or chip power if 5V is not present
VCC5	8,9,22,23	I	5V V_{CC} input for card power and/or chip power
GND	10,24		Ground
$\overline{\text{BOC}}$	11	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
VCC12	12,26	I	12V V_{PP} input card power
BVPP	13	O	Switched output that delivers 0V, 3.3V, 5V, 12V or high impedance to card
BVCC	14,15	O	Switched output that delivers 0V, 3.3V, 5V, or high impedance to card
BVPPD1	16	I	Logic input that controls voltage of BVPP (see control-logic table)
BVPPD0	17	I	Logic input that controls voltage of BVPP (see control-logic table)
$\overline{\text{BSHDN}}$	18	I	Logic input that shuts down BVPP/BVCC and set BVPP/BVCC to high-impedance state
$\overline{\text{BVCCD0}}$	19	I	Logic input that controls voltage of BVCC (see control-logic table)
$\overline{\text{BVCCD1}}$	20	I	Logic input that controls voltage of BVCC (see control-logic table)
$\overline{\text{AOC}}$	25	O	Logic-level overcurrent reporting output that goes low when an overcurrent condition exists
AVPP	27	O	Switched output that delivers 0V, 3.3V, 5V, 12V or high impedance to card

Absolute Maximum Ratings Over Operating Free-Air Temperature (unless other-wise noted)*

Input voltage range for card power:
VCC5.....-0.3V to 7V
VCC3.....-0.3V to 7V
VCC12.....-0.3V to 14V
Logic input voltage.....-0.3V to 7V
Output current (each card):$I_{O\ (AVCC/BVCC)}$.....internally limited
$I_{O(AVPP/BVPP)}$.....internally limited
Operating virtual junction temperature range, T_J.....-40°C to 150°C
Operating free-air temperature range,.T_A.....-40°C to 85°C
Storage temperature range, T_{STG}.....-55°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds.....260°C
Thermal resistance θ_{JA}
SSOP 28.....125°C/W
Power dissipation P_D ($T_A \leq +25°C$)
SSOP 28.....800mW
ESD.....Note1

*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress rating only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum-rated conditions for extended periods may affect device reliability.

Note 1: ESD (electrostatic discharge) sensitive device. Proper ESD precautions are recommended to avoid performance degradation or less of functionality.

Recommended Operating Conditions

		MIN	MAX	UNIT
Input voltage, V_I	VCC5	0	5.25	V
	VCC3	0	5.25	V
	VCC12	0	13.5	V
Output current	$I_{O\ (AVCC/BVCC)}$		1.0	A
	$I_{O\ (AVPP/BVPP)}$		150	mA
Operating virtual junction temperature, T_J		-40	125	°C

Electrical Characteristics (T_A=25°C)

Power Switch

PARAMETER		TEST CONDITIONS*	MIN	TYP	MAX	UNIT
Switch resistance	5V to AVCC/BVCC	VCC5 = 5V		130	180	mΩ
	3.3V to AVCC/BVCC	VCC5 = 5V, VCC3 =3.3V		130	180	
	3.3V to AVCC/BVCC	VCC5 = 0V, VCC3 =3.3V		130	180	
	5V to AVPP/BVPP	T_J = 25°C		3.6	6	Ω
	3.3V to AVPP/BVPP	T_J = 25°C		3.4	6	
	12V to AVPP/BVPP	T_J = 25°C		1.2	6	
$V_{O\ (AVPP/BVPP)}$ Clamp low voltage		I_{PP} at 10mA		0.18	0.8	V
$V_{O\ (AVCC/BVCC)}$ Clamp low voltage		I_{CC} at 10mA		0.13	0.8	V
I_{IKG} Leakage current	I_{PP} high-impedance State	T_A = 25°C		1	10	μA
	I_{CC} high-impedance State	T_A = 25°C		1	10	
I_I Input current	VCC5 = 5V	$V_{O\ (AVCC/BVCC)}$=5V, $V_{O\ (AVPP/BVPP)}$=12V		75	150	μA
	VCC5= 0V, VCC3 = 3.3V	$V_{O\ (AVCC/BVCC)}$=3.3V, $V_{O\ (AVPP/BVPP)}$=12V		75	150	
	Shutdown mode	$V_{O\ (AVCC/BVCC)}$=$V_{O\ (AVPP/BVPP)}$= Hi-Z		1	3	
I_{OS} Short-circuit Output-current Limit	$I_{O(AVCC/BVCC)}$	Output powered into a short to GND	0.8		2.2	A
	$I_{O(AVPP/BVPP)}$		120		400	mA

*Pulse-testing techniques maintain junction temperature close to ambient temperatures; thermal effects must be taken into account separately.

Logic Section

PARAMETER	TEST CONDITION*	MIN	MAX	UNIT
Logic input current			1	μA
Logic input high level		2		V
Logic input low level			0.8	V
Logic output high level	VCC5=5V, I_O=1mA	VCC5 -0.4		V
	VCC5=0V, I_O=1mA, VCC3=3.3V	VCC3 -0.4		
Logic output low level	I_O=1mA		0.4	V

*Pulse-testing techniques maintain junction temperature close to ambient temperatures; thermal effects must be taken into account separately.

Switching Characteristics **

PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
t_r Rise times, output	$V_{O\ (AVCC/BVCC)}$			2.6		ms
	$V_{O\ (AVPP/BVPP)}$			10		
t_f Fall times, output	$V_{O\ (AVCC/BVCC)}$			7.5		
	$V_{O\ (AVPP/BVPP)}$			38		
t_{pd} Propagation delay (see Figure 1)	V_I ($V_{(AVPPD0/BVPPD0)}$) to $V_{O\ (AVPP/BVPP)}$	t_{on}		14		ms
		t_{off}		44		
	V_I ($\overline{AVCCD1}$ / $\overline{BVCCD1}$) to $V_{O\ (AVCC/BVCC)}$ (3.3V)	t_{on}		3.2		
		t_{off}		17		
	V_I ($\overline{AVCCD0}$ / $\overline{BVCCD0}$) to $V_{O\ (AVCC/BVCC)}$ (5V)	t_{on}		4.4		
		t_{off}		20		

**Switching Characteristics are with C_L = 147μF.

§ Refer to Parameter Measurement Information

Parameter Measurement Information

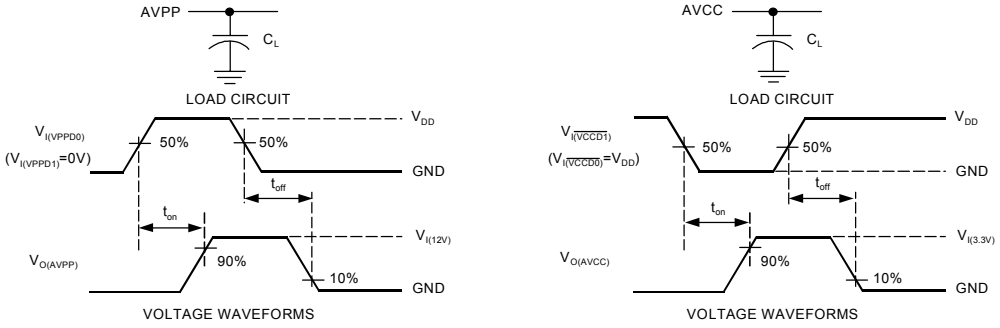


Figure 1. Test Circuits and Voltage Waveforms

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Parameter Measurement Information

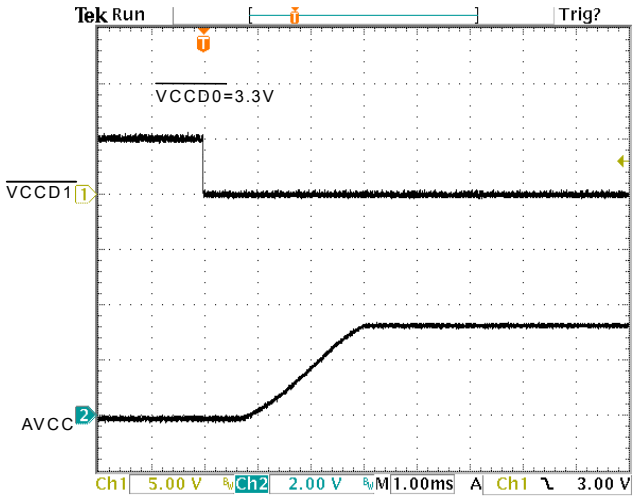


Figure 2. AVCC/BVCC Propagation Delay and Rise Time With 1μF Load, 3.3V Switch

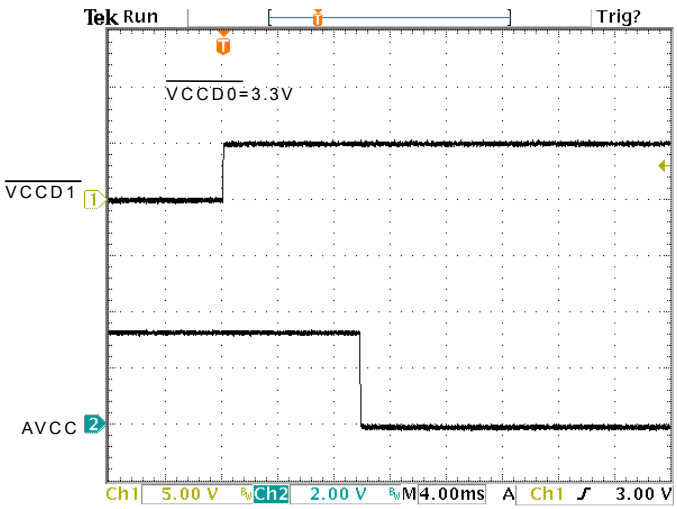


Figure 3. AVCC/BVCC Propagation Delay and Fall Time With 1μF Load, 3.3V Switch

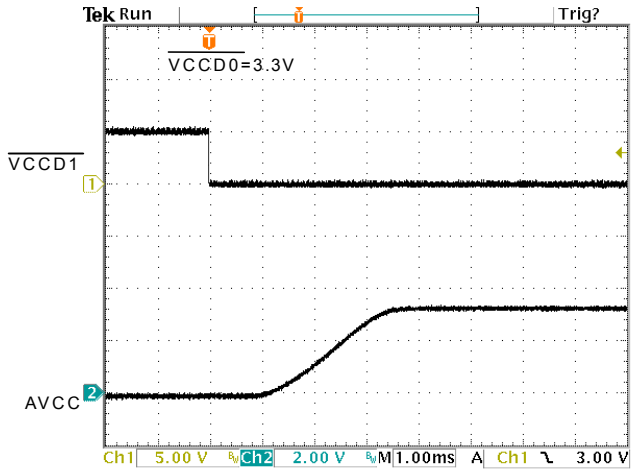


Figure 4. AVCC/BVCC Propagation Delay and Rise Time With 147μF Load, 3.3V Switch

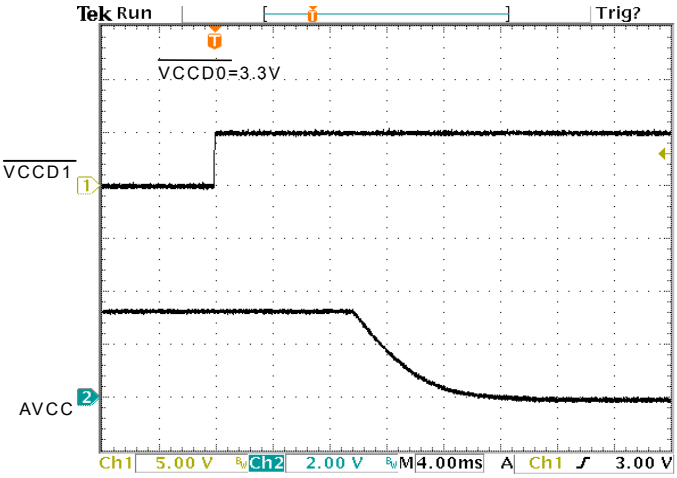


Figure 5. AVCC/BVCC Propagation Delay and Fall Time With 147μF Load, 3.3V Switch

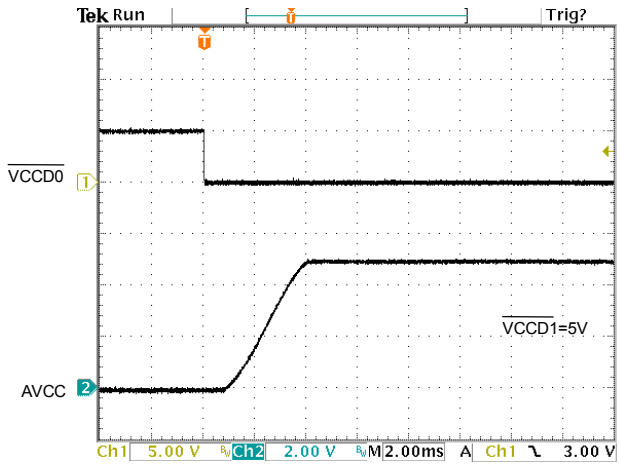


Figure 6. AVCC/BVCC Propagation Delay and Rise Time With 1µF Load, 5V Switch

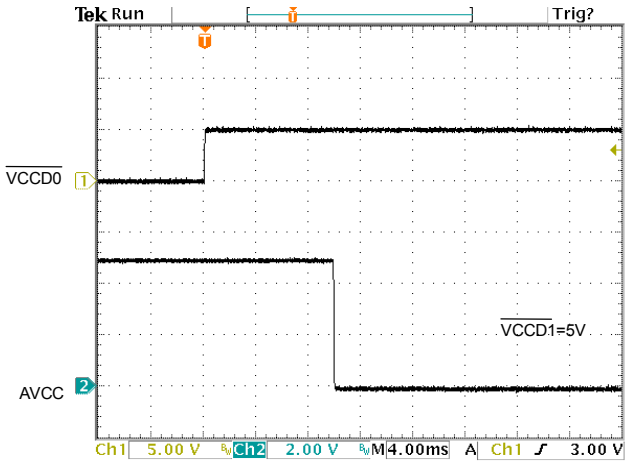


Figure 7. AVCC/BVCC Propagation Delay and Fall Time With 1µF Load, 5V Switch

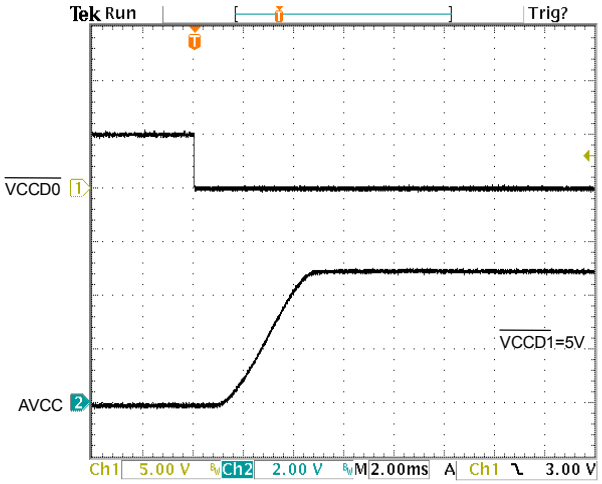


Figure 8. AVCC/BVCC Propagation Delay and Rise Time with 147µF Load, 5V Switch

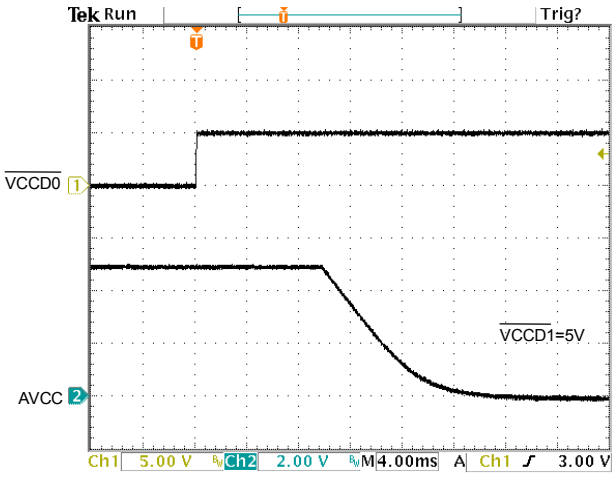


Figure 9. AVCC/BVCC Propagation Delay and Fall Time with 147µF Load, 5V Switch

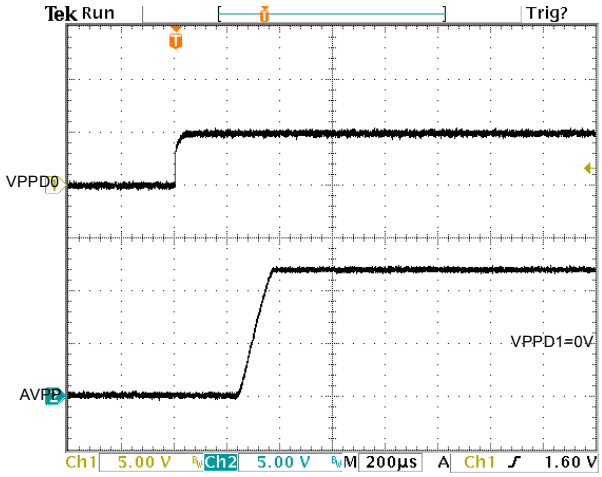


Figure 10. AVPP/BVPP Propagation Delay and Rise Time With 1µF Load, 12V Switch

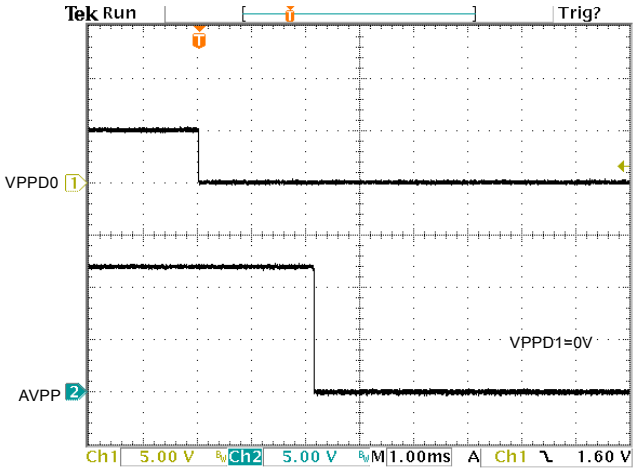


Figure 11. AVPP/BVPP Propagation Delay and Fall Time With 1µF Load, 12V Switch

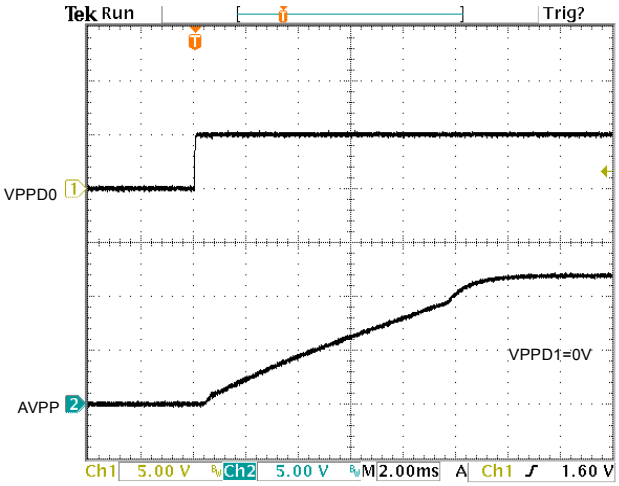


Figure 12. AVPP/BVPP Propagation Delay and Rise Time With 147µF Load, 12V Switch

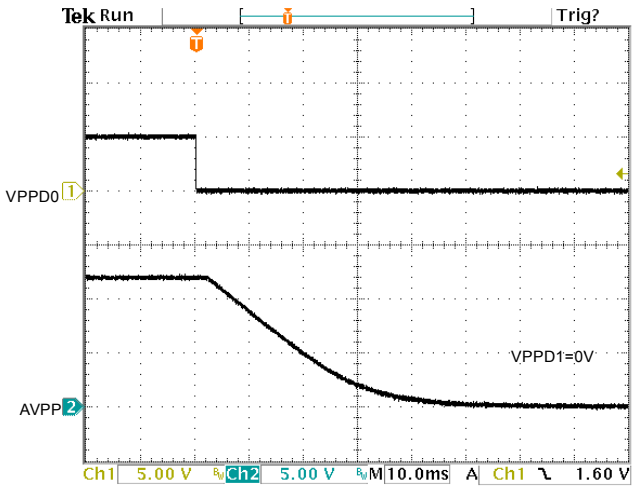


Figure 13. AVPP/BVPP Propagation Delay and Fall Time With 147µF Load, 12V Switch

Application Information

Overview

PC Cards were initially introduced as a means to add EEPROM (flash memory) to portable computers with limited onboard memory. The idea of add-in cards quickly took hold; modems, wireless LANs, Global Positioning Satellite (GPS) systems, multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprised of members from leading computer, software, PC Card, and semiconductor manufactures. One key goal was to realize the “plug and play” concept, i.e. cards and hosts from different vendors should be compatible.

PC Card Power Specification

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connectors. This power interface consists of two V_{CC}, two V_{PP}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{PP} terminals were originally specified as separate signals but are commonly tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage is supplied through the V_{PP} terminals.

Designing for Voltage Regulation

The current PCMCIA specification for output voltage regulation of the 5V output is 5% (250mV). In a typical PC power-system design, the power supply will have an output voltage regulation ($V_{PS(reg)}$) of 2% (100mV). Also, a voltage drop from the power supply to the PC Card will result from resistive losses (V_{PCB}) in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50mV) of the output voltage. Therefore, the allowable voltage drop (V_{DS}) for the G576 would be the PCMCIA voltage regulation less the power supply regula-tion and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100mV for the allowable voltage drop across the G576. The voltage drop is the output current multiplied by the switch resistance of the G576. Therefore, the maximum output current that can be delivered to the PC Card in regulation is the allowable voltage drop across the G576 divided by the output switch resistance.

$$I_O max = V_{DS} / R_{DS(on)}$$

The AVCC/BVCC outputs deliver 1A continuous at 3.3V and 5.5V within regulation over the operating temperature range. Using the same equations, the PCMCIA specification for output voltage regulation of the 3.3V output is 300mV. Using the voltage drop percentages for power supply regulation (2%) and PCB resistive loss (1%), the allowable voltage drop for the 3.3V switch is 200mV. The 12V outputs AVPP/BVPP of the G576 can deliver 150mA continuously.

Overcurrent and overtemperature protection

PC Cards are inherently subuect to damage from mishandling. Host systems require protection against short-circuited cards that could lead to power supply or PCB trace damage. Even systems sufficiently robust to withstand a short circuit would still undergo rapid battery discharge into the damaged PC Card, resulting in a sudden loss of system power. Most hosts include fuses for protection. The reliability of fused systems is poor, and requires troubleshooting and repair, usually by the manufacturer. When fuses are blown.

The G576 uses sense FETs to check for overcurrent conditions in each of the AVCC/BVCC and AVPP/BVPP outputs.Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. When an overcurrent condition is detected, only the power output affected is limited; all other power outputs continue to function normally. The $\overline{AOC}$ / $\overline{BOC}$ indicator, normally a ligic high, are a logic low when an overcurrent condition is detected providing for initiation of system diagnostics and/or sending a warning message to the user.

During power up, the G576 controls the rise time of the AVCC/BVCC and AVPP/BVPP outputs and limits the current into a faulty card or connector. If a short circuit is applied after power is established (e.g., hot insertion of a bad card), current is initially limited only by the impedance between the short and the power supply. In extreme cases, as much as 10A to 15A may flow into the short before the current limiting of the G576 engages. If the AVCC/BVCC or AVPP/BVPP outputs are driven below ground, the G576 may latch nondestructively in an off state, Cycling power will reestablish normal operation.

Overcurrent limiting for the AVCC/BVCC outputs is designed to activate if powered up into a short in the range of 0.8A to 2.2A, typically at about 1.5A. The AVPP/BVPP outputs limit from 120mA to 400mA, typically around 200mA. The protection circuitry acts by linearly limiting the current passing through the switch rather than initiating a full shutdown of the supply. Shutdown occurs only during thermal limiting.

Thermal limiting prevents destruction of the IC from overheating if the package power dissipation rating are exceeded. Thermal limiting disables power output until the device has cooled.

12V Supply Not Required

Most PC Card switches use the externally supplied 12V to power gate drive and other chip functions, which require that power be present at all times. The G576 offers considerable power savings by using an internal charge pump to generate the required higher voltages from 5V input; Therefore, the external 12V supply can be disable except when needed for flash-memory functions, thereby extending battery lifetime. Do not ground the 12V switch inputs when the 12-V input is not used. Additional power savings are realized by the G576 during a software shutdown in which quiescent current drops to a maximum of 3μA.

3.3V Low Voltage Mode

The G576 will operates in a 3.3V low voltage mode when 3.3V is only available input voltage (VCC5=0). This allows host and PC Cards to be operated in low-power 3.3V-only modes such as sleep modes or pager modes. Note that in these operation mode, the G576 will derive its bias current from the 3.3V input pin and only 3.3V can be delivered to the PC Card.

Voltage Transitioning Requirement

PC Cards are migrating from 5V to 3.3V to minimize power consumption, optimize board space, and increase logic speeds. The G576 meets all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3V/5V systems by first powering the card with 5V, then polling it to determine its 3.3V compatibility. The PCMCIA specification requires that the capacitors on 3.3V-compatible cards be discharged to below 0.8V before applying 3.3V power. This function is a power reset and ensures that sensitive 3.3V circuitry is not subjected to any residual 5V charge. The G576 offer a selectable V_{CC} and V_{PP} ground state, in accordance with PCMCIA 3.3V/5V switching specifications.

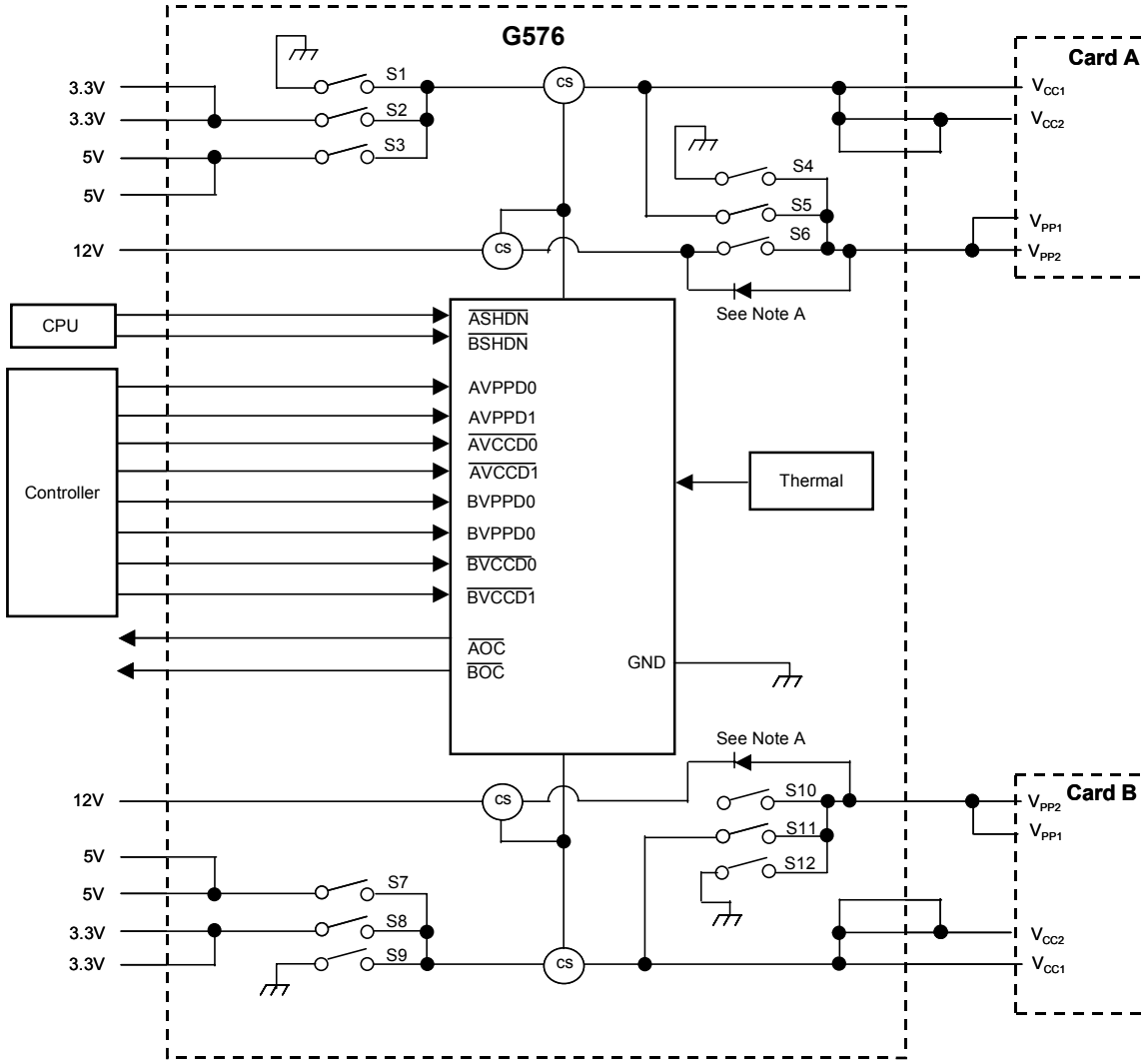
Output Ground Switches

PC Card specification requires that AVCC/BVCC be discharged within 100 ms. PC Card resistance can not be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes.

Power Supply Considerations

The G576 has multiple pins for each of its 3.3V, and 5V power inputs and for switched AVCC/BVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is significantly higher than that specified, resulting in increased voltage drops and lost power. it is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the G576, the power supply inputs should be bypassed with a 1μF electrolytic or tantalum capacitor paralleled by a 0.047μF to 0.1μF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1μF or larger, ceramic capacitor; doing so improves the immunity of the G576 to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the G576 and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similary, no pin should be taken below -0.3V.



Note : MOSFET switch S6/S10 has a back-gate diode from the source to the drain. Unused switch inputs should never be grounded.

Figure 14. Internal Switching Matrix

G576 Control Logic

AVCC

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{ASHDN}$	$\overline{AVCCD1}$	$\overline{AVCCD0}$	S1	S2	S3	AVCC
1	0	0	CLOSED	OPEN	OPEN	0V
1	0	1	OPEN	CLOSED	OPEN	3.3V
1	1	0	OPEN	OPEN	CLOSED	5V
1	1	1	CLOSED	OPEN	OPEN	0V
0	×	×	OPEN	OPEN	OPEN	Hi-Z

AVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{ASHDN}$	AVPPD0	AVPPD1	S4	S5	S6	AVPP
1	0	0	CLOSED	OPEN	OPEN	0V
1	0	1	OPEN	CLOSED	OPEN	AVCC*
1	1	0	OPEN	OPEN	CLOSED	VPP (12V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	×	×	OPEN	OPEN	OPEN	Hi-Z

* Output depends on AVCC

BVCC

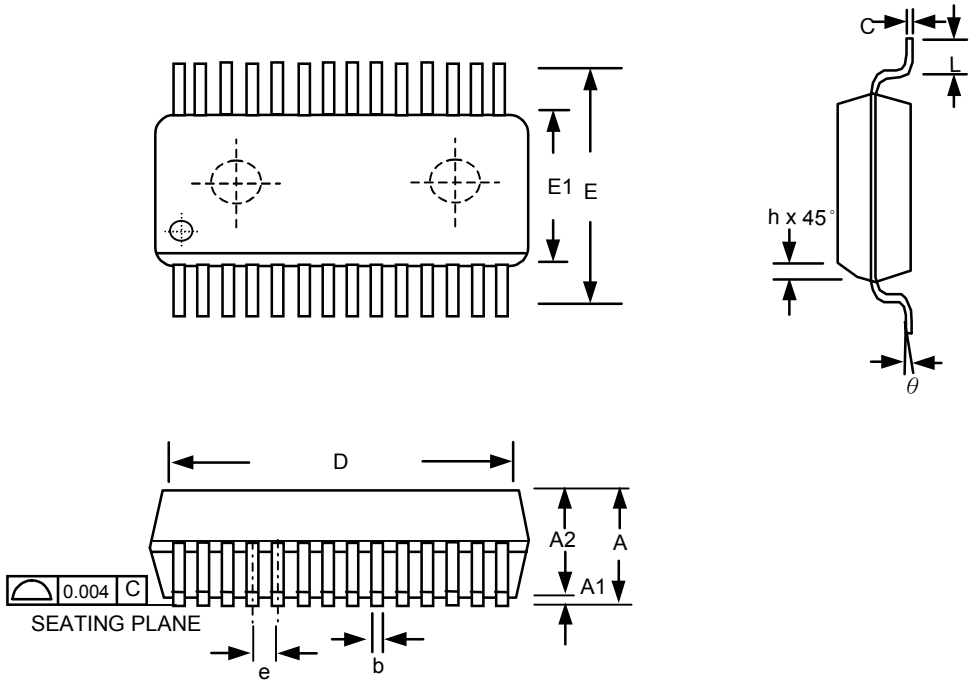
CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{BSHDN}$	$\overline{BVCCD1}$	$\overline{BVCCD0}$	S7	S8	S9	BVCC
1	0	0	CLOSED	OPEN	OPEN	0V
1	0	1	OPEN	CLOSED	OPEN	3.3V
1	1	0	OPEN	OPEN	CLOSED	5V
1	1	1	CLOSED	OPEN	OPEN	0V
0	×	×	OPEN	OPEN	OPEN	Hi-Z

BVPP

CONTROL SIGNALS			INTERNAL SWITCH SETTINGS			OUTPUT
$\overline{BSHDN}$	BVPPD0	BVPPD1	S10	S11	S12	BVPP
1	0	0	CLOSED	OPEN	OPEN	0V
1	0	1	OPEN	CLOSED	OPEN	BVCC*
1	1	0	OPEN	OPEN	CLOSED	VPP (12V)
1	1	1	OPEN	OPEN	OPEN	Hi-Z
0	×	×	OPEN	OPEN	OPEN	Hi-Z

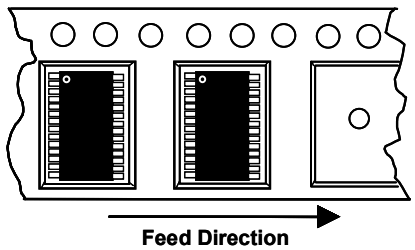
* Output depends on BVCC

Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			2.0			0.079
A1	0.05			0.002		
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	0.30	0.33	0.009	0.012	0.013
c	0.09	0.15	0.21	0.004	0.006	0.008
e	0.65 BASIC			0.026 BASIC		
D	9.90	10.20	10.50	0.390	0.402	0.413
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
L	0.55	0.75	0.95	0.022	0.030	0.038
θ	0	4	8	0	4	8
JEDEC	MO-150 (AH)					

Taping Specification



Feed Direction
Typical SSOP Package Orientation