

## FSTU32X800

### 20-Bit Bus Switch with Precharged Outputs and -2V Undershoot Protection

#### General Description

The Fairchild Switch FSTU32X800 provides 20-bits of high-speed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. The A and B Ports are protected against undershoot to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC®) senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning the switch on. The device also precharges the B Port to a selectable bias voltage (BiasV) to minimize live insertion noise.

The device is organized as two 10-bit switches with a bus enable ( $\overline{OE}_n$ ) signal. When  $\overline{OE}_n$  is LOW, the switch is ON and Port A is connected to Port B. When  $\overline{OE}_n$  is HIGH, the switch is OPEN and the B Port is precharged to BiasV through an equivalent 10-kΩ resistor.

#### Features

- 4Ω switch connection between two ports
- Undershoot Hardened to -2.0V
- Soft enable turn-on to minimize bus-to-bus charge sharing during enable
- Low  $I_{CC}$
- Zero bounce in flow-through mode
- Output precharge to minimize live insertion noise
- Control inputs compatible with TTL level
- See Applications Note AN-5008 for details

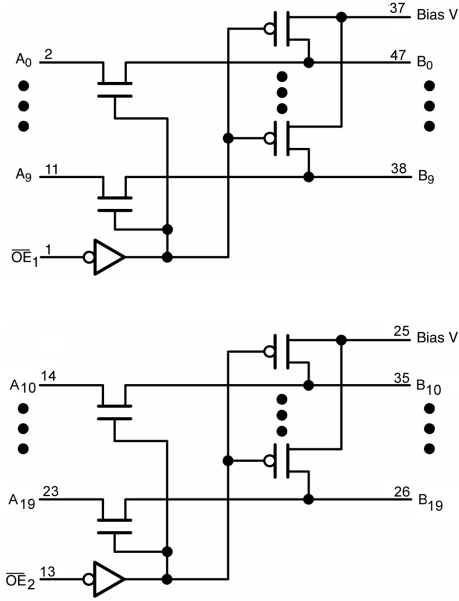
#### Ordering Code:

Order Number	Package Number	Package Description
FSTU32X800QSP	MQA48A	48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide

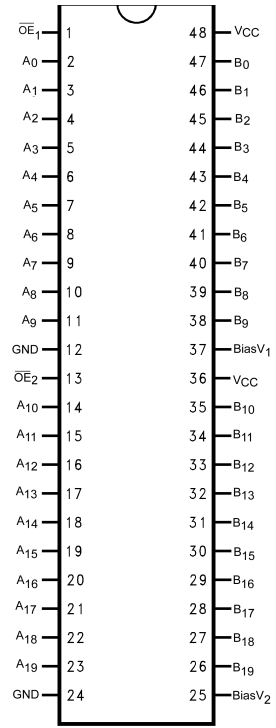
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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**Logic Diagrams**



**Connection Diagram**



**Pin Descriptions**

Pin Name	Description
$\overline{OE}_n$	Bus Switch Enable
A	Bus A
B	Bus B
BiasV <sub>n</sub>	Bus B Voltage Bias

**Truth Table**

$\overline{OE}_n$	B <sub>0</sub> –B <sub>19</sub>	Function
L	A <sub>0</sub> –A <sub>19</sub>	Connect
H	BiasV	Precharge

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-2.0V to +7.0V
Bias V Voltage Range	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Sink Current	128 mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	+/- 100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150 °C

**Recommended Operating Conditions** (Note 3)

Power Supply Operating ( $V_{CC}$ )	4.0V to 5.5V
Precharge Supply (BiasV)	1.5V to $V_{CC}$
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0 ns/V to 5 ns/V
Switch I/O	0 ns/V to DC
Free Air Operating Temperature ( $T_A$ )	-40 °C to +85 °C

**Note 1:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Unused control inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40\text{ °C to }+85\text{ °C}$			Units	Conditions
			Min	Typ (Note 4)	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18\text{ mA}$
$V_{IH}$	HIGH Level Input Voltage	4.0 - 5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.0 - 5.5			0.8	V	
$I_I$	Input Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5V$
$I_O$	Output Current	4.5	0.25			mA	BiasV = 2.4V, B = 0
$I_{OZ}$	OFF-STATE Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq A \leq V_{CC}, V_{IN} = V_{IH}$
$R_{ON}$	Switch On Resistance (Note 5)	4.5		4.0	7.0	$\Omega$	$V_S = 0V, I_{IN} = 64\text{ mA}$
		4.5		4.0	7.0	$\Omega$	$V_S = 0V, I_{IN} = 30\text{ mA}$
		4.5		8.0	15.0	$\Omega$	$V_S = 2.4V, I_{IN} = 15\text{ mA}$
		4.0		11.0	20.0	$\Omega$	$V_S = 2.4V, I_{IN} = 15\text{ mA}$
$I_{CC}$	Quiescent Supply Current (Note 6)	5.5			3.0	$\mu\text{A}$	$V_S = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input (Note 7)	5.5			2.5	mA	$\overline{OE}$ Input at 3.4V Other Inputs at $V_{CC}$ or GND
$I_{BIAS}$	Bias Pin Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$\overline{OE} = 0V, B = 0V, \text{BiasV} = 5.5V$
$I_{OZU}$	Switch Undershoot Current	5.5			100.0	$\mu\text{A}$	$I_{IN} = -20\text{ mA}, \overline{OE} = 5.5V, V_{OUT} \geq V_{IH}$
$V_{IKU}$	Voltage Undershoot	5.5			-2.0	V	$0.0\text{ mA} \geq I_{IN} \geq -50\text{ mA}, \overline{OE} = 5.5V$

**Note 4:** Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25^\circ\text{C}$

**Note 5:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

**Note 6:** Per  $V_{CC}$  pin.

**Note 7:** Per TTL driven inputs, control pins only.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C,}$				Units	Conditions	Figure Number
		$C_L = 50\text{ pF, } R_U = R_D = 500\Omega$						
		$V_{CC} = 4.5 - 5.5\text{V}$		$V_{CC} = 4.0\text{V}$				
		Min	Max	Min	Max			
$t_{PHL}$ , $t_{PLH}$	Propagation Delay Bus to Bus (Note 8)		0.25		0.25	ns	$V_I = \text{OPEN}$	Figures 1, 2
$t_{PZH}$	Output Enable Time $\overline{OE}_1, \overline{OE}_2$ , to $A_n, B_n$	7.0	30.0		35.0	ns	$V_I = \text{OPEN}$ BiasV = GND	Figures 1, 2
$t_{PZL}$		7.0	30.0		35.0	ns	$V_I = 7\text{V}$ BiasV = 3V	
$t_{PHZ}$	Output Disable Time $\overline{OE}_1, \overline{OE}_2$ , to $A_n, B_n$	1.0	6.1		6.5	ns	$V_I = \text{OPEN}$ BiasV = GND	Figures 1, 2
$t_{PLZ}$		1.0	7.3		6.8	ns	$V_I = 7\text{V}$ BiasV = 3V	

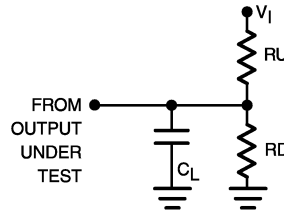
**Note 8:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

## Capacitance (Note 9)

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Control Pin Input Capacitance	3.0		pF	$V_{CC} = 5.0\text{V}$
$C_{I/O}$	Input/Output Capacitance	5.0		pF	$V_{CC}, \overline{OE} = 5.0\text{V}$

**Note 9:**  $T_A = +25\text{ }^\circ\text{C}$ ,  $f = 1\text{ MHz}$ , Capacitance is characterized but not tested.

## AC Loading and Waveforms

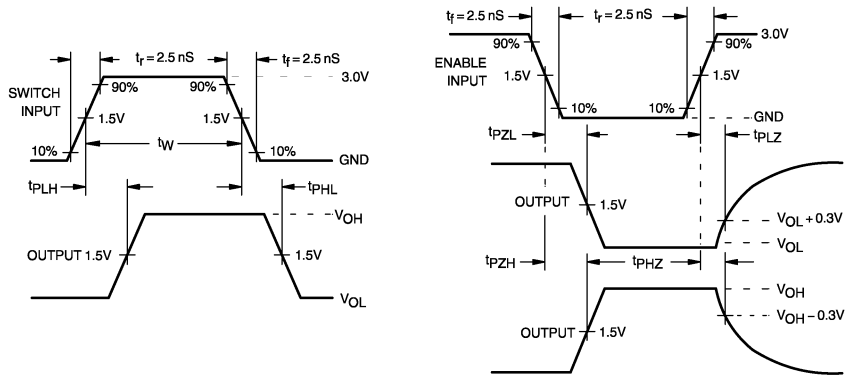


**Note:** Input driven by 50Ω source terminated in 50Ω,  $R_U = R_D = 500\Omega$

**Note:**  $C_L$  includes load and stray capacitance,  $C_L = 50\text{ pF}$

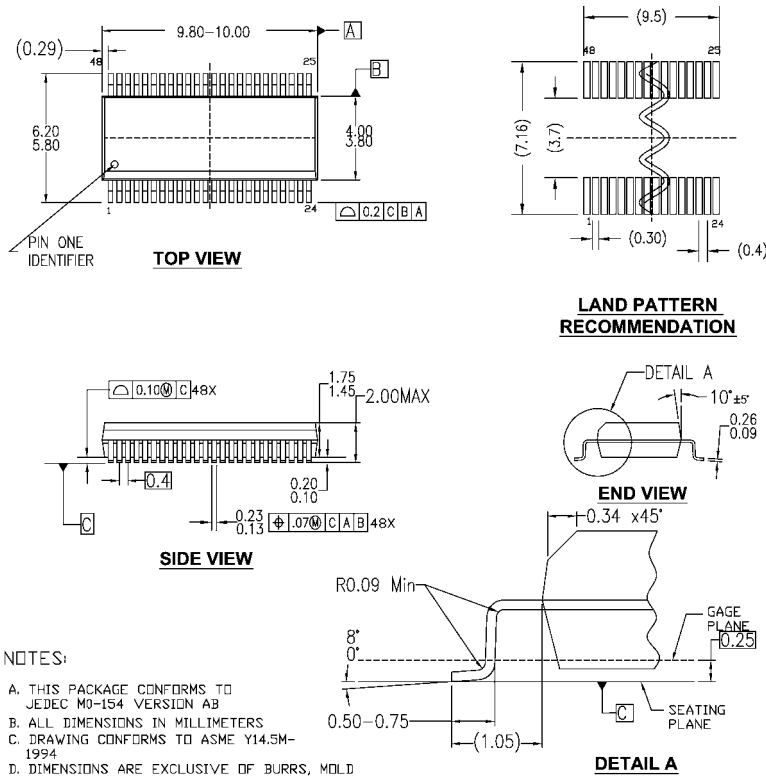
**Note:** Input PRR = 1.0 MHz,  $t_W = 500\text{ ns}$

**FIGURE 1. AC Test Circuit**



**FIGURE 2. AC Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted



- NOTES:
- A. THIS PACKAGE CONFORMS TO JEDEC MO-154 VERSION AB
  - B. ALL DIMENSIONS IN MILLIMETERS
  - C. DRAWING CONFORMS TO ASME Y14.5M-1994
  - D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

MQA48AREVA

**48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide Package Number MQA48A**

**Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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