FS8170 2.5 GHz Low Power Phase-locked Loop IC

Description

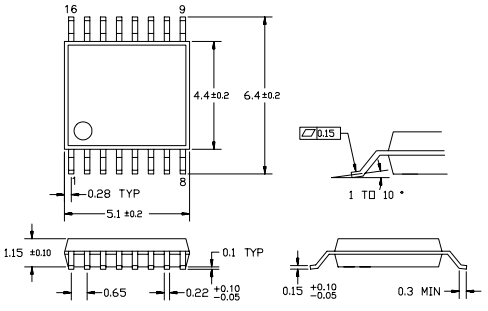
The FS8170 IC is a serial data input, fully programmable phase-locked loop with a 2.5 GHz prescaler for use in the local oscillator subsystem of radio transceivers. Multi-modulus division ratios of 32/33 and 64/65 are selectable thru serial programming to enable pulse swallowing operation. When combined with an external VCO, the FS8170 becomes the core of a very low power frequency synthesizer well-suited for mobile communication applications, such as 2.4 GHz ISM-band wireless data links and cellular GSM and PCS. **The FS8170 is also pin compatible with Fujitsu's MB15E07SL IC.**

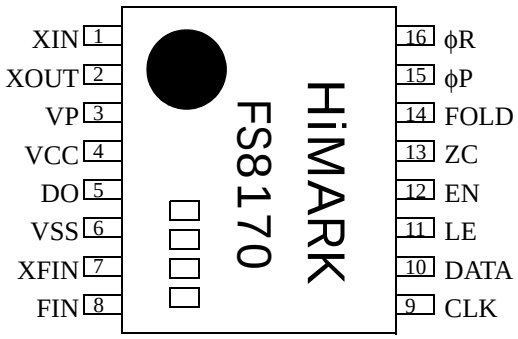
Features

- Maximum input frequency: 2.5 GHz
- Supply voltage range from 2.4 V to 3.6 V
- Low current consumption in locked state: 3.5 mA typ. (V_{CC} = V_P = 2.7 V, T_A = +25 °C)
  4.0 mA typ. (V_{CC} = V_P = 3.0 V, T_A= +25 °C)
  10 µA max. in asynchronous power-down mode
- Digitally-filtered lock detect output
- 18-bit programmable input frequency divider using ÷ 32/33/64/65 multi-modulus prescaler with divide ratio range from 992 to 65631 for ÷ 32/33 mode and from 4032 to 131135 for ÷ 64/65 mode
- 14-bit programmable reference frequency divider with divide ratio range from 3 to 16383
- Programmable charge pump current: 1.5 mA or 6 mA
- Pin compatible with Fujitsu MB15E07, MB15E07L, MB15E07SL
- 16 pin, plastic TSSOP (0.65 mm pitch)

Package and Pin Assignment

16 pin, plastic TSSOP (dimensions in mm)

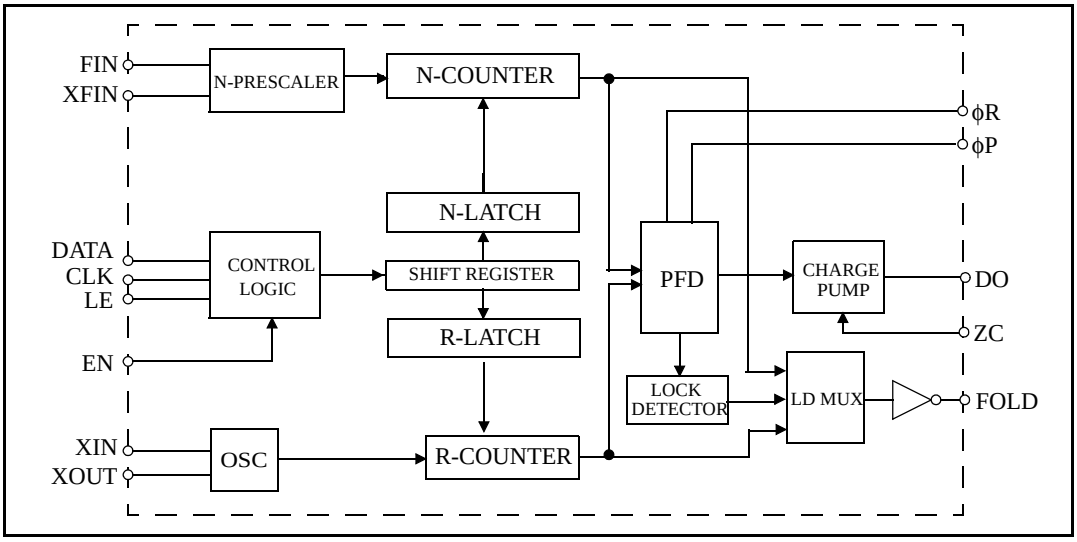




Pin Descriptions

Number	Name	I/O	Description
1	XIN	I	Reference crystal oscillator or external clock input with internally biased amplifier
2	XOUT	O	Reference crystal oscillator output
3	VP	—	Power supply voltage for the charge pump
4	VCC	—	Power supply voltage
5	DO	O	Single-ended charge pump output
6	VSS	—	Ground
7	XFIN	I	Complementary input for prescaler (normally ac-bypassed via a capacitor)
8	FIN	I	VCO frequency input with internally biased input amplifier
9	CLK	I	Shift register clock input
10	DATA	I	Serial data input
11	LE	I	Load enable signal input
12	EN	I	Power-down control
13	ZC	I	Forced high-impedance control for the charge pump
14	FOLD	O	Multiplexed CMOS level output (see Functional Description section for programming information)
15	ϕP	O	Phase comparator N-channel open drain output for an external charge pump
16	ϕR	O	Phase comparator CMOS inverter output for an external charge pump

Functional Block Diagram



Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{CC}	V_{SS} – 0.3 to V_{SS} + 4.0	V
	V_P	V_{CC} to 6.0	V
Input voltage range	V_{FIN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Output voltage range	V_O	V_{SS} to V_{CC}	V
	V_{DO}	V_{SS} to V_P	V
Storage temperature range	T_{STG}	–55 to 125	°C
Soldering temperature range	T_{SLD}	260	°C
Soldering time range	t_{SLD}	4	s
ESD rating (human body mode)		3500	eV

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	V_{CC}	2.4	3.0	3.6	V
	V_P	Vcc	–	5.5	V
Operating temperature	T_A	–40	25	80	°C

Electrical Characteristics

(V_{CC} = V_P = 3.0 V, V_{SS} = 0 V, T_A = –40 to 85 °C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
GENERAL						
Power supply current consumption	$I_{CC,total}$	fin = 2.5 GHz		4		mA
Standby current consumption	$I_{CC,standby}$	ZC = "H" or open			10	µA
FIN operating frequency	f_{FIN}	V_{FIN} = 0.3 V_{pk-pk} sinusoid	50		2500	MHz
XIN operating frequency	f_{XIN}		3		40	MHz
Input sensitivity	P_{FIN}	50 Ω measurement system	-15		+2	dBm
XIN input voltage swing	V_{XIN}		0.5		V_{CC}	V_{pk-pk}
CHARGE PUMP						
RF charge pump output current	IDO_{source}	V_{DO} = V_P/2, CS bit = "H"		-6		mA
	IDO_{sink}	V_{DO} = V_P/2, CS bit = "H"		6		mA
	IDO_{source}	V_{DO} = V_P/2, CS bit = "L"		-1.5		mA
	IDO_{sink}	V_{DO} = V_P/2, CS bit = "L"		1.5		mA
DIGITAL INTERFACE (DATA, CLK, LE, PS, ZC)						
High-level input voltage	V_{IH}		$0.8\times V_{CC}$			V
Low-level input voltage	V_{IL}				$0.2\times V_{CC}$	V
High-level input current	I_{IH}	V_{IH} = V_{CC} = 3.6V	–1		1	µA
Low-level input current	I_{IL}	V_{IL} = 0 V, V_{CC} = 3.6V	–1		1	µA
XIN logic HIGH input current	$I_{IH,XIN}$	V_{IH} = V_{DD}			100	µA
XIN logic LOW input current	$I_{IL,XIN}$	V_{IL} = 0 V	–100			µA
ϕP logic LOW output voltage	V_{OL}	Open drain output			0.4	V
ϕP logic LOW output current	I_{OL}	Open drain output	1			mA
ϕR logic HIGH output voltage	V_{OH}	V_{CC} = V_P = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4			V
ϕR logic LOW output voltage	V_{OL}	V_{CC} = V_P = 3.0 V, I_{OL} = 1 mA			0.4	V
ϕR logic HIGH output current	I_{OH}	V_{CC} = V_P = 3.0 V			–1	mA
ϕR logic LOW output current	I_{OL}	V_{CC} = V_P = 3.0 V	1			mA

Electrical Characteristics

(V_{CC} = V_P = 3.0 V, V_{SS} = 0 V, T_A = –40 to 85 °C unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
FOLD logic HIGH output voltage	V_{OH}	V_{CC} = V_P = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4			V
FOLD logic LOW output voltage	V_{OL}	V_{CC} = V_P = 3.0 V, I_{OL} = 1 mA			0.4	V
FOLD logic HIGH output current	V_{OH}	V_{CC} = V_P = 3.0 V			–1	mA
FOLD logic LOW output current	V_{OL}	V_{CC} = V_P = 3.0 V	1			mA
MICROWIRE TIMING						
DATA to CLK setup time	t_{SU1}		10			ns
DATA to CLK hold time	t_{HOLD1}		10			ns
CLK to LE setup time	t_{SU2}		20			ns
CLK to LE hold time	t_{HOLD2}		30			ns
LE Pulse width	t_{EW}		50			ns

Functional Description

Programmable Input Frequency Divider

The VCO output to the FIN pin is divided by the programmable divider and then internally output to the phase/frequency detector (PFD) as f_V. The programmable input frequency divider consists of a multi-modulus (selectable ÷ 32/33 or ÷ 64/65 *(M/M+1))* prescaler and a 18-bit N-counter, which is further comprised of a 7-bit swallow A-counter, and a 11-bit main *B*-counter. The total divide ratio, *N*, is related to values for *M*, *A*, and *B* through the relation

$$N = (M + 1) \times A + M \times (B - A) = M \times B + A,$$

with $B \geq A$. The minimum programmable divisor for continuous counting is given by $M \times (M - 1)$, and is $32 \times (32 - 1) = 992$ for the ÷ 32/33 prescaler mode, and is $64 \times (64 - 1) = 4032$ for the ÷ 64/65 mode. Hence, the valid total divide ratio range for the input divider is $N = 992$ to 65631 for the ÷ 32/33 mode and $N = 4032$ to 131135 for the ÷ 64/65 mode.

Programmable Reference Frequency Divider

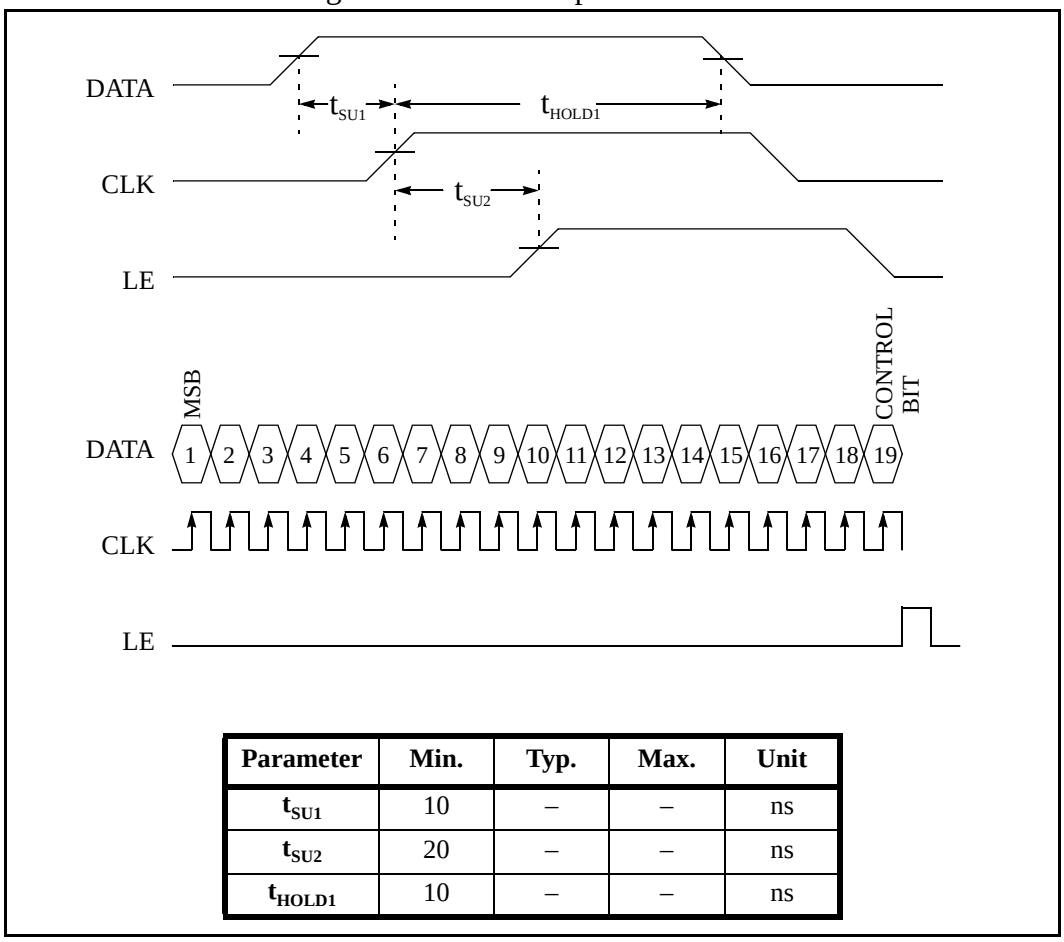
The crystal oscillator output is divided by the programmable reference divider and then internally output to the PFD as f_R. The programmable reference frequency divider consists of a 14-bit reference R-counter. Becasue of its specific design, the minimum acceptable divisor for *R* is 3, and hence the total divide ratio, *R*, ranges from 3 to 16383.

Shift Register Configuration

The divide ratios for the input and reference dividers are input using a 19-bit serial interface consisting of separate clock (CLK), data (DATA), and load enable (LE) lines. The format of the serial data is shown in Table 1. The data on the DATA line is written to the shift register on the rising edge of the CLK signal and is input with MSB first, and the last bit is used as the latch select control bit. The data on the DATA line should be changed on the falling edge of CLK, and LE should be held LOW while data is being written to the shift register. Data is transferred from the shift register to one of the frequency divider latches when LE is set HIGH. When the latch select control bit is set LOW, data is loaded to the 18-bit *N*-counter latch, and when the latch select control bit is set HIGH, the 4 MSBs are recognized as CS, LDS, FC, SW, respectively, and the next 14 data bits are loaded to the 14-bit *R*-counter latch. The definition of the 4 MSBs will be described in Table 5 and 6. Note that LDS should be set LOW for normal operation.

Also, serial input data timing waveforms are shown in Fig. 1.

Fig. 1 – Serial data input waveforms



Parameter	Min.	Typ.	Max.	Unit
t_{SU1}	10	–	–	ns
t_{SU2}	20	–	–	ns
t_{HOLD1}	10	–	–	ns

LSB ↓ Data Flow → MSB ↓

Table 1: Serial data input format

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
CB	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11
	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS	CS

CB	Control bit for selecting the N or R latch
A1 to A7	Control bits for setting the divide ratio of the programmable swallow counter (0 to 127)
B1 to B11	Control bits for setting the divide ratio of the programmable main counter (3 to 2047)
R1 to R14	Control bits for setting the divide ratio of the programmable reference counter (3 to 16383)
SW	Control bit for setting the divide ratio of the prescaler (32/33 or 64/65)
FC	Control bit for setting the polarity of the phase/frequency detector
LDS	Control bit for selecting the output for the FOLD pin
CS	Control bit for setting the charge pump current level

Table 2: Binary 7-bit data format for swallow counter

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Table 3: Binary 11-bit data format for main counter

Divide ratio (B)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Table 4: Binary 14-bit data format for reference counter

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 5: Data format for 3 optional bits

Bit	H	L	Description
SW	32/33	64/65	Prescaler dual-modulus ratio setting
CS	$\pm$ 6 mA	$\pm$ 1.5 mA	Charge pump current setting
LDS	FO signal	LD signal	FOLD output select setting

Table 6: Data format for FC bit (LDS = HIGH)

	FC = HIGH				FC = LOW			
	DO	ϕR	ϕP	FOLD	DO	ϕR	ϕP	FOLD
$f_R > f_V$	H	L	L	FOLD = f_R	L	H	Z[a]	FOLD = f_V
$f_R < f_V$	L	H	Z		H	L	L	
$f_R = f_V$	Z	L	Z		Z	L	Z	

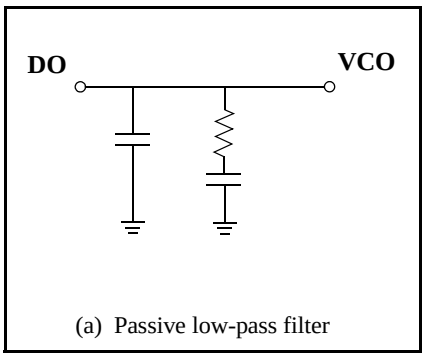
a. Z denotes high impedance state

Phase/Frequency Detector (PFD)

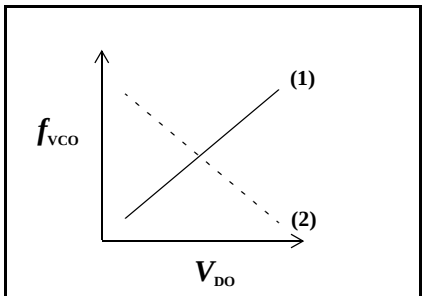
The PFD compares an internal input frequency divider output signal, f_V, with an internal reference frequency divider output signal, f_R, and generates an error signal, DO, which is proportional to the phase error between f_V and f_R. The DO output is intended for use with a passive filter as shown in Fig. 2 (a). The polarity of DO is selectable by setting the bit FC to high or low. The setting should depend on the frequency-voltage characteristic of external VCO as depicted in Fig. 2 (b).

The input/output waveforms for the PFD are shown in Fig. 3.

Fig. 2 – Low-pass filter and external VCO frequency-voltage characteristic



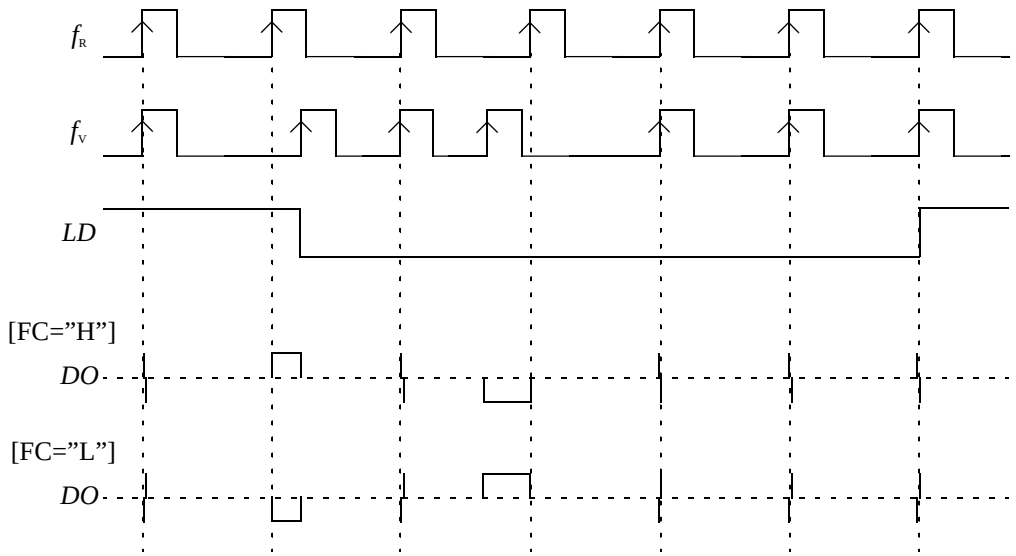
(a) Passive low-pass filter



(b) VCO frequency-voltage characteristic

Note: If VCO has a positive tuning curve similiar to trace (1), set FC = "H," otherwise if the VCO has a negative tuning curve similar to trace (2), set FC = "L."

Fig. 3 – Phase comparator output waveforms



1. Pulses of finite width on DO output are generated during locked state to prevent dead zone.
2. A "locked" condition (LD is HIGH) is indicated when the phase error is less than t1 or t2 at least for 3 consecutive comparison cycles, otherwise an "unlocked" condition (LD is LOW) is indicated.
3. The values of t_1 and t_2 depend on the XIN input frequency:
   $t_1 \geq 2/fosc$ (e.g. $t_1 \geq 250$ ns, if $f_{XIN} = 8$ MHz)
   $t_2 \geq 2/fosc$ (e.g. $t_2 \geq 250$ ns, if $f_{XIN} = 8$ MHz)
4. LD becomes HIGH during power-down mode (when EN is set LOW).

Charge Pump (CP)

The phase error signal, DO, generated from the PFD will pump charge into an external loop filter, which then converts the charge to produce the VCO's tuning voltage. With a constant pumping rate, the shift of the VCO's tuning voltage will be directly proportional to the phase error signal DO. Two pumping rates, 1.5 mA and 6 mA, are provided by the chip and are selectable through the bit CS as defined previously in Table 5. Also, the charge pump characteristics corresponding to both modes are shown in the Typical Characteristics section. The internal charge pump may be turned off by the pin ZC. When ZC is set low, the internal charge pump will stay in its high-impedance state and will not pump any charge into the external LPF. In this case, the user is allowed to utilize one's own charge pump by two control pins ϕP and ϕR which are defined in Table 6. ϕP and ϕR are the error signals directly proportional to the positive/negative phase error when FC = "H." When FC = "L," the relation becomes negative/positive.

Table 7: Setting for the pin ZC

ZC	Do Output
H	Normal output
L	High impedance

Multi-function Lock Detect Output (FOLD)

A digital lock detect function is included with the phase detector through an internal digital filter to produce a logic level output which is available on the FOLD output pin. The criterion of lock indication depends on the period of the crystal oscillator reference. The lock dectect output is HIGH whenever the phase error between phase detector inputs is less than 2 times of the crystal period for more than three consecutive comparison cycles, otherwise is low. Note that LD becomes HIGH during the power saving mode. The LD output is depicted in Fig. 3 as well.

Power-down Control (EN)

By setting the pin EN to LOW, the chip enters into power-down mode, reducing the current consumption. During the power-down mode, the phase detector output, DO, is set to its high impedance. Normal operation mode resumes when EN is switched to HIGH. To prove a smooth start-up condition, an intermittent control circuit is activated when the device returns to normal operation. Due to the unknown relationship between f_V and f_R after returning from power-down, the PFD output is unpredictable and may give rise to a significant jump in the VCO's frequency which will result in an increased lock-up time. To prevent this, the FS8170 employs an intermittent control circuit to limit the magnitude of the error signal generated by the phase detector when it returns to normal operation, thus ensuring a much quicker return to the fully phase-locked condition.

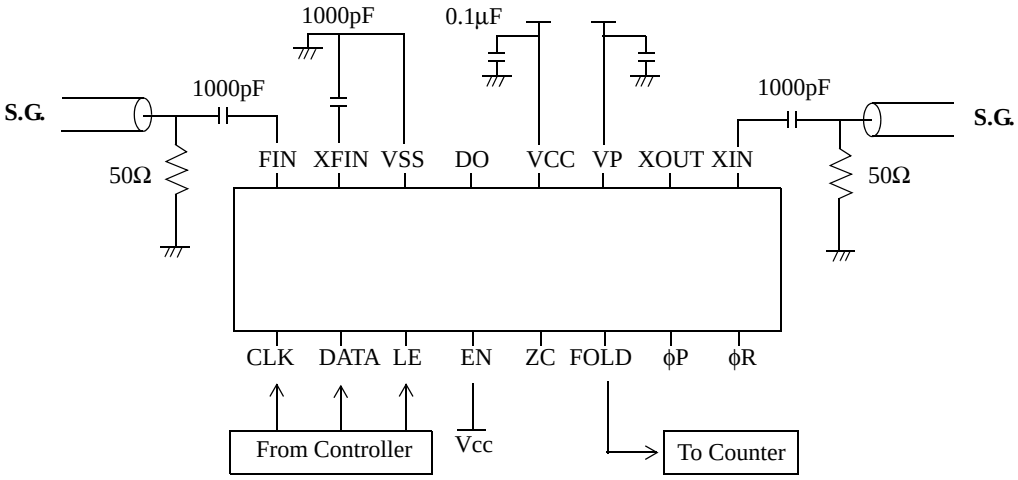
Table 8: Setting for the pin EN

EN	Status
H	Normal operation mode
L	Power-down mode

Measurement Circuit Setup

The circuit shown in Fig. 4 is used for measuring the input sensitivity of the FIN input of the PLL.

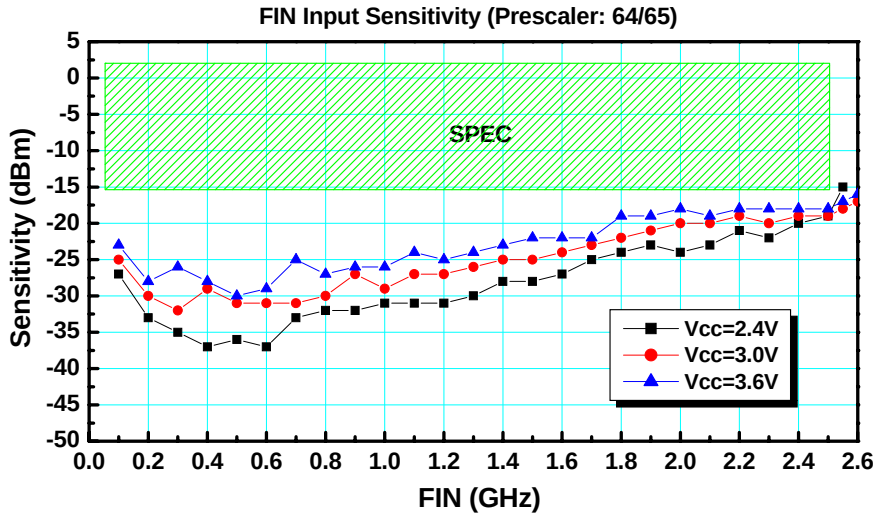
Fig. 4 – FIN input sensitivity test circuit

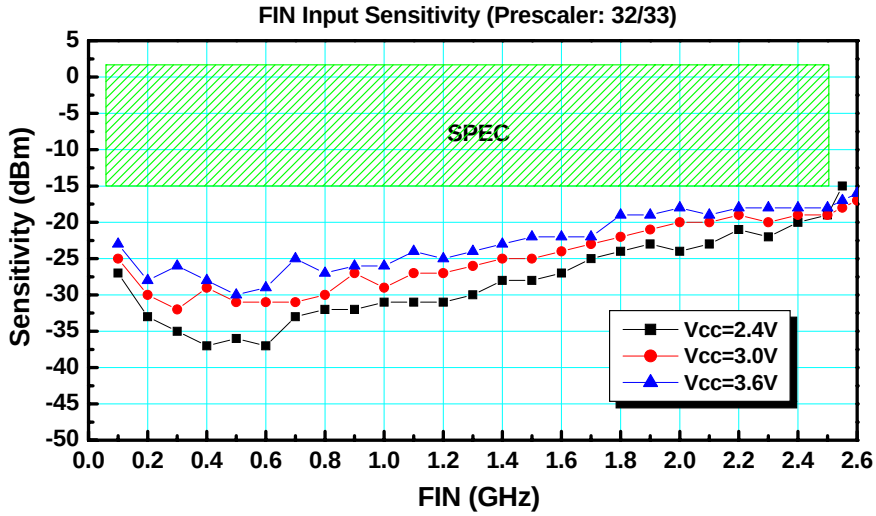


Typical Characteristics

FIN Input Sensitivity

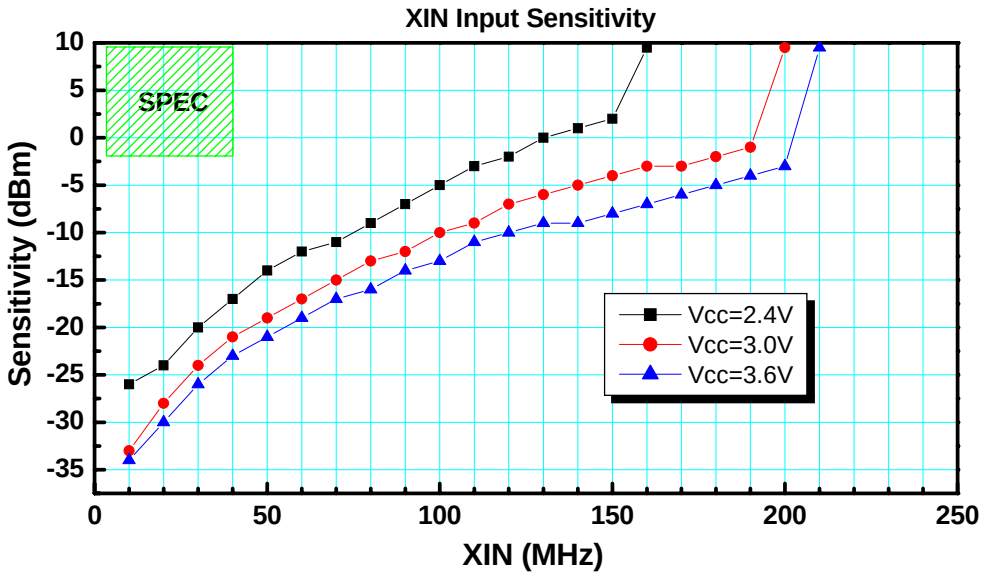
Fig. 5 – Input sensitivity vs. frequency





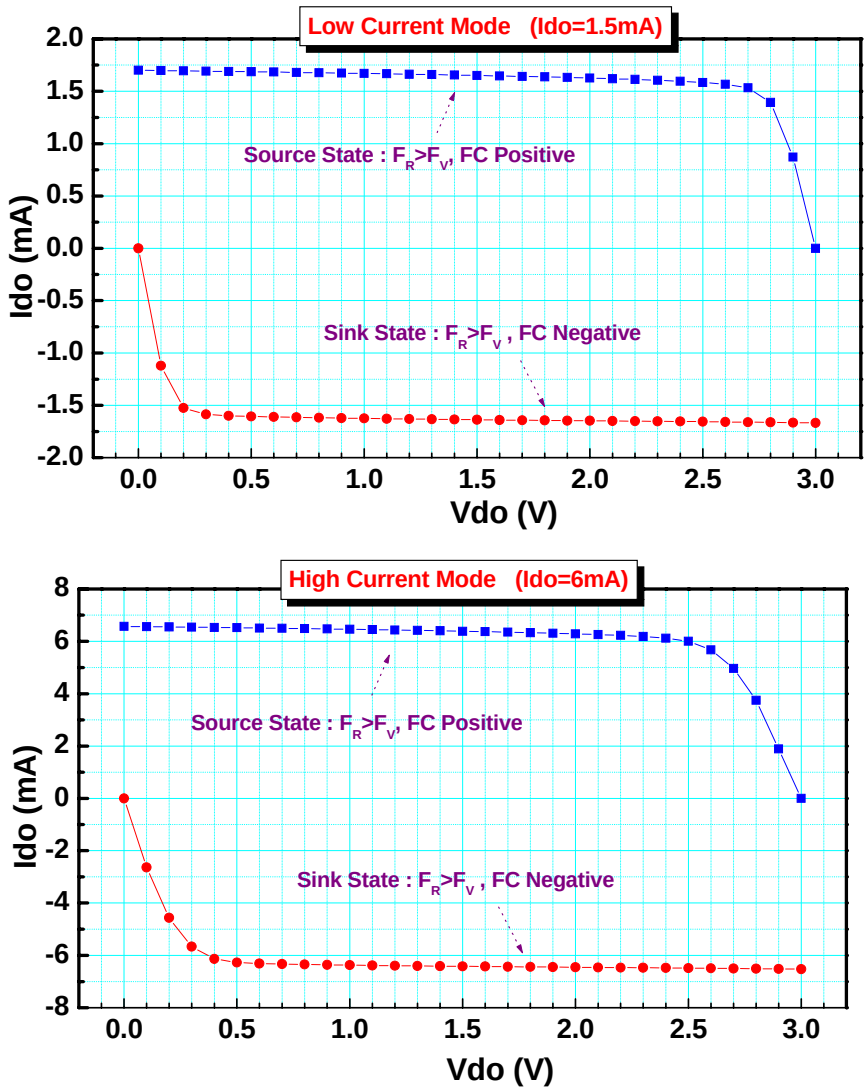
XIN Input Sensitivity

Fig. 6 – XIN input sensitivity vs. frequency



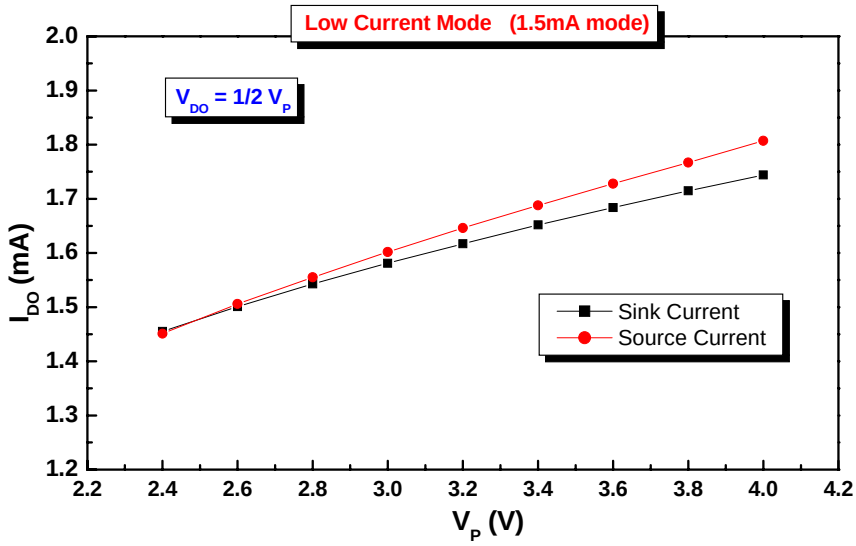
Charge Pump Characteristic

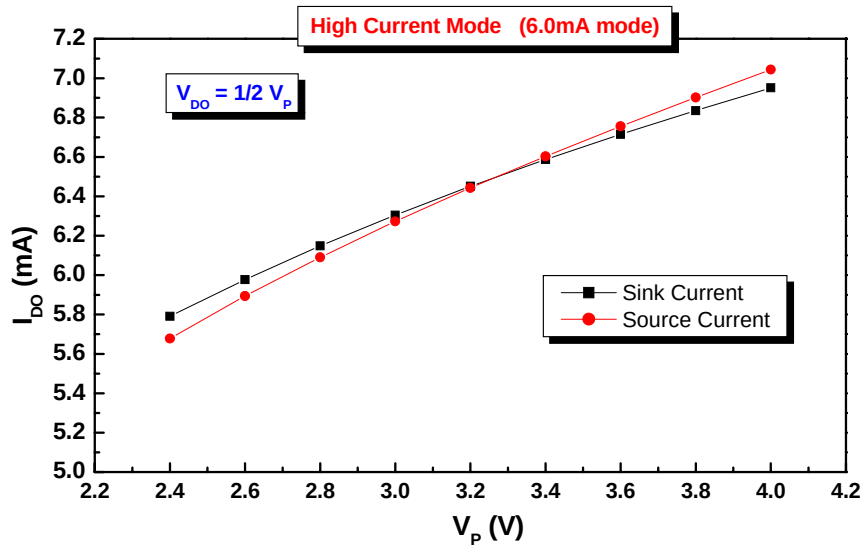
Fig. 7 – Charge pump current vs. V_{DO}



Supply Voltage Dependence of Charge Pump Current

Fig. 8 – Charge pump current vs. supply voltage at $V_{DO} = V_P/2$





Appication Circuit