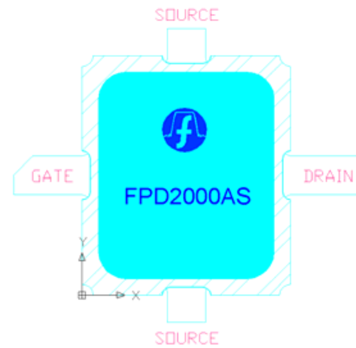
- PERFORMANCE (1.8 GHz)
  - ♦ 33 dBm Output Power (P_{1dB})
  - ♦ 14 dB Power Gain (G_{1dB})
  - ♦ 46 dBm Output IP3
  - ♦ 10V Operation
  - ♦ 50% Power-Added Efficiency
  - ♦ Evaluation Boards Available
  - ♦ Design Data Available on Website
  - ♦ Usable Gain to 4GHz



SEE PACKAGE OUTLINE FOR MARKING CODE

- DESCRIPTION AND APPLICATIONS

The FPD2000AS is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), optimized for power applications in L-Band. The surface-mount package has been optimized for low parasitics.

Typical applications include drivers or output stages in PCS/Cellular base station transmitter amplifiers, as well as other power applications in WLL/WLAN amplifiers.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT *f* = 1.8 GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	V_{DS} = 10V; I_{DS} = 350 mA Γ_S and Γ_L tuned for Optimum IP3	32	33		dBm
Power Gain at dB Gain Compression	G_{1dB}	V_{DS} = 10V; I_{DS} = 350 mA Γ_S and Γ_L tuned for Optimum IP3	12.5	14.0		
Maximum Stable Gain S_{21}/S_{12}	MSG	V_{DS} = 10 V; I_{DS} = 350 mA P_{IN} = 0dBm, 50Ω system		20		dB
Power-Added Efficiency at 1dB Gain Compression	PAE	V_{DS} = 10V; I_{DS} = 350 mA Γ_S and Γ_L tuned for Optimum IP3		45		%
3rd-Order Intermodulation Distortion	IP3	V_{DS} = 10V; I_{DS} = 350 mA Γ_S and Γ_L tuned for Optimum IP3 P_{OUT} = 22 dBm (single-tone level)		-47	-44	dBc
Saturated Drain-Source Current	I_{DSS}	V_{DS} = 1.3 V; V_{GS} = 0 V	975	1150	1325	mA
Maximum Drain-Source Current	I_{MAX}	V_{DS} = 1.3 V; V_{GS} ≅ +1 V		1800		mA
Transconductance	G_M	V_{DS} = 1.3 V; V_{GS} = 0 V		1200		mS
Gate-Source Leakage Current	I_{GSO}	V_{GS} = -3 V		35	85	µA
Pinch-Off Voltage	$\|V_P\|$	V_{DS} = 1.3 V; I_{DS} = 4 mA	0.7	0.9	1.4	V
Gate-Source Breakdown Voltage	$\|V_{BDGS}\|$	I_{GS} = 4 mA	14	16		V
Gate-Drain Breakdown Voltage	$\|V_{BDGD}\|$	I_{GD} = 4 mA	20	22		V
Thermal Resistivity (channel-to-case)	Θ_{CC}	See Note on following page		20		°C/W

- RECOMMENDED OPERATING BIAS CONDITIONS
  Drain-Source Voltage: From 5V to 10V
  Quiescent Current: From 25% I_{DSS} to 55% I_{DSS}

- ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V_{DS}	$-3V < V_{GS} < +0V$		12	V
Gate-Source Voltage	V_{GS}	$0V < V_{DS} < +8V$		-3	V
Drain-Source Current	I_{DS}	For $V_{DS} > 2V$		I_{DSS}	mA
Gate Current	I_G	Forward / Reverse current		+15/-2	mA
RF Input Power[2]	P_{IN}	Under any acceptable bias state		900	mW
Channel Operating Temperature	T_{CH}	Under any acceptable bias state		175	ºC
Storage Temperature	T_{STG}	Non-Operating Storage	-40	150	ºC
Total Power Dissipation	P_{TOT}	See De-Rating Note below		7.6	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits[3]		2 or more Max. Limits		80	%

[1]$T_{Ambient}$ = 22°C unless otherwise noted [2]Max. RF Input Limit must be further limited if input VSWR > 2.5:1
[3]Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:
  P_{DC}: DC Bias Power
  P_{IN}: RF Input Power
  P_{OUT}: RF Output Power
- Total Power Dissipation to be de-rated as follows above 22°C:
  P_{TOT}= 7.6 - (0.05W/°C) x T_{PACK}
  where T_{PACK} = *source tab lead temperature above 22°C*
  (coefficient of de-rating formula is the Thermal Conductivity)

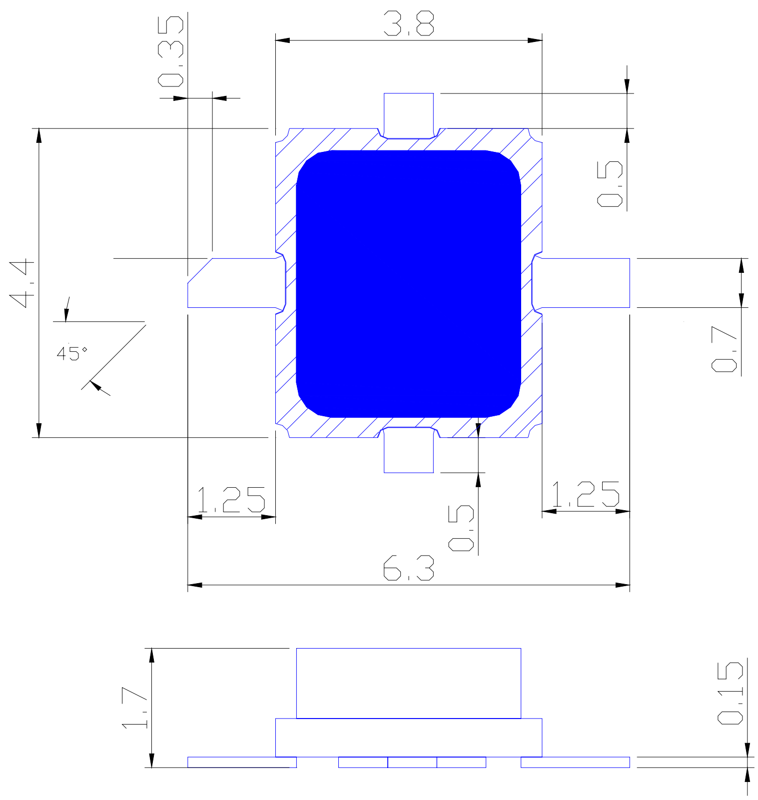
Example: For a 55°C source lead temperature: P_{TOT} = 7.6 - (0.05 x (55 – 22)) = 5.95W

- **For optimum heatsinking, metal-filled through (Source) via holes should be used directly below the central metallized ground pad on the bottom of the package.**
- *Note on Thermal Resistivity:* The nominal value of 20°C/W is measured with the package mounted on a large heatsink with thermal compound to ensure adequate (unsoldered) contact. The package temperature is referred to the Source leads.

- HANDLING PRECAUTIONS
  To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

- BIASING GUIDELINES
  - Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
  - Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD2000AS.
  - Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 1.43 Ω for the recommended 200mA operating point. This approach will require a DC Source resistor capable of at least 200mW dissipation.
  - The recommended 350mA bias point is nominally a Class AB mode. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point.

- PACKAGE OUTLINE
  (dimensions in millimeters – mm)

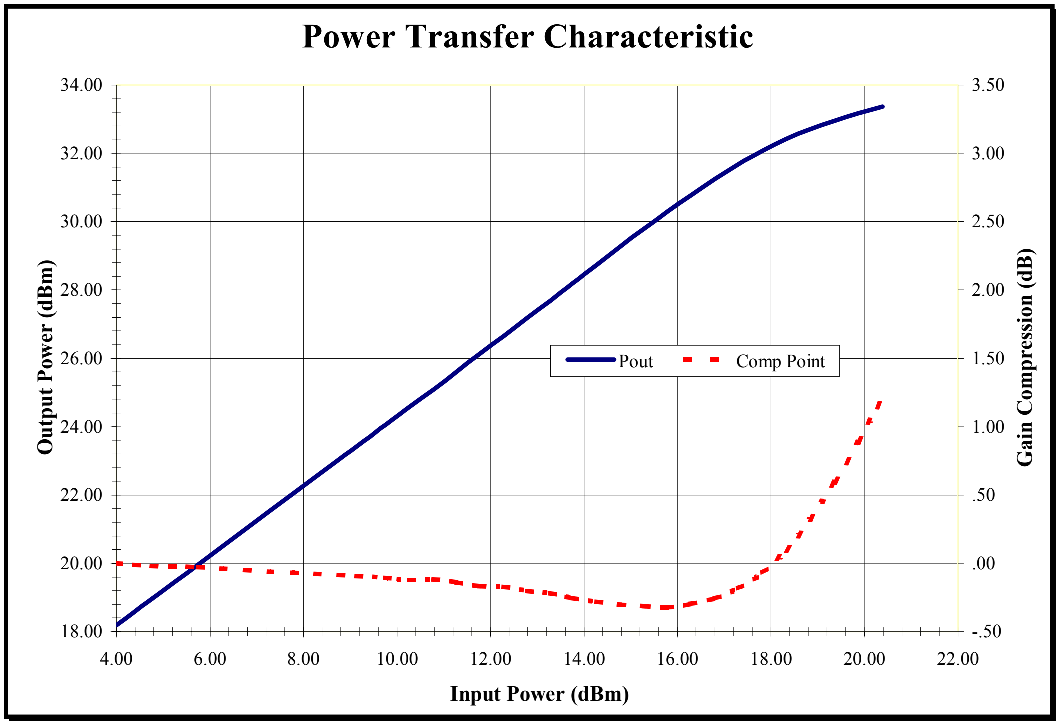


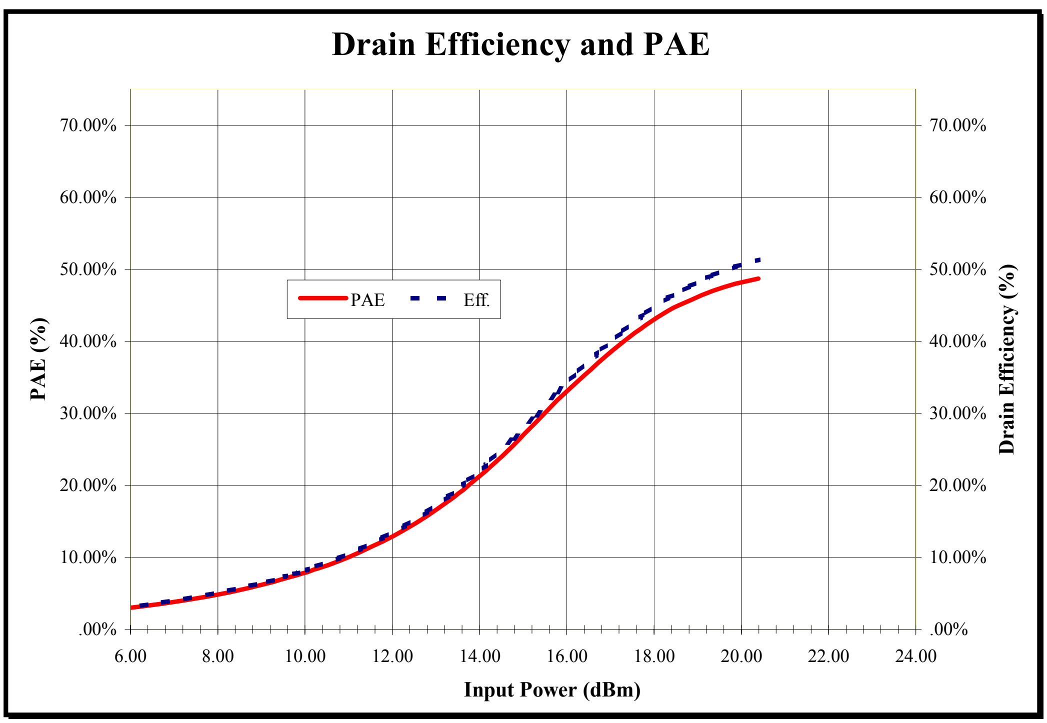
PACKAGE MARKING CODE
Example:
***f*1ZD**
P2F

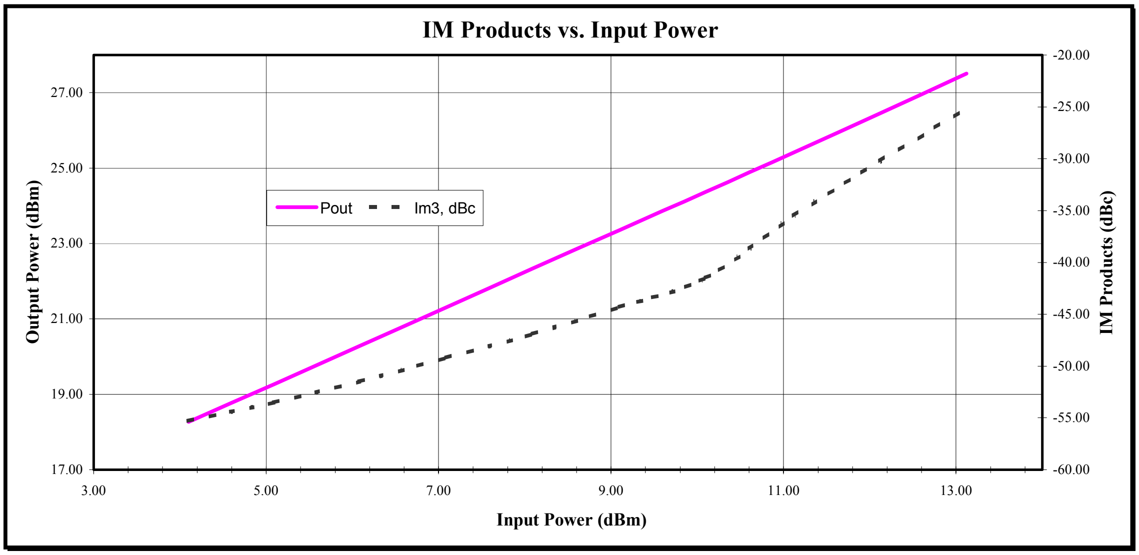
***f* = Filtronic**
1ZD = Lot and Date Code
P2F = Status, Part Code, Part Type

All information and specifications subject to change without notice.

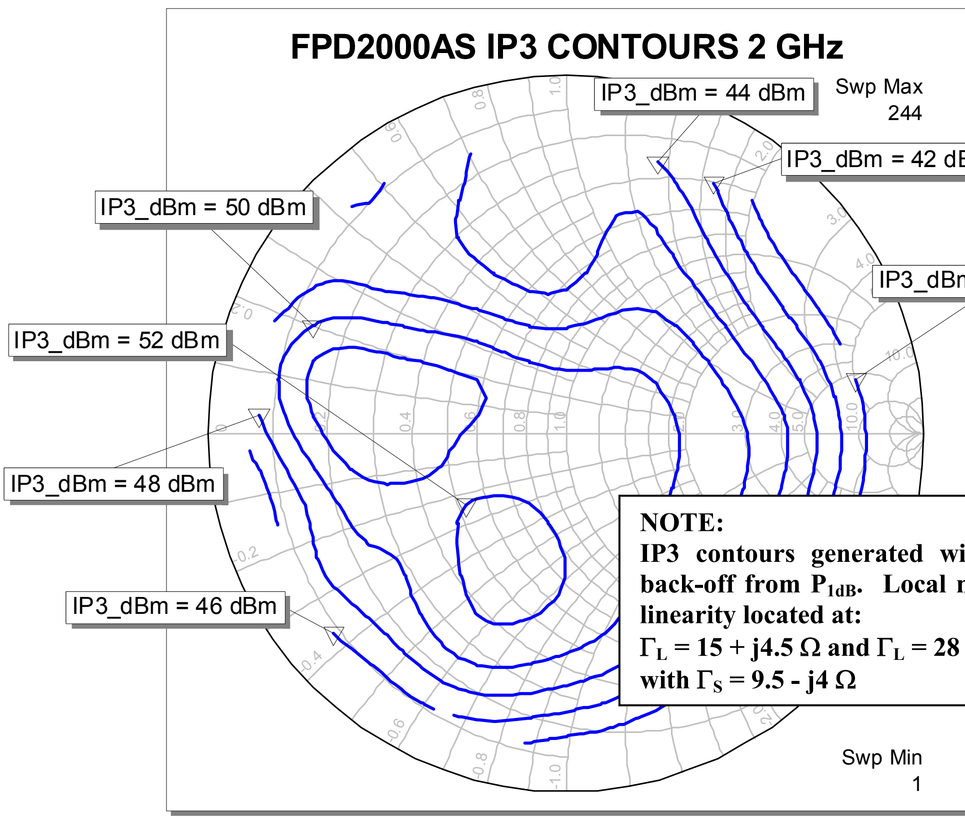
- TYPICAL RF PERFORMANCE (V_{DS} = 10V I_{DS} = 350mA *f* = 2000 MHz):



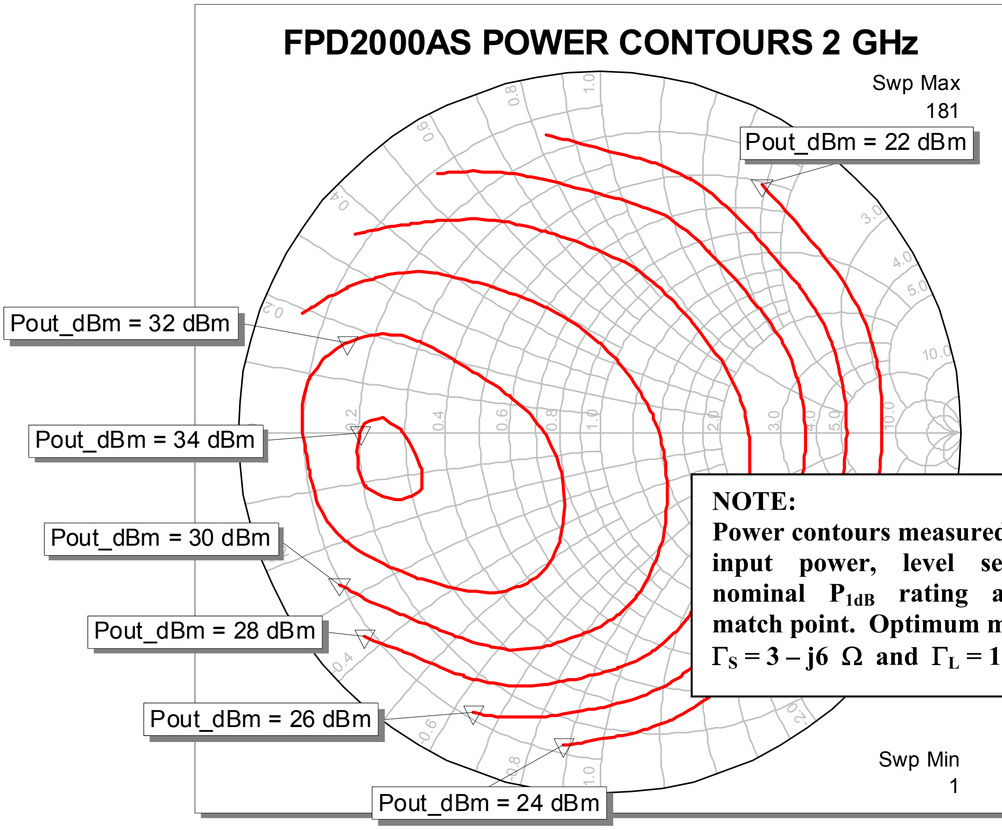




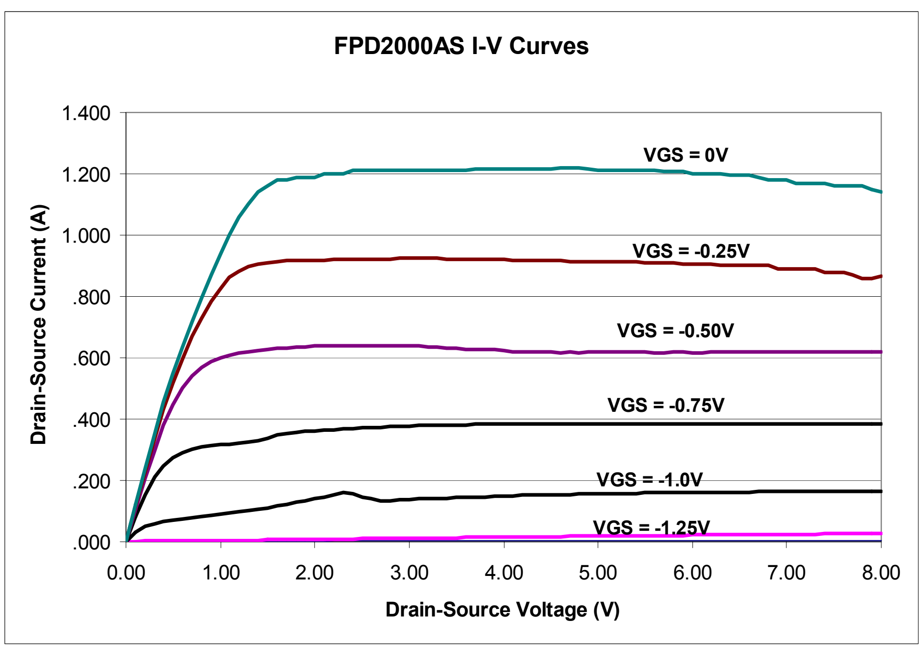
Note: Graph above shows Input and Output power as single carrier or single-tone levels.



NOTE:
IP3 contours generated with P_{IN} = 11dB back-off from P_{1dB}. Local maxima for best linearity located at:
$\Gamma_L = 15 + j4.5\ \Omega$ and $\Gamma_L = 28 – j25\ \Omega$
with $\Gamma_S = 9.5 - j4\ \Omega$



NOTE:
Power contours measured at constant input power, level set to meet nominal P_{1dB} rating at optimum match point. Optimum match: $\Gamma_S = 3 - j6\ \Omega$ and $\Gamma_L = 11 - j3\ \Omega$



- RF PERFORMANCE OVER FREQUENCY: