August 2005

FMS6366
Selectable YPbPr HD/SD 4:2:2 Video Filter Driver with Y, C and Composite Outputs

Features

- Pin-compatible version of the FMS6419 for 4:2:2 video
- Requires external delay compensation
- 6th order standard/high definition video filters
- YPbPr 4:2:2 filters (8/30MHz : 4/15MHz : 4/15MHz)
- YC standard definition filters (8MHz)
- Composite summer output
- DC-coupled inputs, AC-coupled outputs
- Outputs provide 6dB gain to 150Ω AC-coupled loads
- Dual multiplexed inputs
- 0.3% differential gain with 0.1° differential phase
- 5V only
- Lead free (Pb-free) packaging

Applications

- Cable set-top boxes
- Satellite set-top boxes
- DVD players
- HDTV
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

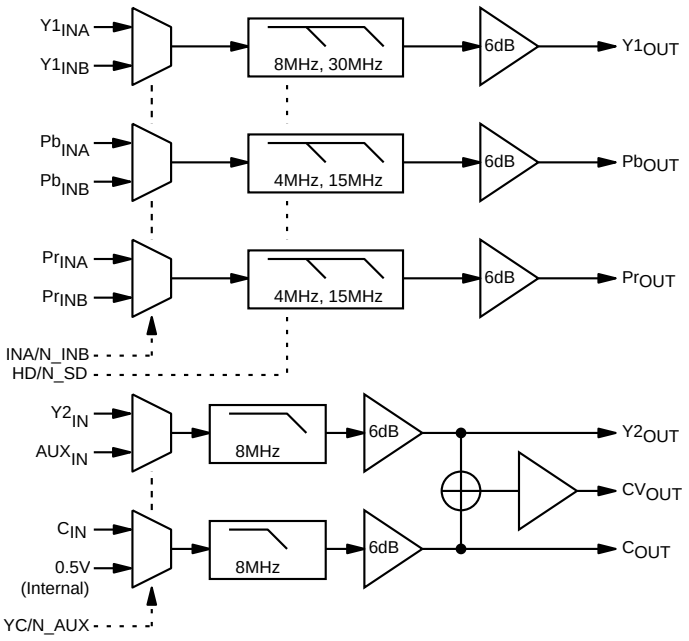
The FMS6366 Filter Driver offers comprehensive filtering for set top box or DVD applications. This part consists of triple 6th order filters with selectable cutoffs for SD or HD. The filters are in a 4:2:2 configuration such that Y1 switches between 8MHz (SD) and 30MHz (HD). The Pb and Pr channels switch between 4MHz (SD) and 15MHz (HD). The required delay compensation must be performed in the digital domain prior to filtering by the FMS6366.

An additional S-video path is provided for SD signals. The Y2 and C signals are both filtered at 8MHz. A composite summer is included to provide a composite output based on Y2 and C.

A 2:1 multiplexer is provided on each filter channel with separate select lines for the YPbPr and YC signals.

All inputs accept DC-coupled ground referenced $1V_{pp}$ input signals. The filter outputs include +6dB of gain resulting in a $2V_{pp}$ signal into an AC-coupled dual video load (75Ω).

Block Diagram



DC Specifications

(T_C = 25°C, V_i = 1V_{PP}; V_{CC} = 5.0V,all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current[1]	V_{CC} no load		125	150	mA
V_i	Input Voltage Max	Reference to ground		1.3		V
V_{il}	Digital Input Low[1]	INA, HD, YC	0		0.8	V
V_{ih}	Digital Input High[1]	INA, HD, YC	2.4		V_{CC}	V
PSRR	PSRR (all channels)	DC		-40		dB

Standard Definition Electrical Specifications

(T_C = 25°C, V_i = 1V_{PP}; V_{CC} = 5.0V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{SD}	SD Gain[1]	All channels	5.4	6.0	6.6	dB
f_{1dBSD4}	-1dB Bandwidth for SD[1]	Y1, Y2, C	4.0	7.4		MHz
f_{1dBSD2}		Pb, Pr	2.0	3.9		MHz
f_{CSD4}	-3dB Bandwidth for SD	Y1, Y2, C		8.5		MHz
f_{CSD2}		Pb, Pr		4.5		MHz
f_{SBSD}	Attenuation: SD (stopband reject)[1]	All channels at f = 27MHz	37	55		dB
dG	Differential Gain	All channels		0.3		%
dϕ	Differential Phase	All channels		0.1		°
THD	Output Distortion (all channels)	V_{OUT} = 1.8V_{pp} at 1MHz		0.15		%
$X_{TALKYPbPr}$	Crosstalk (channel-to-channel)	V_{OUT} = 1.8V_{pp} at 1MHz, YPbPr		-70		dB
$X_{TALKYCCV}$	Crosstalk (channel-to-channel)	V_{OUT} = 1.8V_{pp} at 1MHz, YCCV		-62		dB
IN_{MUXISO}	IN_{MUX} Isolation	V_{IN} = 1V_{pp} at 1MHz		-70		dB
SNR	Signal-to-Noise Ratio	All channels, NTC-7 weighting 4.2MHz lowpass, 100kHz highpass		70		dB
t_{pdSD4}	Input to Output Prop Delay for SD	Y1, Y2, C, CV In to Out at 400kHz		75		ns
t_{pdSD2}		Pb, Pr In to Out at 400kHz		135		ns
$t_{42SDYPbPr}$	4:2:2 Filter delay (compensate in the digital domain)	Y1 to Pb/Pr delay		60		ns
t_{CLDCV}	Chroma-Luma delay CV_{OUT}[1]	f = 3.58MHz	-35	-4	35	ns
t_{CLGCV}	Chroma-Luma gain CV_{OUT}[1]	f = 3.58MHz	95	100	105	%

High Definition Electrical Specifications

(T_C = 25°C, V_i = 1V_{pp}; V_{CC} = 5.0V, HD/N_SD = 1, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AV_{HD}	HD Gain[1]	Y1, Pb, Pr in HD Mode	5.4	6.0	6.6	dB
f_{1dBHD4}	-1dB Bandwidth for HD[1]	Y1	20	27		MHz
f_{1dBHD2}		Pb, Pr	10	14.2		MHz
f_{CHD4}	-3dB Bandwidth for HD	Y1		31.5		MHz
f_{CHD2}		Pb, Pr		16		MHz
f_{SBHD}	Attenuation: HD (stopband reject)[1]	All Channels at f = 74.25MHz	35	40		dB
t_{pdHD4}	Prop Delay for HD	Y1 delay In to Out at 400kHz		25		ns
t_{pdHD2}		Pb, Pr delay In to Out at 400kHz		40		ns

High Definition Electrical Specifications (Continued)

(T_C = 25°C, V_i = 1V_{pp}; V_{CC} = 5.0V, HD/N_SD = 1, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{42HDYPbPr}$	4:2:2 Filter delay (compensate in the digital domain)	Y1 to Pb/Pr delay		15		ns

Note:

1. 100% tested at 25°C

Absolute Maximum Ratings (beyond which the device may be damaged)

Parameter	Min	Max	Units
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} + 0.3	V
Output Current Any One Channel, Do Not Exceed		50	mA

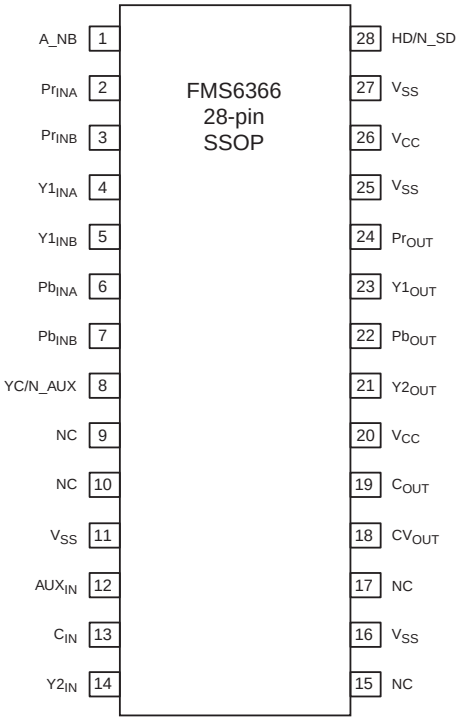
Reliability Information

Parameter	Min	Typ	Max	Units
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance (Θ_{JA}), JEDEC Standard Multi-layer Test Boards, Still Air		47		°C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temperature Range	0		70	°C
V_{CC} Range	4.75	5.0	5.25	V

Pin Configuration



Pin Descriptions

Pin #	Pin	Type	Description
1	A_NB	INPUT	Logic input selects between channel <A> or <B>. (1): A input, (0): B input
2	Pr_{INA}	INPUT	Pr input, channel A
3	Pr_{INB}	INPUT	Pr input, channel B
4	$Y1_{INA}$	INPUT	Y1 (Luminance) input, channel A. Must include sync.
5	$Y1_{INB}$	INPUT	Y1 (Luminance) input, channel B. Must include sync.
6	Pb_{INA}	INPUT	Pb input, channel A
7	Pb_{INB}	INPUT	Pb input, channel B
8	YC/N_AUX	INPUT	Logic input selects between YC and AUX. (1): YC input, (0): AUX input
9	NC		No Connect, leave floating
10	NC		No Connect, leave floating
11	V_{SS}	INPUT	Must be tied to ground, do not float
12	AUX_{IN}	INPUT	Composite video input
13	C_{IN}	INPUT	Chrominance input
14	$Y2_{IN}$	INPUT	Y2 (Luminance) input. Must include sync.
15	NC		No Connect, leave floating
16	V_{SS}	INPUT	Must be tied to ground, do not float
17	NC		No Connect, leave floating
18	CV_{OUT}	OUTPUT	Filtered composite video output
19	C_{OUT}	OUTPUT	Filtered chrominance output
20	V_{CC}	INPUT	+5V supply, do not float
21	$Y2_{OUT}$	OUTPUT	Y2 output
22	Pb_{OUT}	OUTPUT	Pb output
23	$Y1_{OUT}$	OUTPUT	Y1 output
24	Pr_{OUT}	OUTPUT	Pr output
25	V_{SS}	INPUT	Must be tied to ground, do not float
26	V_{CC}	INPUT	+5V supply, do not float
27	V_{SS}	INPUT	Must be tied to ground, do not float
28	HD/N_SD	INPUT	Logic input selects between HD and SD mode. (1): HD, (0): SD

Standard Definition Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{PP}; V_{CC} = 5.0V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 1. Frequency Response Pb, Pr

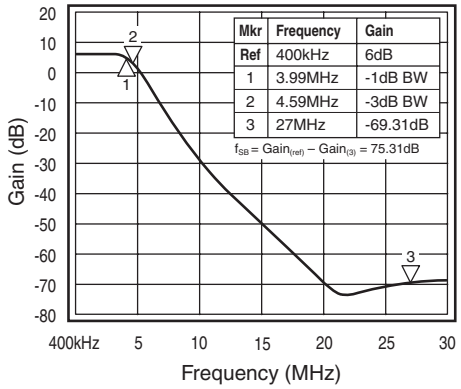


Figure 2. Frequency Response Y1, Y2, C, CV

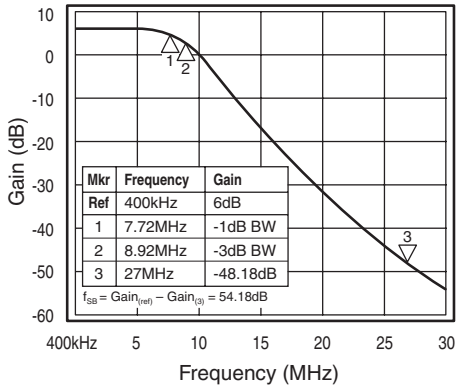


Figure 3. Group Delay vs. Freq. Pb, Pr

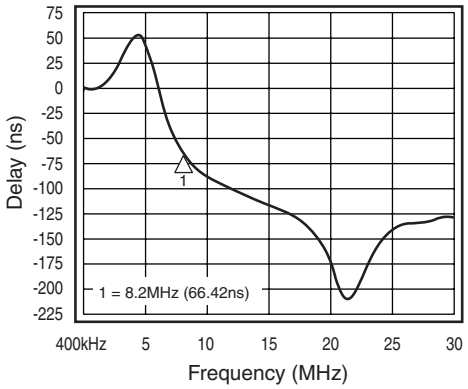


Figure 4. Group Delay vs. Freq. Y1, Y2, C, CV

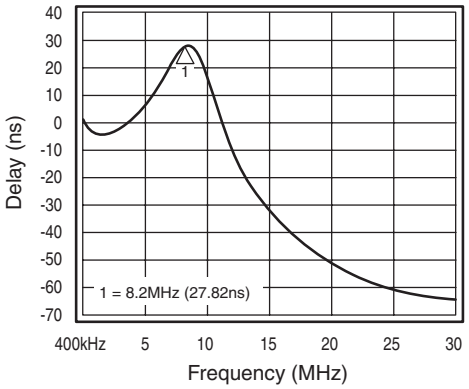


Figure 5. Noise vs. Frequency Pb, Pr

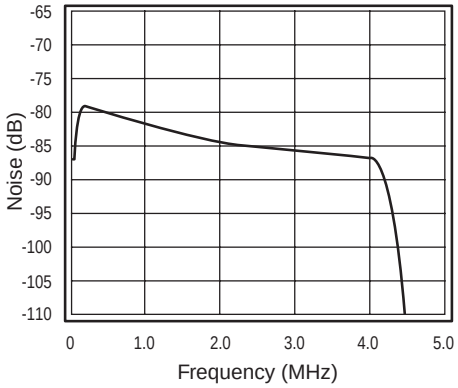
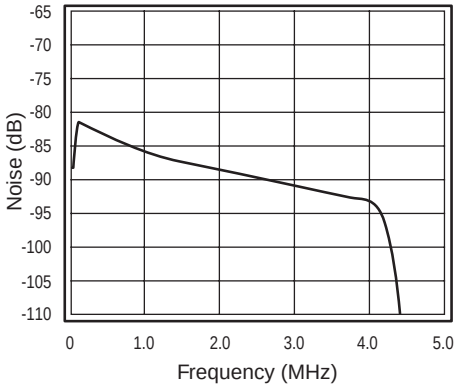


Figure 6. Noise vs. Frequency Y1, Y2, C, CV



Standard Definition Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{PP}; V_{CC} = 5.0V, HD/N_SD = 0, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 7. Differential Gain Pb, Pr

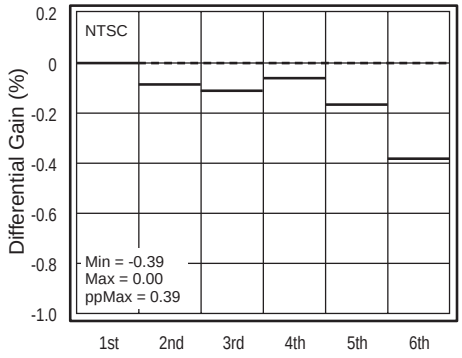


Figure 8. Differential Phase Pb, Pr

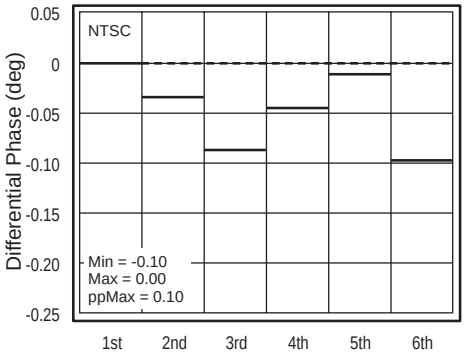


Figure 9. Differential Gain Y1, Y2, C, CV

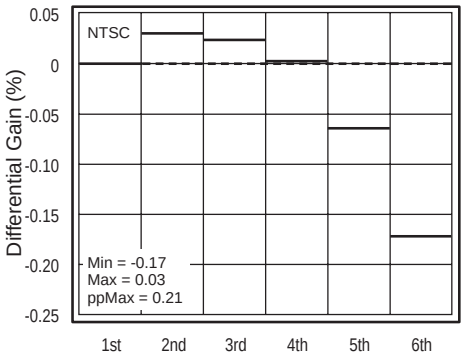


Figure 10. Differential Phase Y1, Y2, C, CV

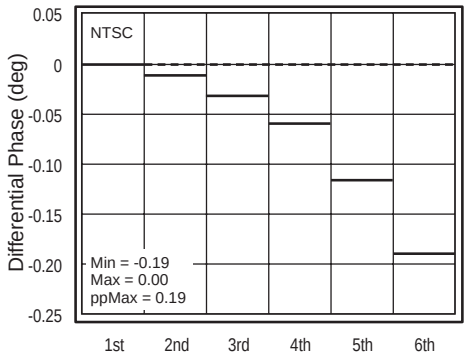
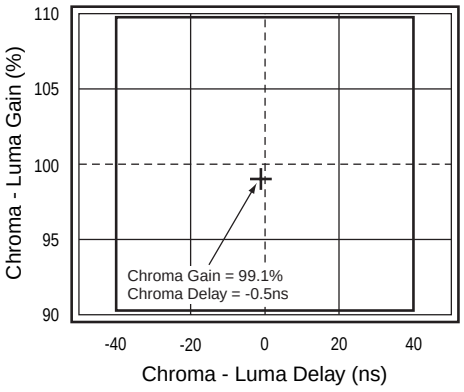


Figure 11. Chroma - Luma Gain vs. Chroma - Luma Delay



High Definition Typical Performance Characteristics

(T_C = 25°C, V_i = 1V_{pp}; V_{CC} = 5.0V, HD/N_SD = 1, R_{SOURCE} = 37.5Ω, all inputs AC coupled with 0.1μF, all outputs AC coupled with 220μF into 150Ω, referenced to 400kHz; unless otherwise noted)

Figure 12. Frequency Response Pb, Pr

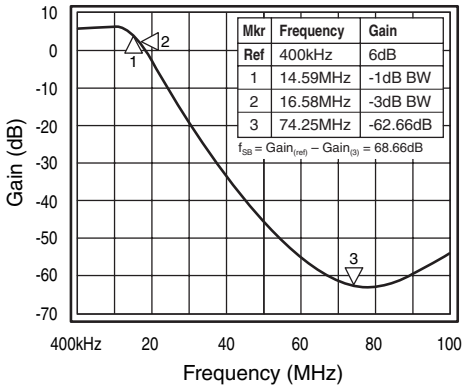


Figure 13. Frequency Response Y1, Y2, C, CV

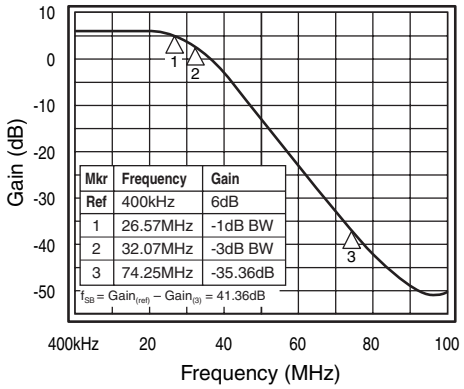


Figure 14. Group Delay vs. Freq. Pb, Pr

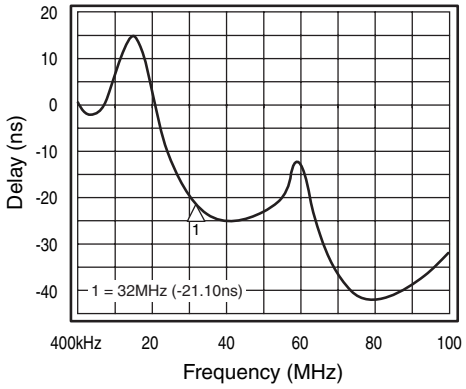
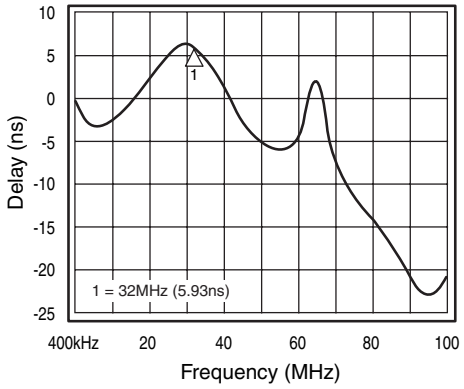


Figure 15. Group Delay vs. Freq. Y1, Y2, C, CV



General Description

The FMS6366 offers comprehensive filtering for set top box or DVD applications. This part consists of triple 4:2:2 6th order filters with selectable 30/15MHz or 8/4MHz frequencies for YPbPr and a dual 8MHz filter for YC with a composite summer. Two-to-one multiplexers are provided on the triple filters as well as provisions for auxiliary input to the composite channel. The triple filters are intended for YPbPr signals. All channels accept DC coupled ground-referenced $1V_{pp}$ signals. The filters output $2V_{pp}$ signals into AC coupled terminated loads.

The FMS6366 is a next generation filter solution from Fairchild Semiconductor addressing the expanding filtering needs for set top boxes, and DVD players. The product provides selectable 4:2:2 HD/SD filtering on the YPbPr channels. Thus, the FMS6366 addresses the requirement for a single set top box to be compatible with a variety of resolution standards. Additionally, the product provides additional filters for Y, C, and Composite Video (CV) outputs. Multiplexers on the YPbPr and CV channels provide further flexibility.

For DVD applications, the product provides filtering and output drive amplification for 6 channels of outputs. These include Y1, Pb, Pr, Y2, C, and CV outputs.

For Set top boxes, this product provides two channels of filtered video with the flexibility of selectable high order filtering for multiple resolution standards. Additional flexibility is provided by the Y (Luma) and C (Chroma) filters with a composite summer.

All channels provide 6dB gain, accept 1V ground referenced inputs, and drive AC coupled loads.

Functional Description

DC Levels

At any given time, the input signal's DC levels must be between 0.0V and 1.3V to utilize the optimal headroom and to avoid clipping at the outputs. The Y channels accept $1V_{pp}$ signals with the sync tip at ground. The Pb, Pr and C channels should be centered around 0.5V. This will ensure that the filter will utilize the optimal headroom and avoid clipping.

DC-Coupled Output Applications

The 220uF capacitor coupled with the 150Ω termination forms a high pass filter that blocks the DC while passing the video frequencies and avoiding tilt. Lower values such as 10uF cause unacceptable tilt in the output signal. By AC coupling, the average DC level is zero. Thus, the output voltages of all channels will be centered around zero.

DC coupling the output of the FMS6366 is allowable, but not recommended. There are several trade-offs: The average DC level on the outputs will be 2V. Each output will dissipate an additional 40mW nominally. The application will need to accommodate a 1V DC offset sync tip. Also, it is recommended to limit one 150Ω load per output.

The FMS6366 is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

Driving Digital Pins

The FMS6366 digital inputs are compatible with most 3.3V and 5V logic. Verify that the V_{ih} and V_{il} are within the specified limits.

Applications

A typical application for the FMS6366 is shown in Figure 16.

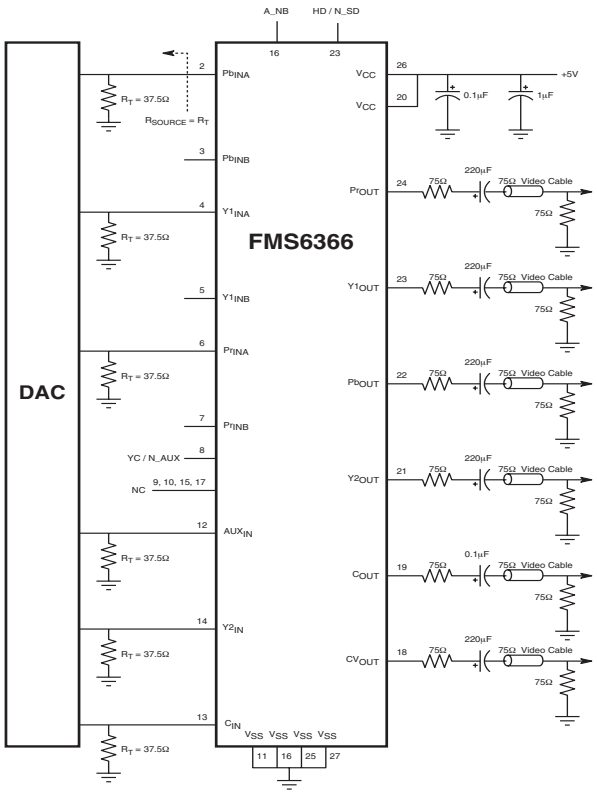


Figure 16. Typical Application Diagram

Digital Delay Compensation

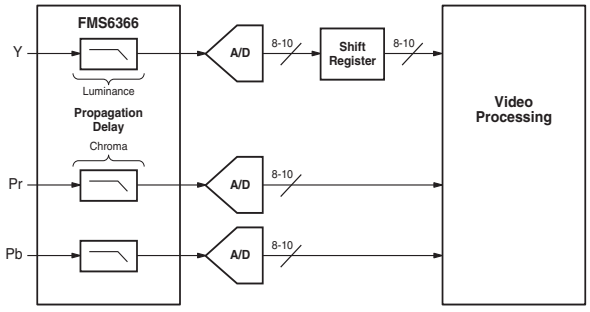


Figure 17. Digital Delay Compensation for anti-alias 4:2:2 filters

The Chroma filters are one half the bandwidth of the Luminance filter therefore the propagation delay time through the Chroma filter is longer than the Luminance filter. In the Standard Definition (SD) case, the Chroma filter propagation delay is typically 60 nanoseconds longer than the Luminance filter. This is three clock cycles at 54MHz so it is easily corrected by adding digital delay as shown in Figure 18 and illustrated as a shift register in Figure 17. In the High Definition (HD) setting the Chroma filter propagation delay is typically 15ns longer than the Luminance filter. This is one clock cycle at 74.25MHz so it is also easily corrected by adding digital delay to the luminance path.

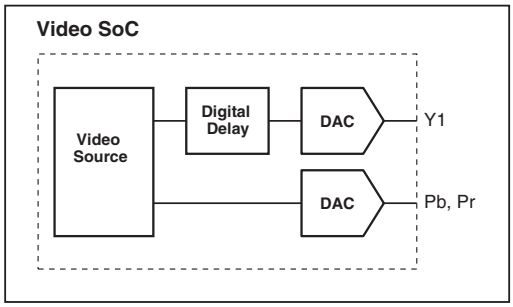
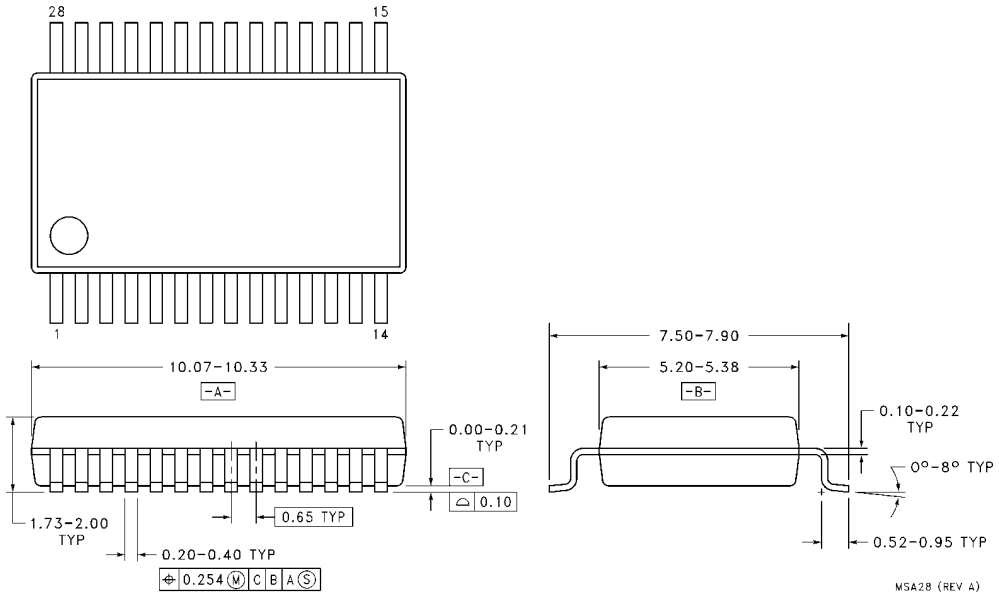


Figure 18. Digital Delay Compensation for 4:2:2 reconstruction filters

Package Dimensions

SSOP-28



Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty
FMS6366	FMS6366MSA28	Yes	SSOP-28	Rail	47
FMS6366	FMS6366MSA28X	Yes	SSOP-28	Reel	2000

Temperature range for all parts: 0˚C to 70˚C.

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CoolFET™	FRFET™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CROSSVOLT™	GlobalOptoisolator™	MicroFET™	PowerTrench®	SuperSOT™-6
DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E²CMOS™	I²C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	*i-Lo*™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
The Power Franchise®		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I15