FAIRCHILD SEMICONDUCTOR®

February 2007

FDMS2734
N-Channel UltraFET Trench® MOSFET
250V, 14A, 122mΩ

Features

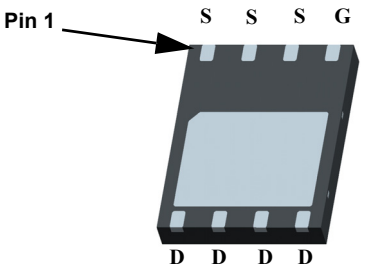
- Max $r_{DS(on)}$ = 122mΩ at V_{GS} = 10V, I_D = 2.8A
- Max $r_{DS(on)}$ = 130mΩ at V_{GS} = 6V, I_D = 1.7A
- Low Miller Charge
- Optimized efficiency at high frequencies
- RoHS Compliant

General Description

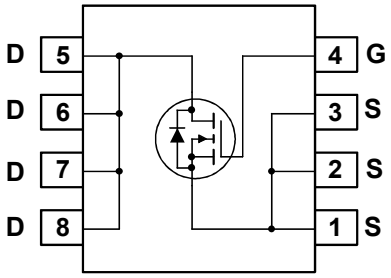
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

Application

- DC - DC Conversion



Power 56 (Bottom view)



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			250	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Silicon limited)	T_C = 25°C		14	A
	-Continuous	T_A = 25°C	(Note 1a)	2.8	
	-Pulsed			16	
P_D	Power Dissipation	T_C = 25°C		78	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

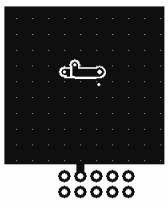
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2734	FDMS2734	Power 56	13”	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	250			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		250		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200V,			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{GS} = 0V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-11		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 2.8A		105	122	mΩ
		V_{GS} = 6V, I_D = 1.7A		110	130	
		V_{GS} = 10V, I_D = 2.8A T_J = 125°C		217	258	
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 2.8A		11		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 100V, V_{GS} = 0V, f = 1MHz		1775	2365	pF
C_{oss}	Output Capacitance			80	110	pF
C_{rss}	Reverse Transfer Capacitance			25	40	pF
R_g	Gate Resistance	f = 1MHz		0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 125V, I_D = 2.8A V_{GS} = 10V, R_{GEN} = 6Ω		22	36	ns
t_r	Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t_f	Fall Time			12	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V, V_{DD} = 125V, I_D = 2.8A		30	42	nC
Q_{gs}	Gate to Source Gate Charge			7		nC
Q_{gd}	Gate to Drain “Miller” Charge			9		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.8A (Note 2)		0.75	1.20	V
t_{rr}	Reverse Recovery Time	I_F = 2.8A, di/dt = 100A/μs		79	119	ns
Q_{rr}	Reverse Recovery Charge			214	321	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics T_J = 25°C unless otherwise noted

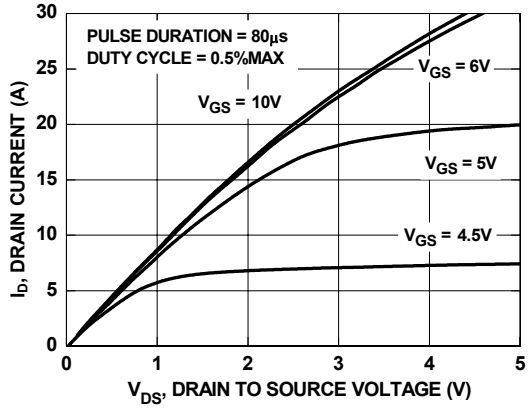


Figure 1. On Region Characteristics

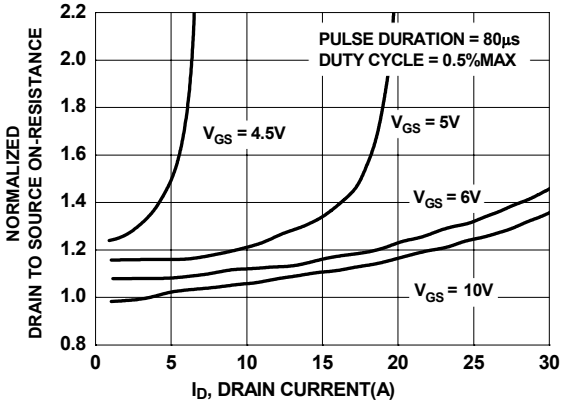


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

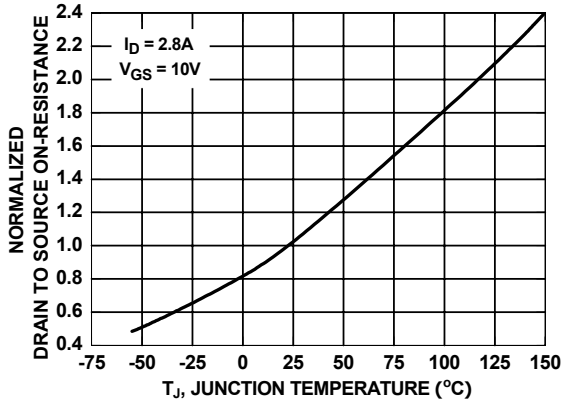


Figure 3. Normalized On Resistance vs Junction Temperature

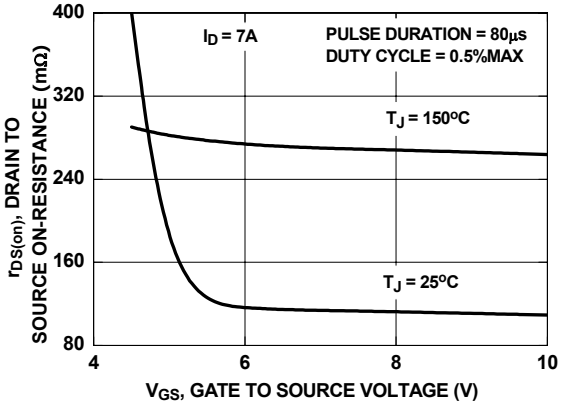


Figure 4. On-Resistance vs Gate to Source Voltage

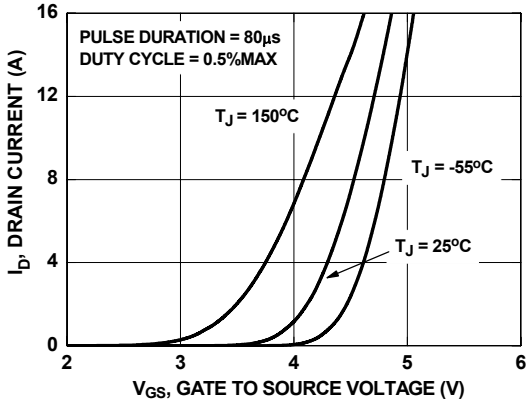


Figure 5. Transfer Characteristics

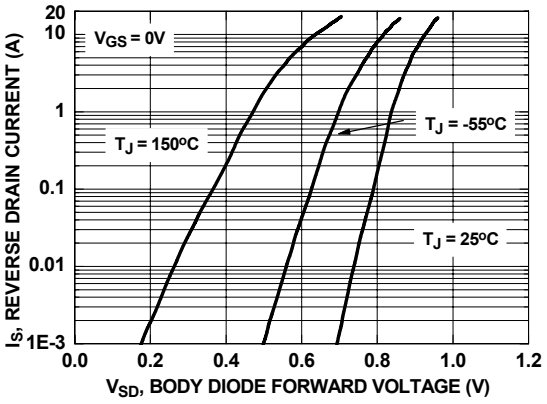


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

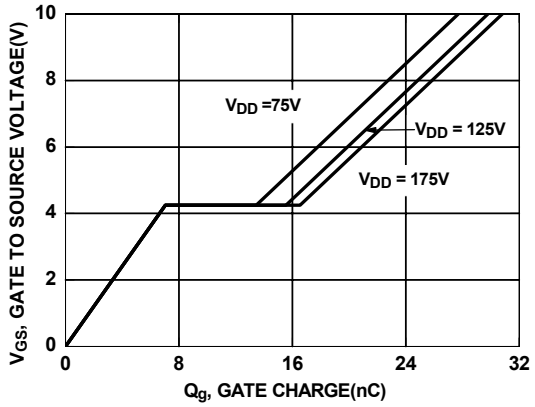


Figure 7. Gate Charge Characteristics

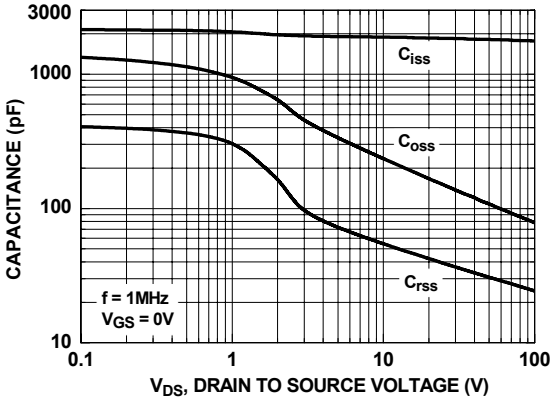


Figure 8. Capacitance vs Drain to Source Voltage

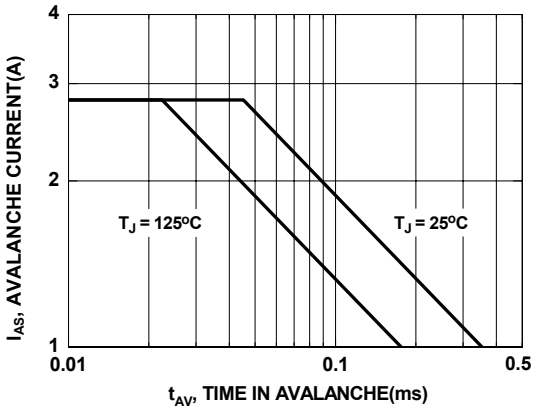


Figure 9. Unclamped Inductive Switching Capability

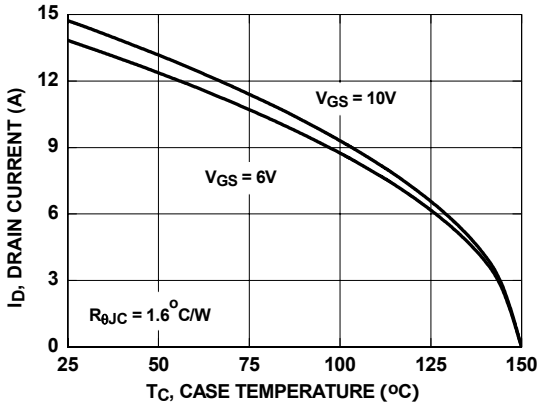


Figure 10. Maximum Continuous Drain Current vs Case Temperature

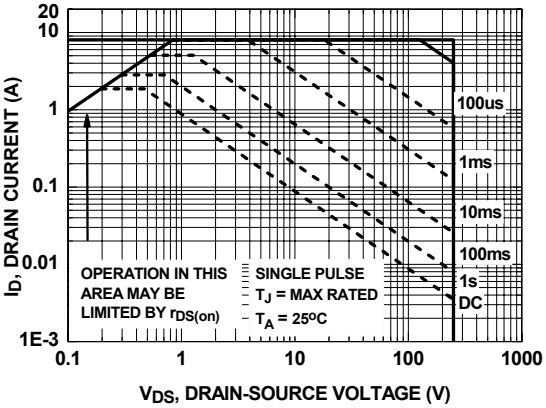


Figure 11. Forward Bias Safe Operating Area

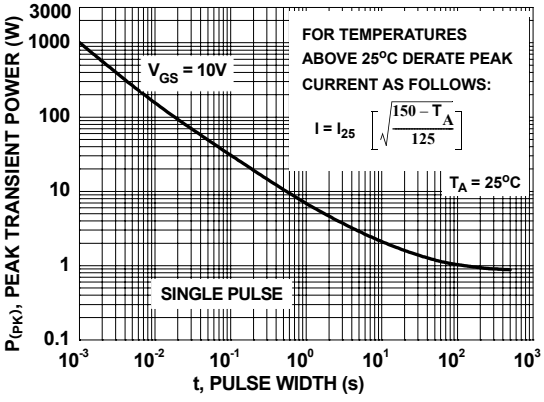


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

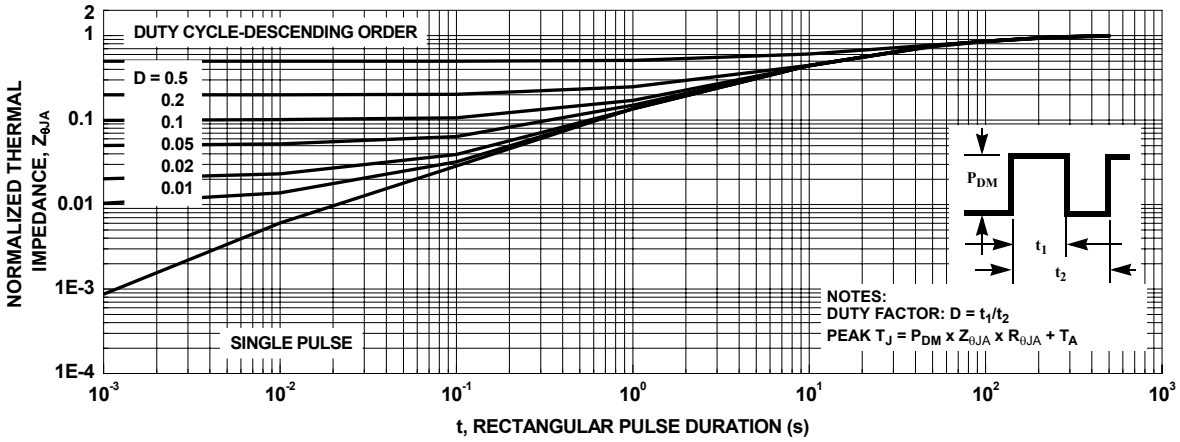
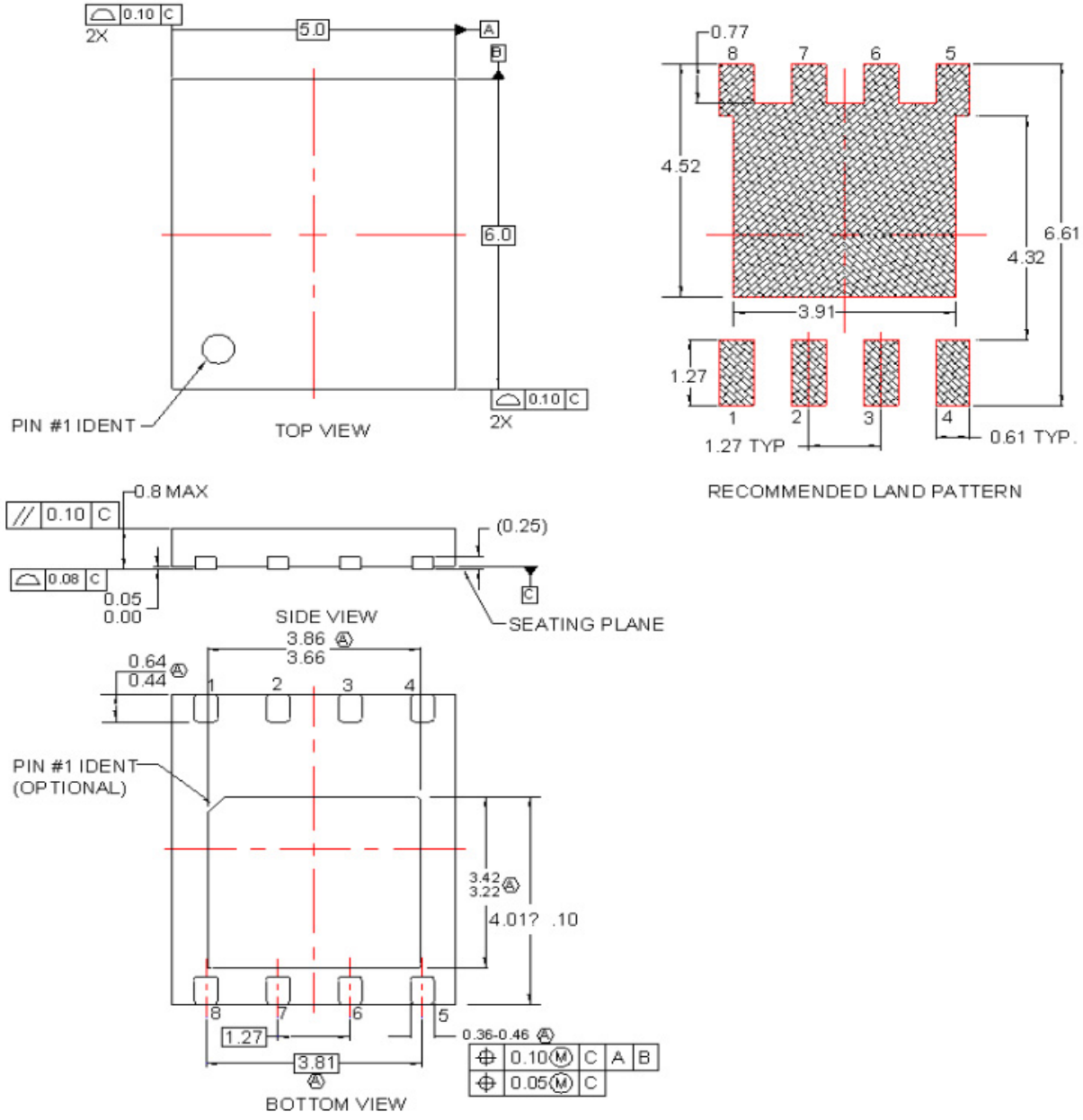


Figure 13. Transient Thermal Response Curve



NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229. DATED 11/2001.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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Definition of Terms

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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