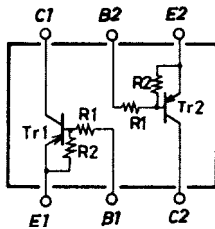


**FC113**

PNP Epitaxial Planar Silicon Composite Transistor

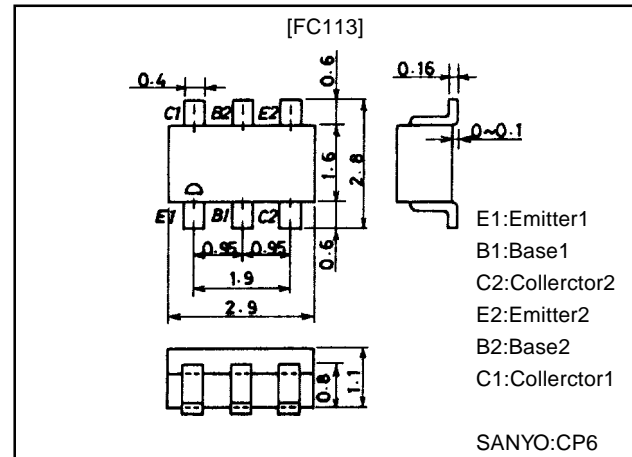
Switching Applications**Features**

- On-chip bias resistors ($R_1=10k\Omega$, $R_2=10k\Omega$)
- Composite type with 2 transistors contained in the CP package currently in use, improving the mounting efficiency greatly.
- The FC113 is formed with two chips, being equivalent to the 2SA1344, placed in one package.
- Excellent in thermal equilibrium and pair capability.

Electrical Connection**Package Dimensions**

unit:mm

2067

**Specifications****Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		-50	V
Collector-to-Emitter Voltage	V_{CEO}		-50	V
Emitter-to-Base Voltage	V_{EBO}		-10	V
Collector Current	I_C		-100	mA
Collector Current (Pulse)	I_{CP}		-200	mA
Collector Dissipation	P_C	1 unit	200	mW
Total Dissipation	P_T		300	mW
Junction Temperature	T_j		150	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to+150	$^\circ\text{C}$

Electrical Characteristics at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB}=-40\text{V}$, $I_E=0$			-0.1	μA
Collector Cutoff Current	I_{CEO}	$V_{CE}=-40\text{V}$, $I_B=0$			-0.5	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=-5\text{V}$, $I_C=0$	-170	-250	-360	μA
DC Current Gain	h_{FE}	$V_{CE}=-5\text{V}$, $I_C=-10\text{mA}$	50			
Gain-Bandwidth Product	f_T	$V_{CE}=-10\text{V}$, $I_C=-5\text{mA}$		200		MHz
Output Capacitance	C_{ob}	$V_{CB}=-10\text{V}$, $f=1\text{MHz}$		5.1		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=-10\text{mA}$, $I_B=-0.5\text{mA}$		-0.1	-0.3	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C=-10\mu\text{A}$, $I_E=0$	-50			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C=-100\mu\text{A}$, $R_{BE}=\infty$	-50			V
Input OFF-State Voltage	$V_{I(off)}$	$V_{CE}=-5\text{V}$, $I_C=-100\mu\text{A}$	-0.8	-1.1	-1.5	V
Input ON-State Voltage	$V_{I(on)}$	$V_{CE}=-0.2\text{V}$, $I_C=-10\text{mA}$	-1.0	-2.0	-4.0	V
Input Resistance	R_1		7.0	10	13	$k\Omega$
Resistance Ratio	R_1/R_2		0.9	1.0	1.1	

Note: The specifications shown above are for each individual transistor.

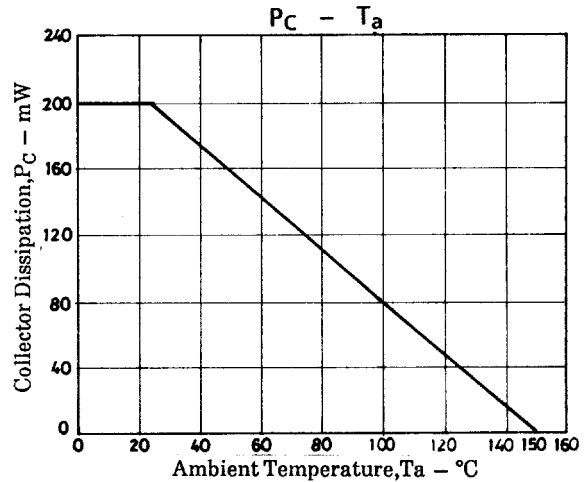
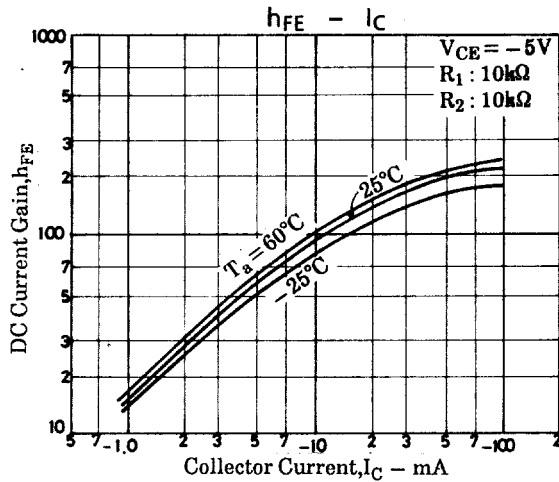
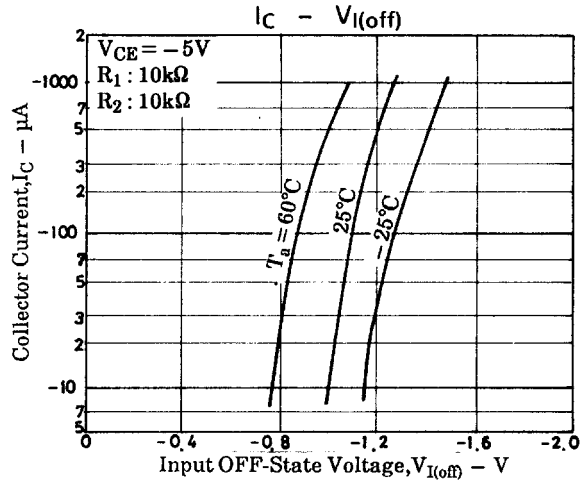
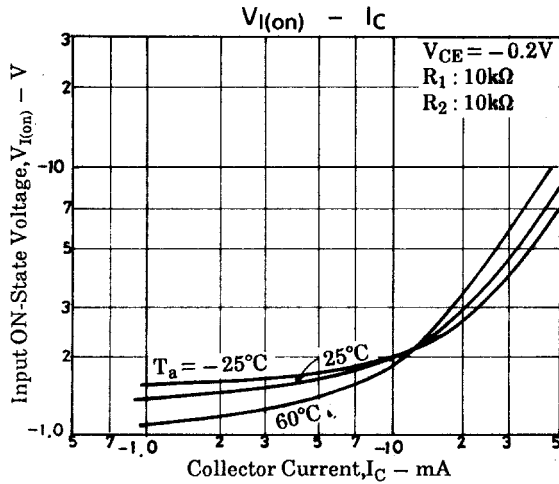
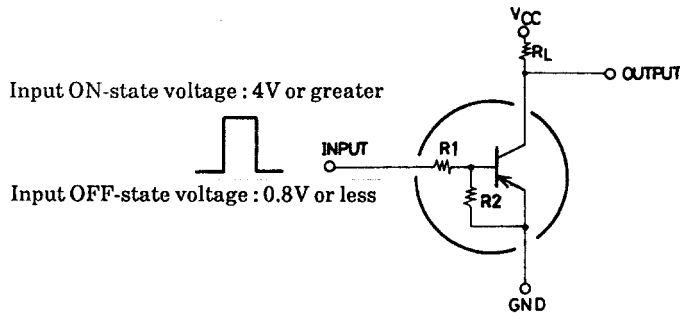
Marking:113

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

52098HA (KT)/4139MO, TS No.3081-1/2

Sample Application Circuit



■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

- ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use:
- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of May, 1998. Specifications and information herein are subject to change without notice.