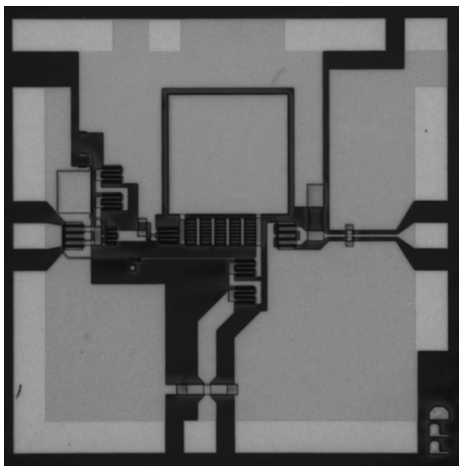
SUMITOMO ELECTRIC

02.03.04

F0100604B

10 Gb/s Receiver

Transimpedance Amplifier



♦ *Features*

- Low voltage of +5.0 /-3.5V power supply
- 400 Ω high transimpedance
- Typical 9.0 GHz broad bandwidth
- 17.0 dB high gain
- Over 18 dB wide dynamic range
- Excellent equivalent input noise current of 10 pA/Hz$^{1/2}$

♦ *Applications*

- Preamplifier of an optical receiver circuit for STM-64/OC-192 (10 Gb/s)

♦ *Functional Description*

The F0100604B is a stable GaAs integrated transimpedance amplifier capable of 17.0 dB gain at a typical 9.0 GHz 3 dB-cutoff-frequency, making it ideally suited for a 10 Gb/s optical receiver circuit, for example, OC-192/STM-64, instrumentation, and measurement applications. The integrated feedback loop design provides broad bandwidth and stable operation.

Only chip-shipment is available for all product lineups of GaAs transimpedance amplifiers, because the packaged preamplifier can not operate with the maximum performance owing to parasitic capacitance of the package.

♦ *Absolute Maximum Ratings*

T_a=25 °C, unless specified

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	-0.5 to 7.0	V
Supply Voltage	V_{SS}	-4.0 to +0.5	V
Supply Current	I_{DD}	160	mA
Supply Current	I_{SS}	-60	mA
Ambient Operating Temperature	T_a	-40 to +90	° C
Storage Temperature	T_{stg}	-50 to +125	° C

♦ *Recommended Operating Conditions*

T_a=25 °C, V_{DD}=+5.0 V, V_{SS}=-3.5 V, unless specified

Parameter	Symbol	Value		Units
		Min.	Max.	
Supply Voltage	V_{DD}	4.75	5.25	V
Supply Voltage	V_{SS}	-3.68	-3.32	V
Ambient Operating Temperature	T_a	0	70	° C

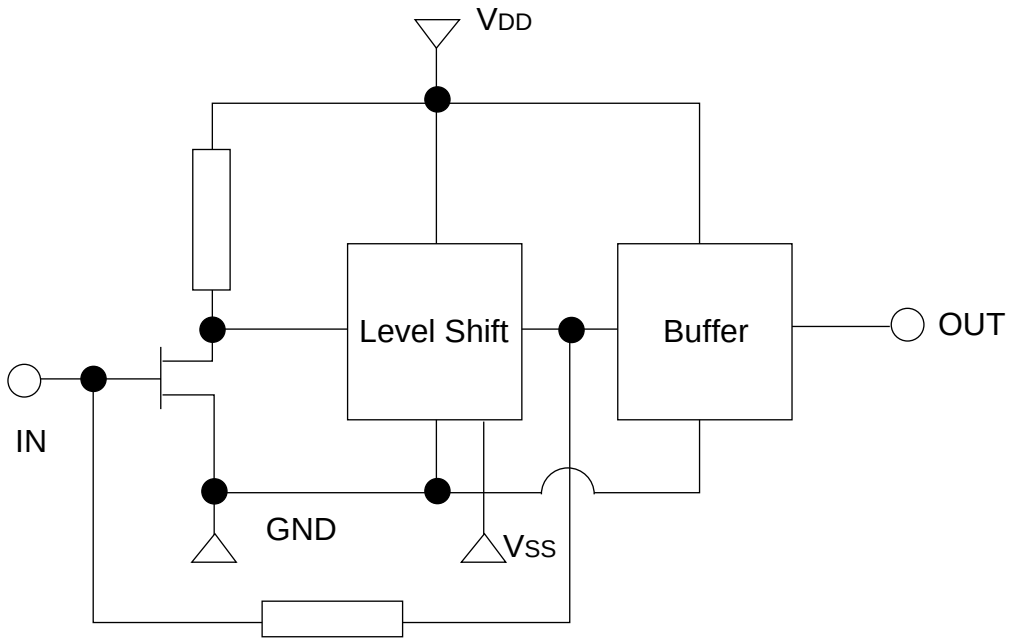
♦ *Electrical Characteristics*

T_a=25 °C, V_{DD}=+5.0 V, V_{SS}=-3.5 V, unless specified

Parameter	Symbol	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Supply Current	I_{DD}	DC	-	100	-	mA
	I_{SS}		-	30	-	
Gain	S_{21}	PIN=-20dBm f=1GHz, RL=50Ω	-	17.0	-	dB
-3dB High Frequency Cut-off	F_C	PIN=-20dBm RL=50Ω	-	9.0	-	GHz
Input Impedance	R_I	f=1GHz	-	55		Ω
Trans-Impedance	Z_T	*1 f=1GHz	-	400	-	Ω
Output Voltage	V_O	DC	-	1.6	-	V
Input Voltage	V_I	DC	-	0.2	-	V

*1 $Z_T = \frac{R_I+50}{2} \times 10^{\frac{S_{21}}{20}}$

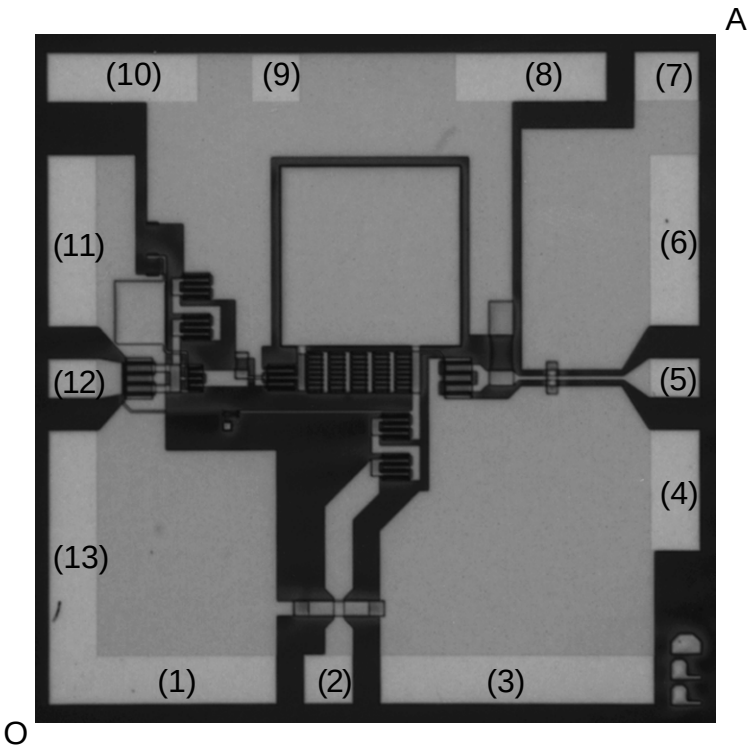
♦ *Block Diagram*



♦ *Die Pad Description*

V_{DD}	Supply Voltage
V_{SS}	Supply Voltage
GND	Ground
IN	Input
OUT	Output

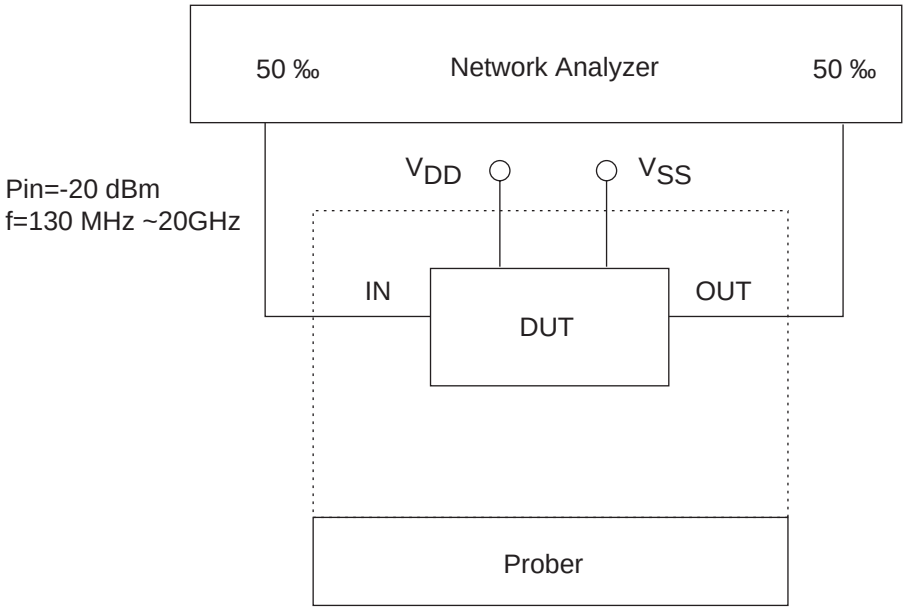
♦ *Die Pad Assignments*



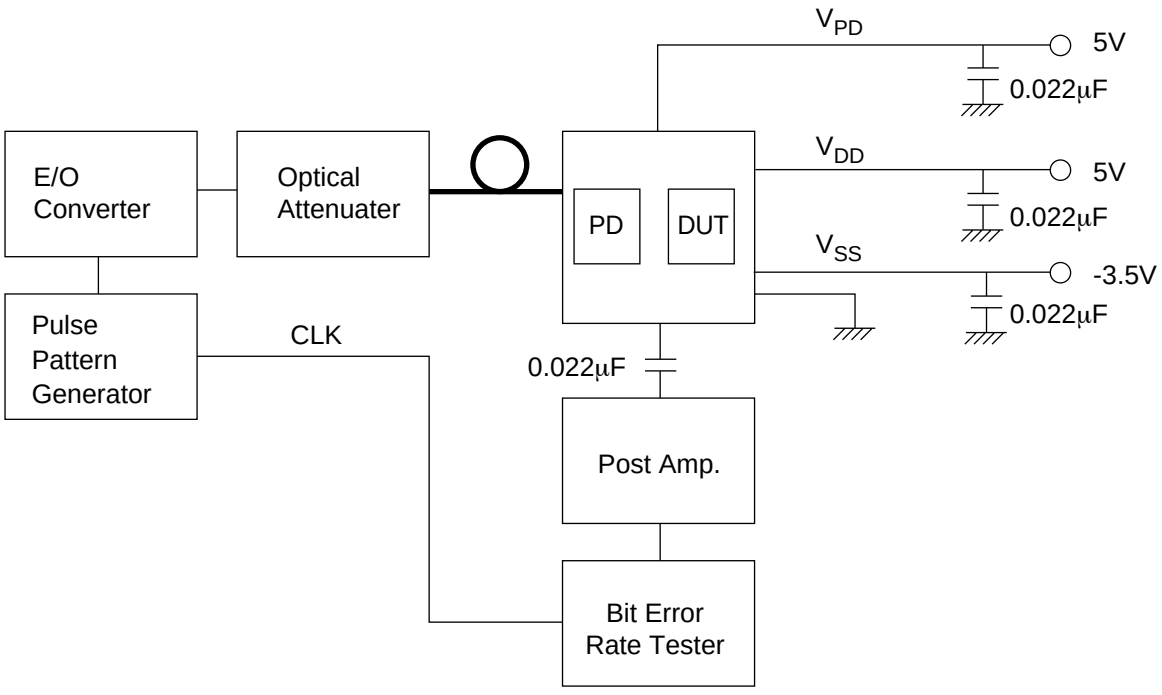
No.	Symbol	Center Coordinates(μm)	No.	Symbol	Center Coordinates(μm)
(1)	GND	(375,100)	(10)	V_{DD}	(200,1280)
(2)	V_{SS}	(600,100)	(11)	GND	(100,960)
(3)	GND	(970,100)	(12)	IN	(100,690)
(4)	GND	(1280,470)	(13)	GND	(100,320)
(5)	OUT	(1280,690)			
(6)	GND	(1280,960)			
(7)	GND	(1265,1280)			
(8)	V_{DD}	(1000,1280)	O		(0,0)
(9)	V_{DD}	(500,1280)	A		(1380,1380)

♦ *Test Circuits*

1) AC Characteristics



2) Sensitivity Characteristics

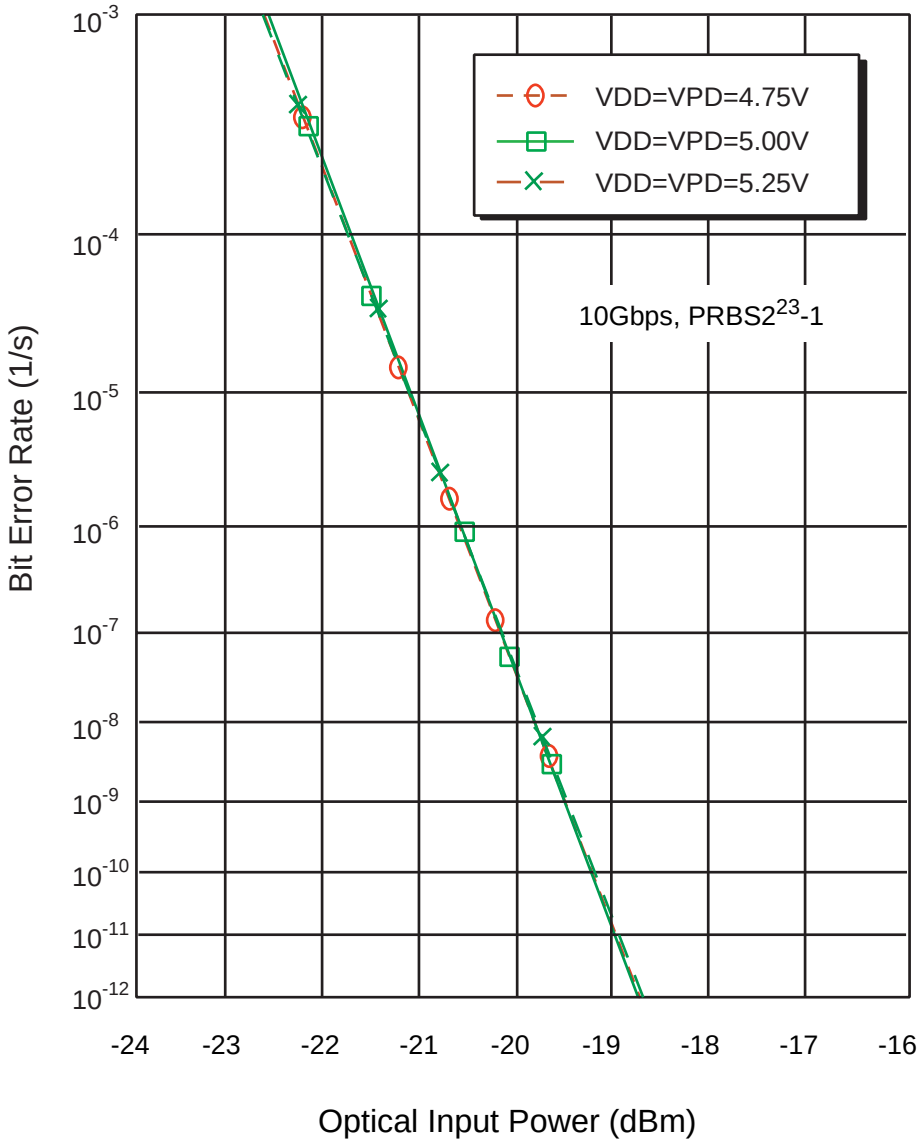


♦ *Examples of AC Characteristics*

(1) Gain (S_{21})

(2) Input Noise Current Density & Transimpedance

♦ *Typical Bit Error Rate*



C_{PD}=0.25pF

♦ *General Description*

A transimpedance amplifier is applied as a pre-amplifier which is an amplifier for a faint photo-current from a PIN photo diode (PD). The performance in tems of sensitivity, bandwidth, and so on, obtained by this transimpedance amplifier strongly depend on the capacitance brought at the input terminal; therefore, “typical”, “minimum”, or “maximum” parameter descriptions can not always be achieved according to the employed PD and package, the assembling design, and other technical experts. This is the major reason that there is no product lineup of packaged transimpedance amplifiers.

Thus, for optimum performance of the transimpedance amplifier, it is essential for customers to design the input capacitance carefully .

Hardness to electro-magnetic interference and fluctuation of a power supply voltage is also an important point of the design, because very faint photo-current flows into the transimpedance amplifier. Therefore, in the assembly design of the interconnection between a PD and a transimpedance, noise should be taken into consideration.

♦ *Die-Chip Description*

The F0100604B is shipped like the die-chip described above. The die thickness is typically 600 μm ± 20 μm with the available pad size uncovered by a passivation film of 95 μm square. The material of pads is TiW/Pt/Au and the backside is metalized by Ti/Au.

♦ *Assembling Condition*

SEI recommends the assembling process as shown below and affirms sufficient wire-pull and die-shear strength. The heating time of one minute at the temperature of 310 °C gave satisfactory results for die-bonding with AuSn performs. The heating and ultrasonic wire-bonding at the temperature of 150 °C by a ball-bonding machine is effective.

♦ *Quality Assurance*

For the F01 series products, there is only one technically inevitable drawback in terms of quality assurance which is to be impossible of the burn-in test for screening owing to die-shipment. SEI will not ship them if customers do not agree on this point. On the other hand, the lot assurance test is performed completely without in any problems according to SEI's authorized rule. A microscope inspection is conducted in conformance with the MIL-STD-883C Method 2010.7.

♦ *Precautions*

Owing to their small dimensions, the GaAs FET's from which the F0100604B is designed are easily damaged or destroyed if subjected to large transient voltages. Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static-electricity-charged operations or ungrounded equipment.