*January 1996, Rev C* **FN7299**

## 100V Half Bridge Driver

*élantec*

The EL7761 provides a low cost solution to many half bridge applications. The EL7761 is DC coupled so that there are no start up problems associated with AC coupled schemes. A single resistor from $D_{SET}$ to GND provides "dead time" programmability. Shorting $D_{SET}$ to $V_{DD}$ gives the shortest delay (~100ns).
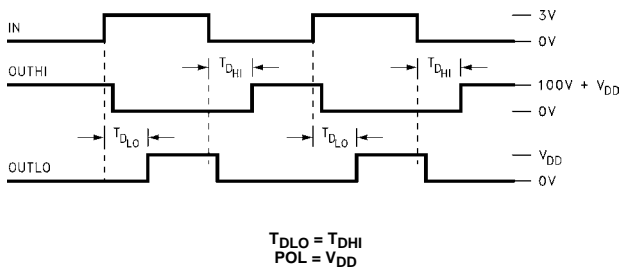
The POL pin controls the polarity of the low side driver. The polarity of the upper driver is always inverting. The EN pin, when low, forces the high and low side outputs into their low state.

## Pinout

**EL7761**
**(16-PIN PDIP, SOIC)**
TOP VIEW
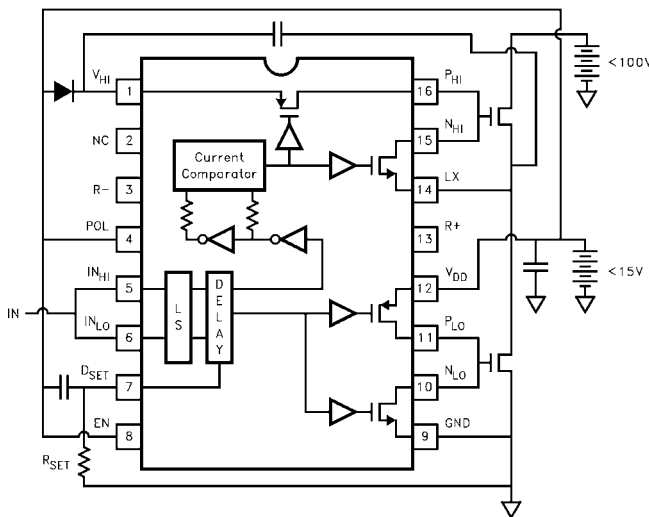


**EL7761 WAVEFORM EXAMPLE**



$T_{DLO} = T_{DHI}$
POL = $V_{DD}$

## Features

- 100V High Side Voltage
- Programmable Delay
- Direct Coupled
- No Start Up Ambiguity
- Rail to Rail Output
- 1MHz Operation
- Shutdown Function
- 1.0 Amp Peak Current
- Improved Response Times
- Matched Rise and Fall Times
- Low Supply Current
- Low Output Impedance
- Low Input Capacitance

## Applications

- Uninterruptible Power Supplies
- Distributed Power Systems
- IGBT Drive
- DC-DC Converters
- Motor Control
- Power MOSFET Drive
- Switch Mode Power Supplies

## Ordering Information

| PART NUMBER | TEMP. RANGE | PACKAGE | PKG. NO. |
|---|---|---|---|
| EL7761CN | -40°C to +85°C | 16-Pin PDIP | MDP0031 |
| EL7761CS | -40°C to +85°C | 16-Pin SOIC | MDP0027(Note) |

NOTE: Contact factory

| | POL | POLARITY |
|---|---|---|
| Low Side | GND<br>$V_{DD}$ | Inverting<br>Non-Inverting |
| Hi Side | X | Inverting |

## Absolute Maximum Ratings $(T_A = 25°C)$

Supply ($V_{HI}$ to GND) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .100V
Supply ($V_{DD}$ to GND) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 16.5V
Input Pins. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3V below GND,
. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .+0.3V above $V_{DD}$
Peak Current per Output . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .2A

Storage Temperature Range . . . . . . . . . . . . . . . . . . .-65°C to +150°C
Ambient Operating Temperature . . . . . . . . . . . . . . . .-40°C to +85°C
Operating Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . 125°C
Power Dissipation
SOIC . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1100mW
PDIP . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .1800mW

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$*

## DC Electrical Specifications $T_A = 25°C$, $V_{DD} = 15V$, $C_{LOAD} = 1000pF$, unless otherwise specified

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT/OUTPUT** | | | | | | |
| $V_{IH}$ | Logic "1" Input Voltage | | 3.0 | 2.4 | | V |
| $I_{IH}$ | Logic "1" Input Current | | | 0.1 | 10.0 | µA |
| $V_{IL}$ | Logic "0" Input Voltage | | | 1.8 | 0.8 | V |
| $I_{IL}$ | Logic "0" Input Current | | | 0.1 | 10.0 | µA |
| $V_{HVS}$ | Input Hysteresis | | | 0.5 | | V |
| $V_{ENH}$ | Enable Threshold | Positive Edge | 2.8 | 1.6 | | V |
| $V_{ENL}$ | Disable Threshold | Negative Edge | | 0.9 | 0.6 | V |
| $V_{EN HYS}$ | Enable Hysteresis | | | 0.7 | | V |
| $I_{DS OFF}$ | Output Leakage | $GND \leq V_{OUT} \leq V_{DD}$ | -10.0 | 0.2 | 10.0 | µA |
| $R_{OH}$ | Pull-up Resistance | $I_{OUT} = -100mA$ | | 5.0 | 10.0 | $\Omega$ |
| $R_{OL}$ | Pull-down Resistance | $I_{OUT} = +100mA$ | | 5.0 | 10.0 | $\Omega$ |
| $I_{PK}$ | Peak Output Current | | | 1.0 | | A |
| $I_{DC}$ | Continuous Output Current Source/Sink | | 50.0 | | | mA |
| **POWER SUPPLY** | | | | | | |
| $I_{DD}$ | Supply Current into $V_{DD}$ | $R_{SET} = 5.1k$ | | 6.0 | 10.0 | mA |
| $I_{HI}$ | Supply Current into $V_{HI}$ | | | 2.0 | 4.0 | mA |
| $I_{DD OFF}$ | Supply Current into $V_{DD}$ | $V_{EN} = 0.6V$ | | | 750.0 | uA |
| $V_{DD}$ | Operating Voltage | | 4.5 | | 15.0 | V |

**AC Electrical Specifications**  $T_A$ = 25°C, $V_{DD}$ = 15V, $C_{LOAD}$ = 1000pF, unless otherwise specified

| PARAMETER | DESCRIPTION | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_R$ | Rise Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | 15.0<br>20.0 | <br>40.0 | ns |
| $t_F$ | Fall Time | $C_L$ = 500pF<br>$C_L$ = 1000pF | | 15.0<br>20.0 | <br>40.0 | ns |
| $t_{D\ ON\ HI}$ | High Side Turn On Delay Time | $D_{SET}$ = $V_{DD}$<br>$R_{SET}$ = 5.1k<br>$R_{SET}$ = 400k | 50.0<br>75.0<br>750.0 | 100.0<br>125.0<br>1150.0 | 150.0<br>200.0<br>1500.0 | ns |
| $t_{D\ ON\ LO}$ | Low Side Turn On Delay Time | $D_{SET}$ = $V_{DD}$<br>$R_{SET}$ = 5.1k<br>$R_{SET}$ = 400k | 50.0<br>75.0<br>750.0 | 100.0<br>125.0<br>1150.0 | 150.0<br>200.0<br>1500.0 | ns |
| $t_{D\ OFF\ HI}$ | High Side Turn Off Delay Time | $D_{SET}$ = $V_{DD}$ | | 100.0 | 150.0 | ns |
| $t_{D\ OFF\ LO}$ | Low Side Turn Off Delay Time | $D_{SET}$ = $V_{DD}$ | | 100.0 | 150.0 | ns |
| $t_{D\ MISMATCH}$ | High to Lo Side Turn On Delay Mismatch | $R_{SET}$ = 400k | | | ±10.0 | % |

## *Pin Descriptions*

| PIN # | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{HI}$ | Positive supply for the high side driver. |
| 2 | NC | |
| 3 | $R^-$ | Internal connection between the low side and high side driver. This pin is normally unconnected. |
| 4 | $P_{OL}$ | Controls the polarity of the low side driver. |
| 5 | $IN_{HI}$ | Logic input for the high side driver. |
| 6 | $IN_{LO}$ | Logic input for the low side driver. |
| 7 | $D_{SET}$ | Connection for the delay adjust resistor. |
| 8 | EN | A high voltage on this pin enables the part. |
| 9 | GND | Negative supply of the low side driver and control circuitry. |
| 10 | $N_{LO}$ | Low side driver output pull down. |
| 11 | $P_{LO}$ | Low side driver output pull up. |
| 12 | $V_{DD}$ | Positive supply of the low side driver and control circuitry. |
| 13 | $R^+$ | Internal connection between the low side and high side driver. This pin is normally unconnected. |
| 14 | LX | Negative supply for the high side driver. |
| 15 | $N_{HI}$ | High side driver output pull down. |
| 16 | $P_{HI}$ | High side driver output pull up. |

# *Typical Performance Curves*

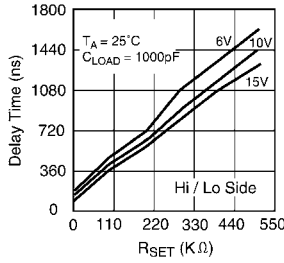**Quiescent Supply Current vs. Supply Voltage**
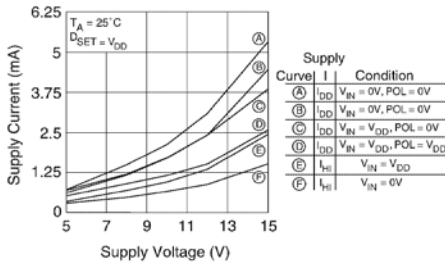
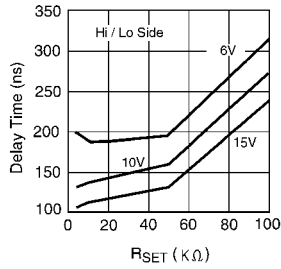**Avg. Supply Current into V_DD vs. Voltage and Frequency**
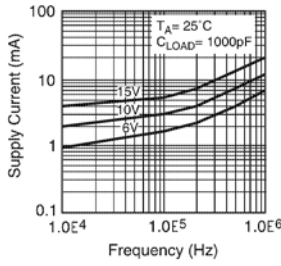
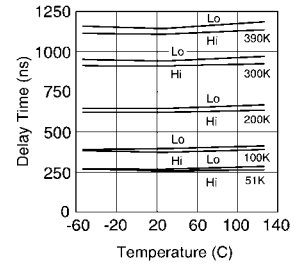**Average Supply Current into V_HI vs. Voltage and Frequency**
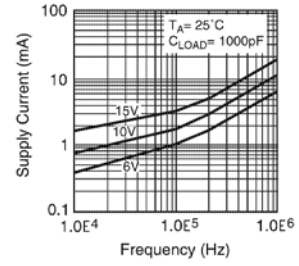
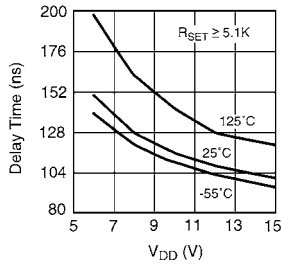**Output Rising Edge Delay vs. R_SET and Supply Voltage**

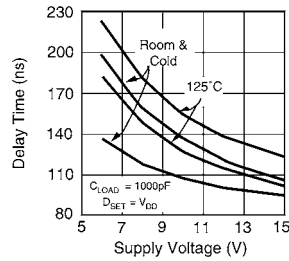**Output Rising Edge Delay vs. R_SET and Supply Voltage (Detail)**

**Output Rising Edge Delay vs. Temperature and R_SET**
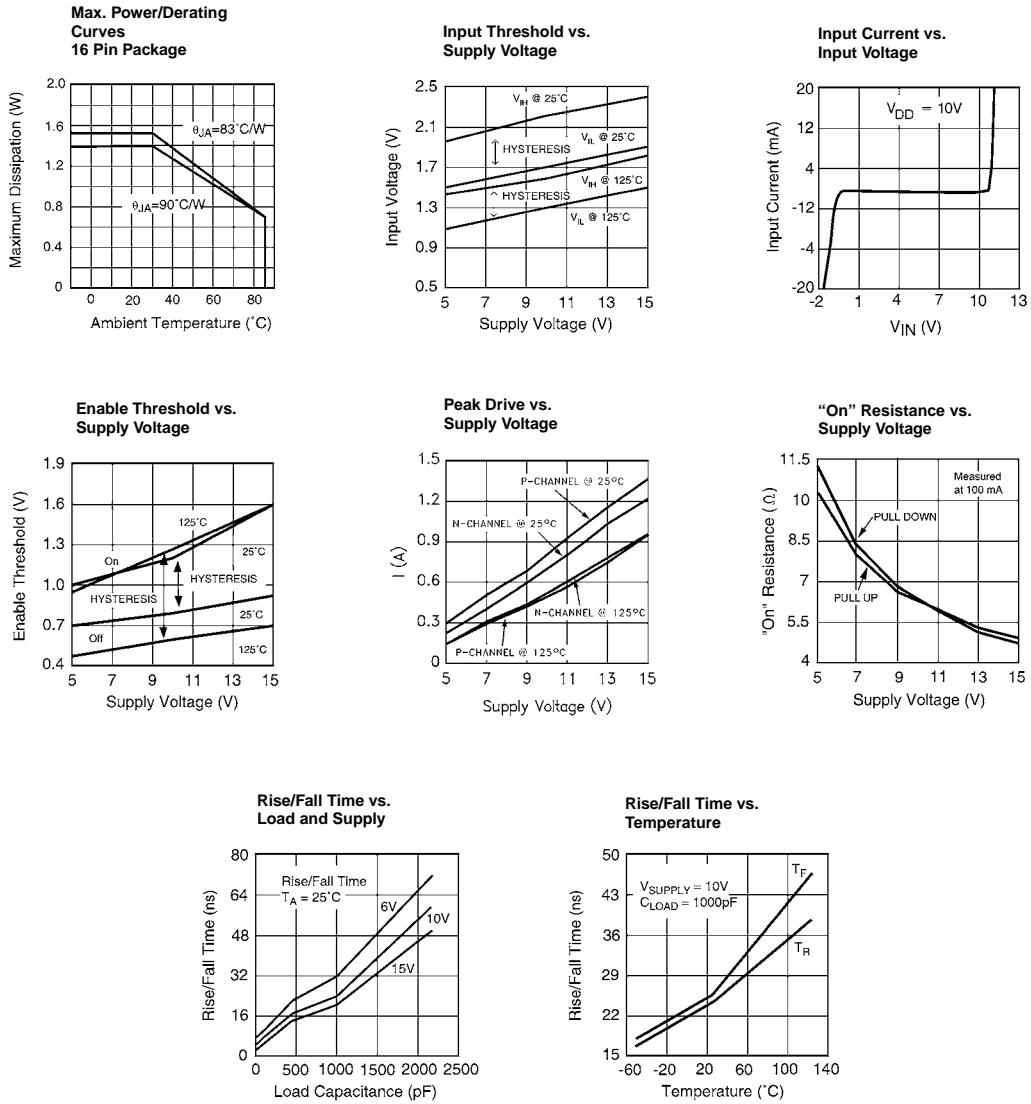
**Output Falling Edge Delay vs. Supply Voltage and Temperature**

**Delay Times* vs. Supply Voltage and Temperature**

**\*Minimum Rising and Falling Edge Delay Time**

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# *Typical Performance Curves*

**Max. Power/Derating
Curves
16 Pin Package**

**Input Threshold vs.
Supply Voltage**

**Input Current vs.
Input Voltage**

**Enable Threshold vs.
Supply Voltage**

**Peak Drive vs.
Supply Voltage**

**"On" Resistance vs.
Supply Voltage**

**Rise/Fall Time vs.
Load and Supply**

**Rise/Fall Time vs.
Temperature**

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