Data Sheet | August 2, 2007 | FN7216.3

Low Power 430MHz HFM Oscillator with Disable

The EL6201 is a solid state high performance laser modulation oscillator with external resistor adjustable frequency and amplitude. The EL6201 is available in both the 8 Ld MSOP and the 5 Ld SOT-23, to enable device placement close to the laser for reduced EMI.

The oscillator frequency is set by connecting a single external resistor from the R_{FREQ} pin to ground. The oscillator current output amplitude is set by connecting a single external resistor from the R_{AMP} pin to ground. The oscillator in the MSOP package also contains a high speed output disable function using the $\overline{OE}$ pin. The $\overline{OE}$ pin can be driven by a high speed timing signal to control precise laser modulation during read/write operations. The output current is disabled when a logical zero 'L' is driven to the CE pin. Supply current is reduced to microamps when CE = LOW.

The EL6201 has internal supply bypass capacitors to reduce oscillation noise spread through supply connections.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL6201CY	G	8 Ld MSOP	MDP0043
EL6201CY-T7*	G	8 Ld MSOP	MDP0043
EL6201CY-T13*	G	8 Ld MSOP	MDP0043
EL6201CYZ (Note)	b	8 Ld MSOP (Pb-free)	MDP0043
EL6201CYZ-T7* (Note)	b	8 Ld MSOP (Pb-free)	MDP0043
EL6201CYZ-T13* (Note)	b	8 Ld MSOP (Pb-free)	MDP0043
EL6201CW-T7*	L	5 Ld SOT-23	MDP0038
EL6201CW-T7A*	L	5 Ld SOT-23	MDP0038
EL6201CWZ-T7* (Note)	BLAA	5 Ld SOT-23 (Pb-free)	MDP0038
EL6201CWZ-T7A* (Note)	BLAA	5 Ld SOT-23 (Pb-free)	MDP0038

*Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

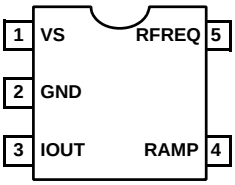
- Small SOT-23 and MSOP8 packages
- Frequency to 430MHz min
- Amplitude to 25mA_{P-P} min
- Output tristate function (MSOP8)
- Power-down function (MSOP8)
- Single +3.5V to +5.0V supply
- Simple to use - only two external resistors required
- Independent resistor setting for frequency and amplitude
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

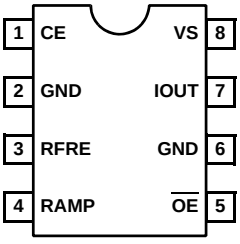
- DVD players
- DVD-ROM drives
- DVD-RAM drives
- CD-RW drives
- MO drives
- Optical pickup head assembly
- Laser diode modulation
- Local oscillator
- Communications lasers

Pinouts

EL6201
(5 LD SOT-23)
TOP VIEW



EL6201
(8 LD MSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Voltages applied to:

V_{CC} . . . . . -0.5V to +6.0V
R_{FREQ}, R_{AMP} . . . . . -0.5V to +6.0V
CE, $\overline{OE}$ . . . . . 0.5 to V_{CC}

Thermal Information

Power Dissipation (maximum) . . . . . See Curves
Operating Ambient Temperature Range . . . . . 0°C to +75°C
Maximum Junction Temperature . . . . . +125°C
Output Current 35mA
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

V_S = +5V, T_A = +25°C, CE = HI, unless otherwise specified. R_{AMP} = 6.67kΩ (I_{OUT} = ±8.5mA), R_{FREQ} = 833Ω (F_O = 330MHz)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
I_S	Supply Current (Enabled)	CE = HIGH, $\overline{OE}$ = LOW		20	27	mA
I_{SD}	Supply Current (Disabled)	CE = LOW			30	µA
I_{STRI}	Supply Current (Tristated)	$\overline{OE}$ = HIGH	6.5	8.5	10.5	mA
V_{LOAD}	Output Voltage Range	Maximum I_{OUTP-P}	1.5		3.5	V
I_{OUTP-P}	Output Current Accuracy	R_{AMP} = 6.67k, I_{OUT} = 2.5V to 3.0V	11	15	19	mA
I_{OS}	Output Current DC offset		-2.5	0	+2.5	mA
V_{INL}	Logic Input Low				0.8	V
V_{INH}	Logic Input High		2.4			V
I_{INL}	Logic Low Input Current	CE or $\overline{OE}$ at 0V			100	µA
I_{INH}	Logic High Input Current	CE or $\overline{OE}$ at +5V			100	µA

AC Electrical Specifications

V_S = +5V, T_A = +25°C, R_{AMP} = 6.67kΩ, R_{FREQ} = 833Ω

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
TC_{OSC}	Oscillator Temperature Coefficient	Measured from +25°C to +125°C die temperature		600		ppm/°C
F_{OSC}	Initial Oscillator Frequency Accuracy		270	330	400	MHz
F_{RANGE}	Oscillator Frequency Range	500Ω ≤ R_{FREQ} ≤ 7kΩ	80		430	MHz
A_{RANGE}	Oscillator Amplitude Range	30kΩ ≤ R_{AMP} ≤ 3kΩ	7.5		25	mA_{P-P}
T_{ON}, CE	EN Delay Time to 50% I_{OUT}	CE = Low to High		300		ns
T_{OFF}, CE	EN Delay Time to 50% I_{OUT}	CE = High to Low		10		ns
T_{ON}, $\overline{OE}$	$\overline{OE}$ Delay Time to 50% I_{OUT}	$\overline{OE}$ = Low to High		10		ns
T_{OFF},$\overline{OE}$	$\overline{OE}$ Delay Time to 50% I_{OUT}	$\overline{OE}$ = High to Low		10		ns
Duty Cycle			40	52	60	%

1. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Typical Performance Curves

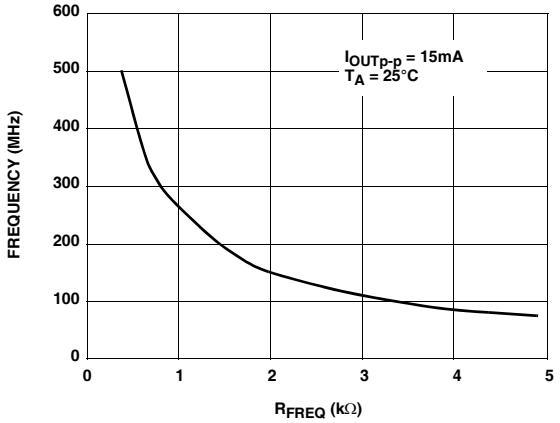


FIGURE 1. FREQUENCY vs R_{FREQ}

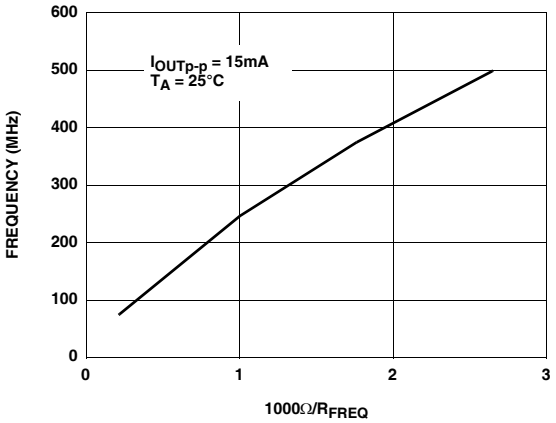


FIGURE 2. FREQUENCY vs 1000Ω/R_{FREQ}

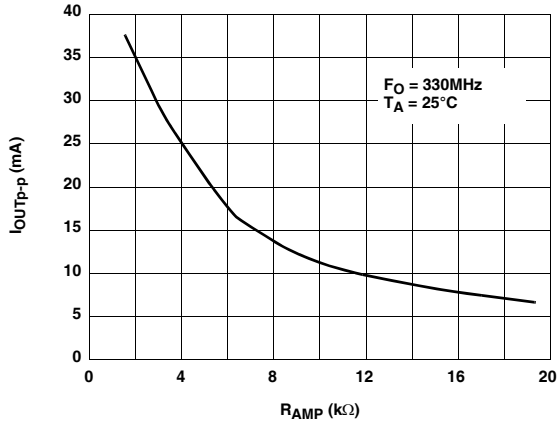


FIGURE 3. I_{OUTp-p} vs R_{AMP}

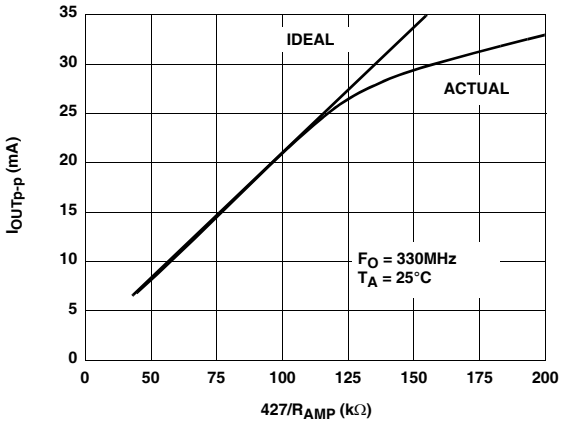


FIGURE 4. I_{OUTp-p} vs 427/R_{AMP}

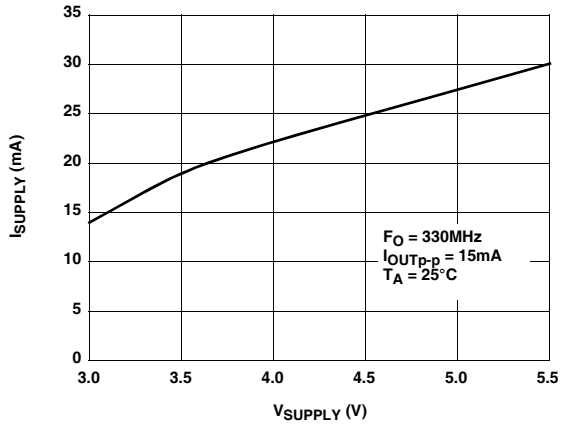


FIGURE 5. I_{SUPPLY} vs V_{SUPPLY}

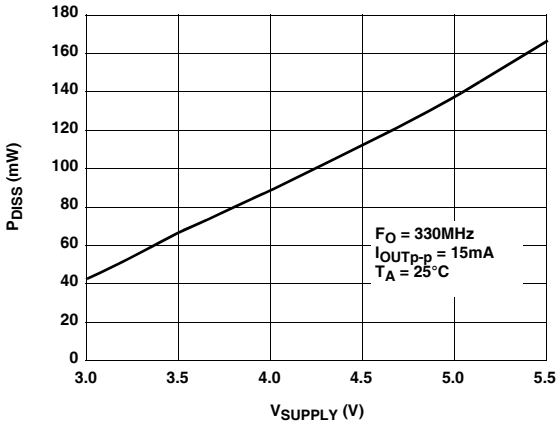


FIGURE 6. DISSIPATION vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

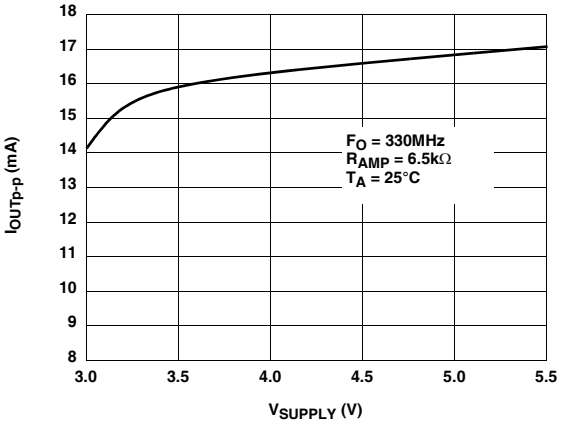


FIGURE 7. I_{OUTP-P} vs V_{SUPPLY}

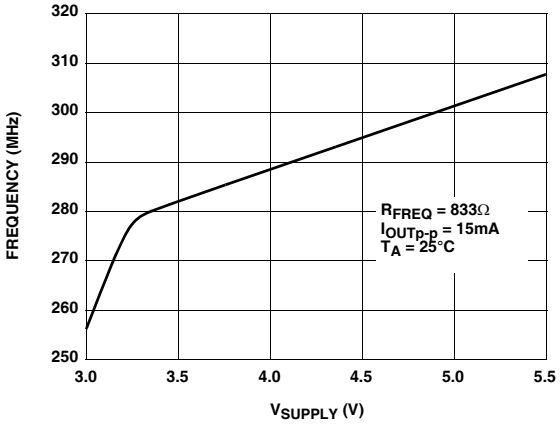


FIGURE 8. FREQUENCY vs V_{SUPPLY}

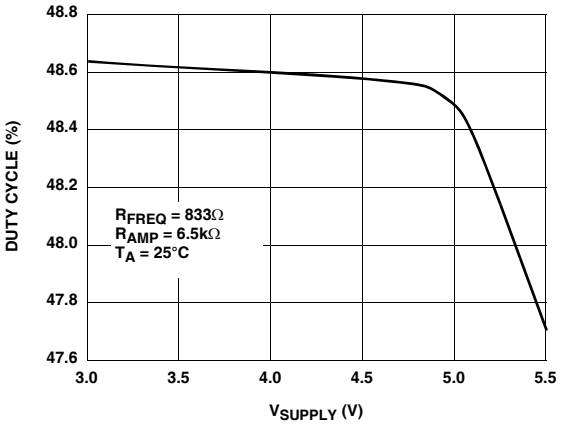


FIGURE 9. DUTY CYCLE (%) vs V_{SUPPLY}

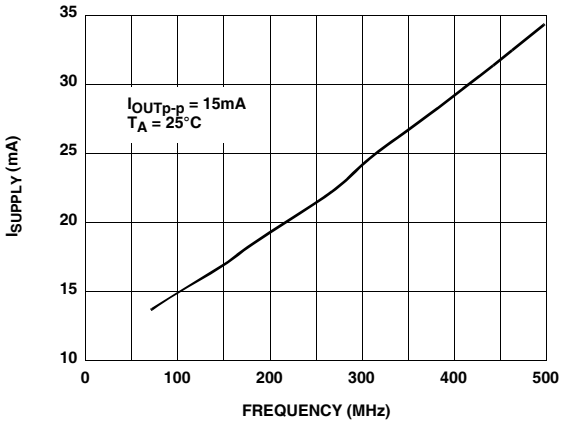


FIGURE 10. I_{SUPPLY} vs FREQUENCY

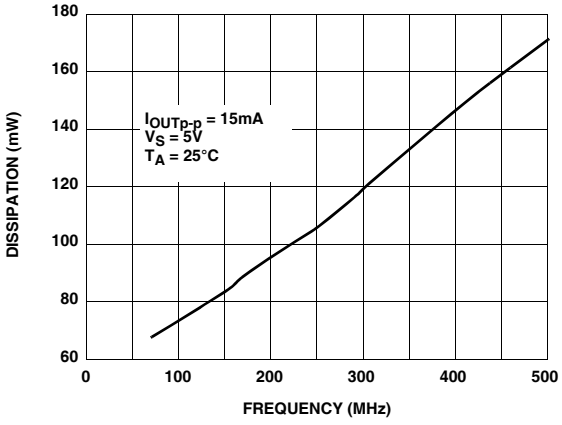


FIGURE 11. DISSIPATION vs FREQUENCY

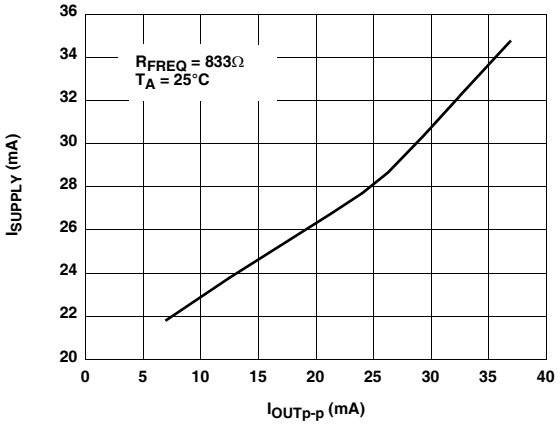


FIGURE 12. I_{SUPPLY} vs I_{OUTp-p}

Typical Performance Curves (Continued)

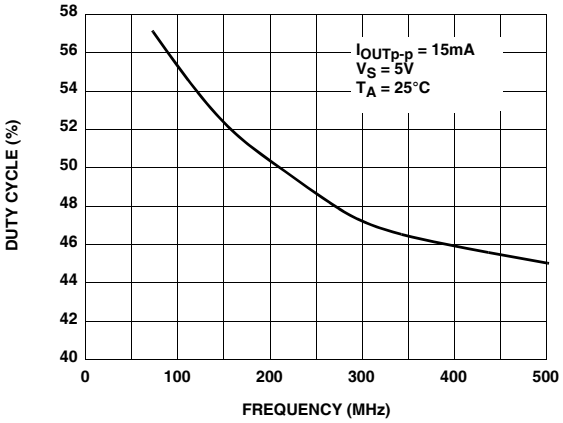


FIGURE 13. DUTY CYCLE vs FREQUENCY

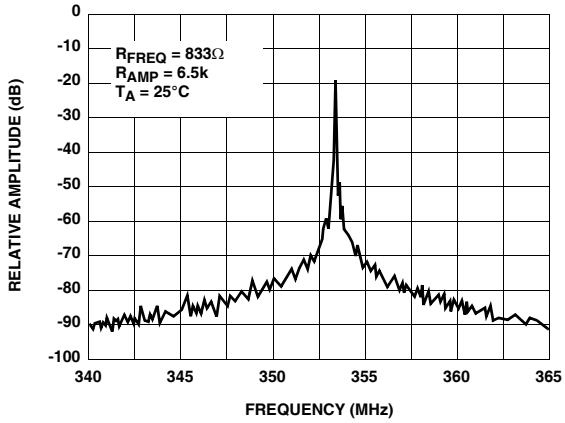


FIGURE 14. OUTPUT SPECTRUM - WIDEBAND

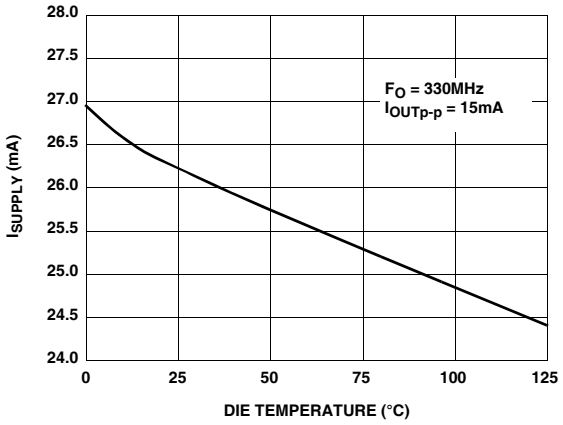


FIGURE 15. I_{SUPPLY} vs DIE TEMPERATURE

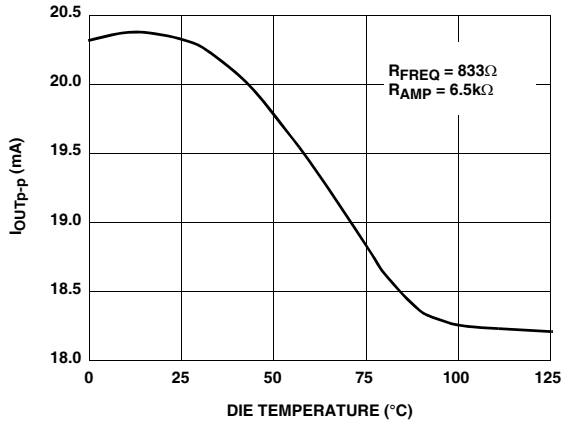


FIGURE 16. I_{OUTp-p} vs DIE TEMPERATURE

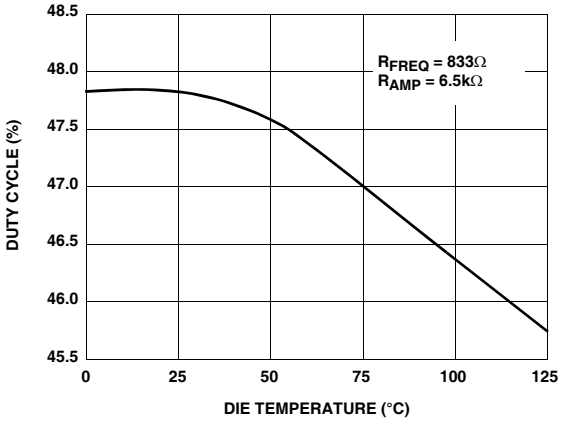


FIGURE 17. DUTY CYCLE vs DIE TEMPERATURE

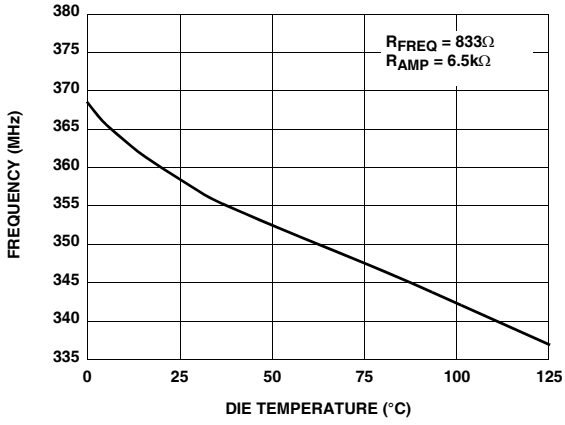


FIGURE 18. FREQUENCY vs DIE TEMPERATURE

Typical Performance Curves (Continued)

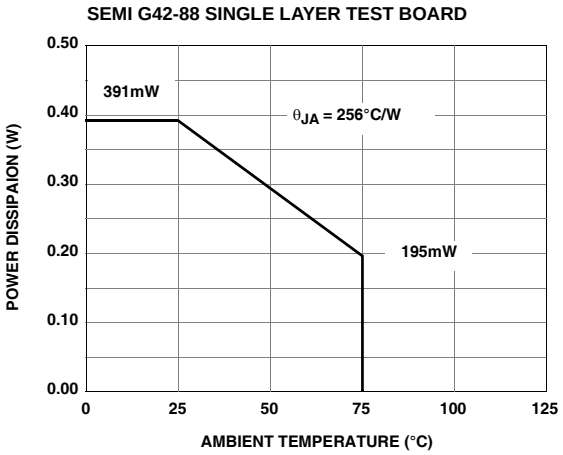


FIGURE 19. SOT23-5 POWER DISSIPATION vs AMBIENT TEMPERATURE

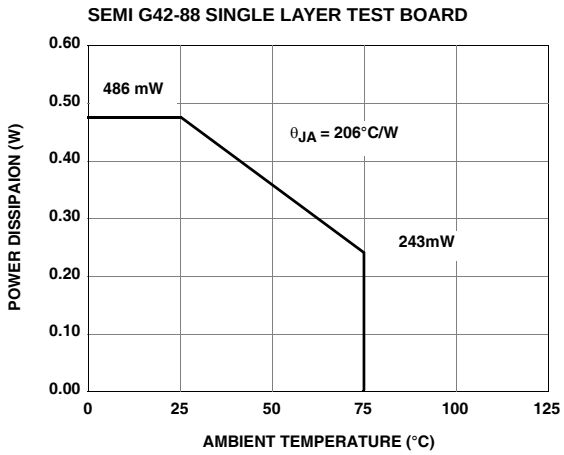
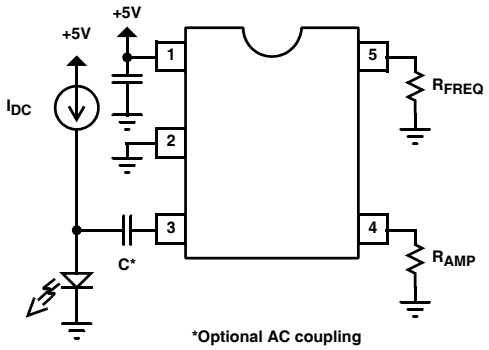


FIGURE 20. MSOP8 POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Application Circuit



Applications Information

The EL6201 is designed to interface easily to laser diodes to break up optical feedback resonant modes and thereby reduce laser noise, but it is also generally useful as a 70MHz to 430MHz oscillator. The first applications section will focus on laser systems, and subsequent sections are of general topics.

Laser Diode Applications

The output of the EL6201 is composed of a sourcing and a sinking current source, switched alternately at the oscillator frequency. The output voltage compliance is V_S to ground, with about 40Ω of series resistance. There is no severe squarewave distortion when the output voltage approaches the supply extremes, although the corners will be rounded. Being a current-source output, the output bias voltage is set by direct connection to the laser diode, which will appear as a low AC impedance with a DC voltage from 1.6V to 2.5V. Thus AC coupling from the EL6201 to the diode is unnecessary. The duty cycle of the output is between 40% and 60%, so the DC contribution from the EL6201 is only ±5% of the peak-to-peak output. This will cause little perturbation of the diode's DC bias current.

Although not necessary, capacitance coupling can be employed. A series capacitive reactance of less than 30Ω is recommended. A 20pF capacitor is thus appropriate at 330MHz. Benefits include no DC error current into the laser diode, and an attenuation of low-frequency noise from the EL6201. Disadvantages include perhaps 20% output AC current loss.

While the diode AC impedance is generally in the low ohm range, any interconnect will create around 8nH per cm. of series inductance. Because the EL6201's output is an AC current source, higher load reactance due to series inductance will cause the EL6201's output voltage to swing more than what a direct connection to the diode would cause. At 400MHz and 15mA_{P-P} output, just one cm. will generate 0.3V_{P-P} of extra driver signal at the fundamental, and more at harmonic frequencies. The output current

waveform is a squarewave, and inductive loads can cause as much as 1V of overshoot. This does not mean that the current delivered to the diode has overshoot - just the voltage seen at the EL6201 output. Measurements show that the EL6201 output edge rate is about 300psec - a speed nearly impossible to deliver over practical interconnects to the diode.

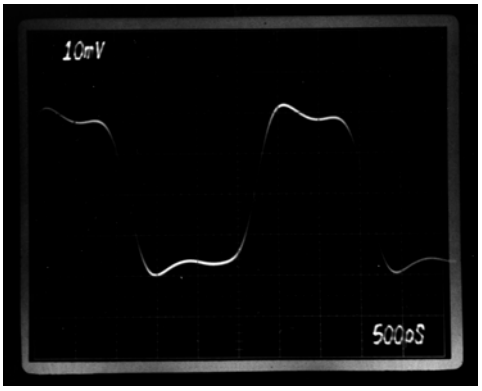


FIGURE 21. OUTPUT CURRENT WAVEFORM - 1GHz BANDWIDTH

General Considerations

EMI and Grounding

From an EMI point of view, the edge rate of the output current is much more important than that of the output voltage. The components are generally small and will be placed over a ground plane, so antenna effects that launch voltage-mode EMI are small. Measurement shows that a practical current edge rate is about 1ns, so interconnect should be over a ground plane and short to minimize inductively launched EMI. Most EMI seems to come from the supply wires connected to the diode/EL6201 board. The internal resistance and inductance of capacitors prevents perfect bypass action, and 150mV$_{P-P}$ noise on the lines is common. There needs to be a lossy series inductance and secondary bypass on the supply side to control signals from propagating down the wires. Alternatively, a series supply resistor can be used, which will also be useful in reducing EL6201 power dissipation. Figure 22 shows the typical connection.

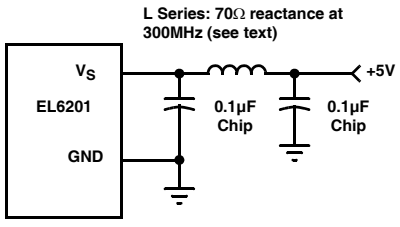


FIGURE 22. RECOMMENDED SUPPLY BYPASSING

The L Series of Figure 22 must be carefully chosen. The goal is to get a series reactance of around 70Ω at 300MHz, so 40nH would suffice. The inductor should be shielded to reduce EMI and have no saturation effects at the supply currents drawn by the EL6201. Finally, there should be no self-resonance at the operating frequency or its harmonics.

Also important is circuit-board layout. At the EL6201's operating frequencies, even the ground plane is not low-impedance, and ground loops should be avoided. Figure 23 shows the output current loops:

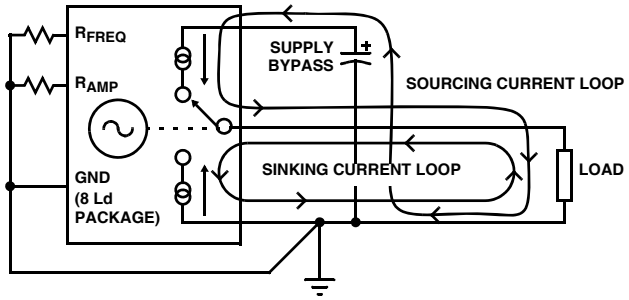


FIGURE 23. OUTPUT CURRENT LOOPS

For the sourcing current loop, the current flows through the supply bypass capacitor. The ground end of the bypass thus should be connected directly to the EL6201 ground pin (output ground pin of the 8 Ld package). A long ground return path will cause the bypass capacitor currents to generate voltage drops in the ground plane of the circuit board, and other components (such as R_{AMP} and R_{FREQ}) will pick this up as an interfering signal. Similarly, the ground return of the load should be considered as noisy and other grounded components should not connect to this path. Slotting the ground plane around the load's return will eliminate adjacent grounded components from seeing the noise.

R_{FREQ} and R_{AMP} Interfaces

R_{AMP} and R_{FREQ} should be connected to the non-load side of the power ground to avoid noise pick-up.

Figure 24 shows an equivalent circuit of these pins. V_{REF} is roughly 0.35V for R_{FREQ} and more accurately 1.17V for R_{AMP}. The R_{AMP} and R_{FREQ} resistor should return to the EL6201's ground very directly lest they pick up high-frequency noise interference. They also should have minimal capacitance to ground. Trimmer resistors can be

used to adjust initial operating points, but they should be replaced with fixed resistors for further testing.

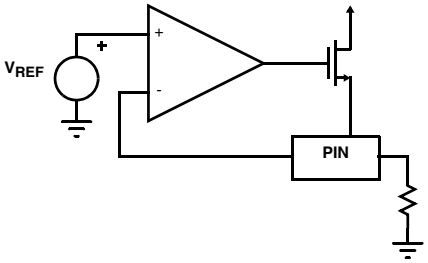


FIGURE 24. R_{FREQ} AND R_{AMP} PIN INTERFACE

External voltage sources can be coupled to the R_{AMP} and R_{FREQ} pins to effect frequency or amplitude modulation or adjustment. It is recommended that a coupling resistor be installed in series with the control voltage and mounted directly next to the EL6201 pin. This will keep the inevitable high-frequency noise of the EL6201's local environment from propagating to the modulation source, and it will keep parasitic capacitance at the EL6201 pin minimized.

Both inputs have several megahertz of bandwidth for analog modulation. The output enable pin can be used to pass digital modulation up to about 20Mbit/sec rates.

Power Dissipation Considerations

Supply current can be predicted by Equation1:

$$I_S = \frac{12mA + I_{OUTp\text{-}p}}{4 + (V_S - 1.6V) \times FREQ \times 8 \times 10^{-12}} \quad \text{(EQ. 1)}$$

The 12mA quantity represents the operating DC current of the EL6201. This is also the current drawn from the supply during output disable. The I_{OUT} quantity is based on a typical 50% duty cycle of output pull-up current, and the fact that the peak-to-peak output current is about twice the pull-up or pull-down currents. The V_S quantity is due to CV^2F losses within the circuit, and the $8*10^{-12}$ quantity represents internal capacitances that must be slewed at the operating frequency. The 1.6V offset is a curve fit to measured data.

The internal die temperature operating range is -40°C to +125°C. Internal temperature is equal to the ambient temperature plus power dissipated times the thermal resistance of the mounted package, θ_{JA}. For a mounted MSOP-8 package, θ_{JA} is 206°C/W. The SOT-23 package has a θ_{JA} of 256°C/W.

Power-Down with the SOT-23 Package

The supply current of the EL6201 is low enough so that a logic output can simply provide the supply current of the part and effect power-down. This is most useful using the EL6201 in the SOT-23 package, which has no enable pin.

RF Applications

The EL6201 can easily interface to reactive loads, and is adequate as a short-range modulated transmitter. Remembering that the output circuitry looks like current sources, impedance matching becomes a matter of transforming the load impedance to an appropriate load line for the EL6201. Also important is maintaining correct DC bias voltage on the output. Since the output will have a net DC current, capacitor coupling would allow the DC level to drift toward a supply rail and increase output harmonic products. In cases where such harmonics are important, Figure 25 shows coupling the EL6201 output to a 50Ω load:

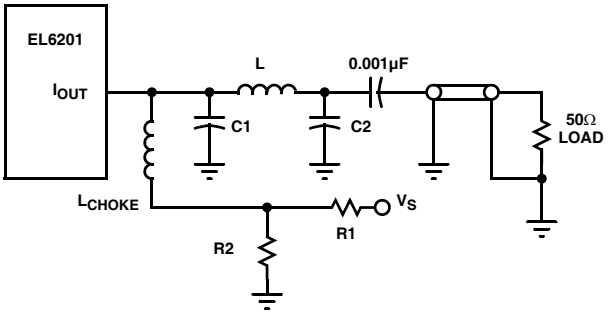


FIGURE 25. TUNED INTERFACE TO 50Ω LEAD

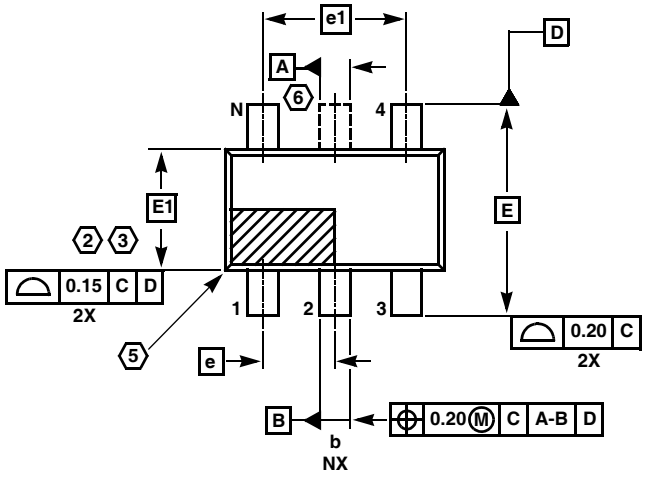
Digital Clock Applications

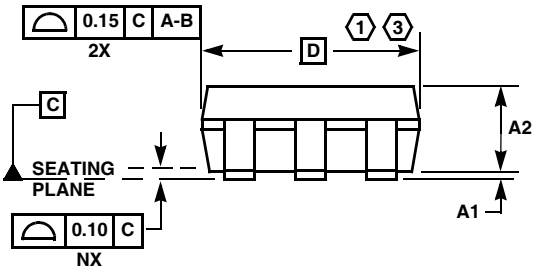
The EL6201 can be used as a digital clock source. If unloaded, the output will simply traverse ground to V_S. It is recommended that the V_S supply be isolated from the main digital supply with an inductor or resistor, whose value is chosen to drop about 250mV. In this way logic noise can be isolated by the series component and the EL6201 local bypass.

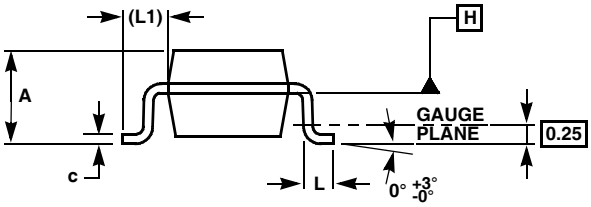
The rise- and fall-time of the output will be equal to $V_S/(C_{LOAD}*I_{OUTP\text{-}P}/2)$. The output current should be the smallest that can set an output rise-time, in the interest of lowest dissipation.

The jitter is about 0.7% of period, RMS.

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

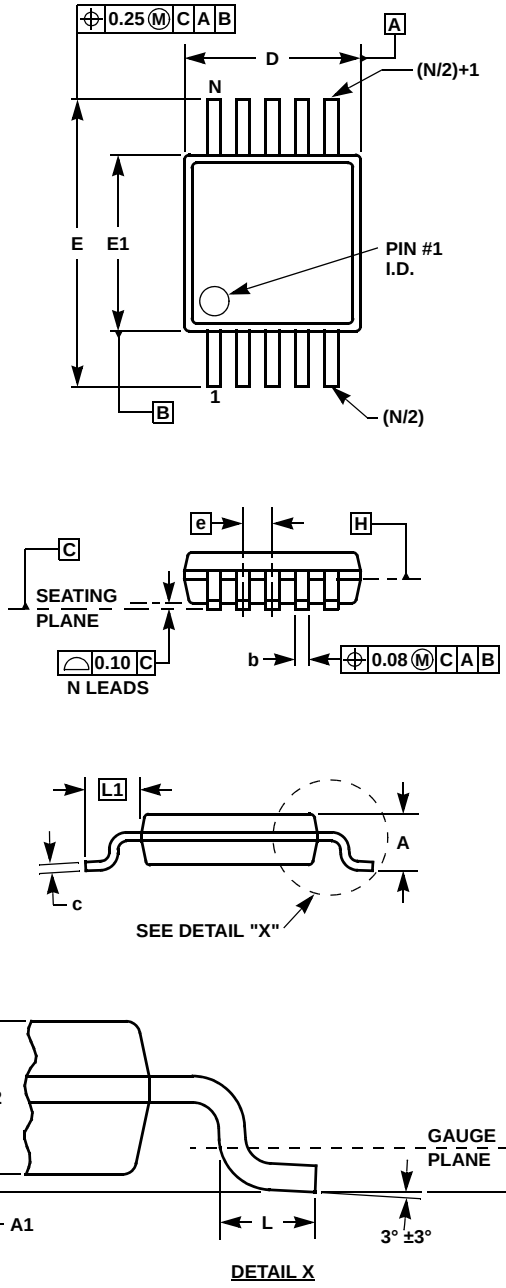
SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.