Figure 1. DPA-Switch Flyback DC-DC Converter Schematic.

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Design Idea DI-29 **DPA-Switch®**

DPA425R

High efficiency – 85% using Schottky rectifiers

No current sense resistor or transformer required Accurate input under/over voltage meets ETSI standards

Operates to zero load with no pre-load required

400 kHz operation minimizes size of magnetics

Output overload, open loop and thermally protected

DPA-Switch greatly simplifies the design compared to a discrete

implementation. Resistor R1 programs the input under/over

voltages to 33 V and 86 V, respectively. Including tolerances

these thresholds guarantee the converter is operational between

36 V and 75 V, without the cost of additional line sense

DC-DC Converter

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Operation

components.

Design Highlights

· Extremely low component count

Resistor R3 programs the internal current limit of the DPA425R to 50% of nominal. The larger *DPA-Switch* selection reduces conduction losses, raising efficiency without circuit changes or increased overload power.

7 V

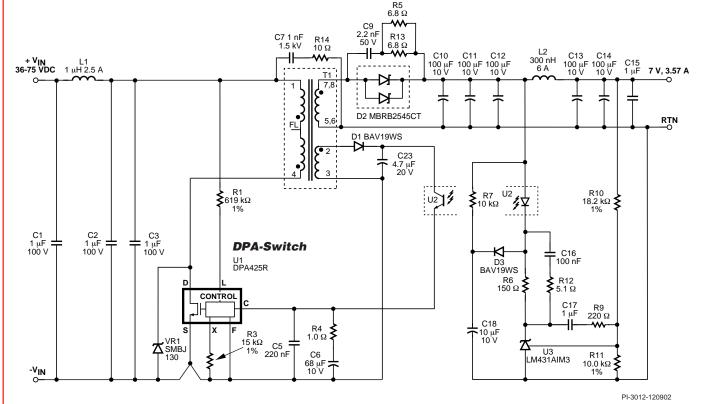
36 - 75 VDC

Zener VR1 clamps leakage inductance spikes, keeping the DRAIN voltage below BV_{DSS} . The bias supply for U1 is provided from an auxiliary flyback transformer winding.

On the secondary, a snubber across D2 (C9, R5 and R13) limits the secondary leakage inductance spikes generated by diode reverse recovery. Inductor L2, C13 and C14 form a post-filter to reduce high frequency output switching ripple. A soft-finish network, C18, D3 and R7, eliminates output turn-on overshoot. The remaining components provide output voltage regulation and loop compensation.



25 W





Topology

Flvback

Key Design Points

- For nominal under-voltage set point V_{UV}: R1 = (V_{UV}-2.35 V)/50 μ A. V_{OV} = (R1×135 μ A)+2.5 V.
- Zener VR1 voltage is 130 V to safely limit the DRAIN voltage below V_{DSS} of 200 V.
- Opto U2 should have a CTR of between 100% and 200% for optimum loop stability.
- Set resonance of L2 and C13 + C14 to beyond loop crossover frequency (typically 5% to 10% of switching frequency).
- Good layout practices should be followed:
 - Locate C5, C6 and R4 close to U1, with grounds returned to the SOURCE pin.
 - Primary return should be connected to the *DPA-Switch* tab, not the SOURCE pin.
 - Minimize the primary and secondary loop areas to reduce parasitic leakage inductance.

Transformer Parameters PR1408 Core Material Siemens N87 Gap for 340 nH/T² Bobbin P1408 8 pin (B&B B-096 or equivalent)

Primary: 6T + 6T, 2 x 27 AWG

Secondary: 3T, 4 x 25 AWG

Bias: 6T, 32 AWG

Primary (4-FL), tape, Bias (2-3), tape,

Secondary (5,6-7,8), tape,

Primary (FL-1), tape

Primary: 49 µH ±10%, Leakage: 1 µH (max)

3.8 MHz (minimum)

Table 1.	Transformer Construction Information.

Winding Details

Winding Order

(pin numbers)

Inductance

Primary Resonant

Frequency

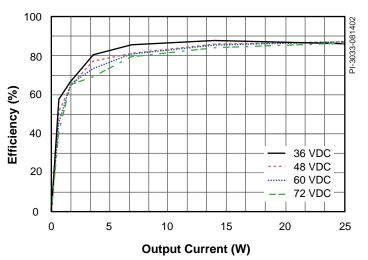


Figure 2. Efficiency vs. Output Power.

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WORLD HEADQUARTERS	EUROPE & AFRICA	SINGAPORE	TAIWAN
AMERICAS	Power Integrations (Europe) Ltd.	Power Integrations, Singapore	Power Integrations
Power Integrations, Inc.	United Kingdom	Republic of Singapore 308900	International Holdings, Inc.
San Jose, CA 95138 USA	Phone: +44-1344-462-300	Phone: +65-6358-2160	Taipei, Taiwan
Customer Service:	Fax: +44-1344-311-732	Fax: +65-6358-2015	Phone: +886-2-2727-1221
Phone: +1 408-414-9665	e-mail: eurosales@powerint.com	e-mail: singaporesales@powerint.com	Fax: +886-2-2727-1223
Fax: +1 408-414-9765	KOREA	JAPAN	e-mail: taiwansales@powerint.com
e-mail: usasales@powerint.com	Power Integrations	Power Integrations, K.K.	INDIA (Technical Support)
CHINA	International Holdings, Inc.	Keihin-Tatemono 1st Bldg.	Innovatech
Power Integrations International	Seoul, Korea	Japan	Bangalore, India
Holdings, Inc.	Phone: +82-2-782-2840	Phone: +81-45-471-1021	Phone: +91-80-226-6023
China	Fax: +82-2-782-4427	Fax: +81-45-471-3717	Fax: +91-80-228-9727
Phone: +86-755-8367-5143	e-mail: koreasales@powerint.com	e-mail: japansales@powerint.com	e-mail: indiasales@powerint.com
Fax: +86-755-8377-9610			
e-mail: chinasales@powerint.com		APPLICATIONS HOTLINE	APPLICATIONS FAX

World Wide +1-408-414-9760

World Wide +1-408-414-9660

