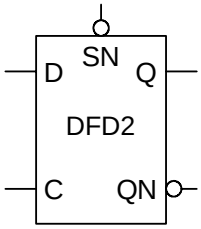
DFD2 is a fast, static, master-slave D flip-flop with 2x drive strength. SET is asynchronous and active low.

Truth Table

SN	D	C	Q	QN
H	H	↑	H	L
H	L	↑	L	H
H	X	↓	no change	
L	X	X	H	L



Capacitance

	Ci (pF)
D	0.025
C	0.020
SN	0.033

Area

1.76 mils^2

Power

6.60 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Delay C to Q	tpdcqr	0.81	1.78	2.26	0.98	1.95	2.41
	tpdcqf	0.73	1.64	2.08	0.88	1.80	2.23
Delay C to QN	tpdcqnr	0.98	1.94	2.43	1.13	2.08	2.58
	tpdcqnf	1.07	1.95	2.40	1.25	2.13	2.57
Delay SN to Q	tpdsnq	0.81	1.77	2.25	1.14	2.09	2.58
Delay SN to QN	tpdsnqn	1.06	1.94	2.37	1.40	2.27	2.69
Output Slope C to Q	op_slcqr	0.66	3.42	5.01	0.65	3.53	5.01
	op_slcqf	0.57	3.00	4.02	0.57	2.85	4.18
Output Slope C to QN	op_slcqnr	0.67	3.58	5.00	0.68	3.50	5.06
	op_slcqnf	0.53	2.86	4.05	0.55	2.90	4.05
Output Slope SN to Q	op_slsnq	0.67	3.43	4.97	0.67	3.53	4.90
Output Slope SN to QN	op_slsnqn	0.56	2.87	4.15	0.56	2.82	4.11

Characteristics		Symbol	[ns]	Characteristics		Symbol	[ns]
Min D Setup Time to C	High	tsudch	0.15	Min D Hold Time to C	High	thdch	0.00
	Low	tsudcl	0.13		Low	thdcl	0.00
Min SN Setup Time to C	Low	tsusnc	0.00	Min SN Hold Time to C	Low	thsnc	0.45
Min C Width	High	twch	0.38				
	Low	twcl	0.82				
Min SN Width	Low	twsn	1.05				