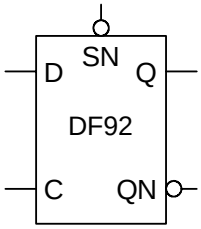
DF92 is a static, master-slave D flip-flop with 2x drive strength. SET is asynchronous and active low.

Truth Table

SN	D	C	Q	QN
H	H	↑	H	L
H	L	↑	L	H
H	X	↓	no change	
L	X	X	H	L



Capacitance

	Ci (pF)
D	0.018
C	0.020
SN	0.025

Area

1.63 mils^2

Power

5.74 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(L) with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.2	L = 1.4	L = 2.0	L = 0.2	L = 1.4	L = 2.0
Delay C to Q	tpdcqr	2.13	3.47	4.11	2.33	3.69	4.32
	tpdcqf	2.26	3.35	3.90	2.47	3.57	4.12
Delay C to QN	tpdcqnr	1.71	3.13	3.81	1.92	3.34	4.02
	tpdcqnf	1.55	2.85	3.42	1.76	3.07	3.62
Delay SN to Q	tpdsnq	2.54	3.85	4.50	2.79	4.12	4.77
Delay SN to QN	tpdsnqn	1.99	3.29	3.84	2.24	3.53	4.10
Output Slope C to Q	op_slcqr	0.97	4.95	7.06	0.95	4.97	7.06
	op_slcqf	0.77	3.62	5.21	0.78	3.63	5.11
Output Slope C to QN	op_slcqnr	1.08	5.03	7.17	1.06	5.01	7.16
	op_slcqnf	1.00	3.93	5.17	0.97	3.91	5.08
Output Slope SN to Q	op_slsnq	1.02	5.06	7.07	1.02	5.06	7.10
Output Slope SN to QN	op_slsnqn	1.05	3.87	5.17	1.02	4.00	5.25

Characteristics		Symbol	[ns]	Characteristics		Symbol	[ns]
Min D Setup Time to C	High	tsudch	0.40	Min D Hold Time to C	High	thdch	0.00
	Low	tsudcl	0.26		Low	thdcl	0.00
Min SN Setup Time to C	Low	tsusnc	0.00	Min SN Hold Time to C	Low	thsnc	0.79
Min C Width	High	twch	1.15				
	Low	twcl	0.91				
Min SN Width	Low	twsn	1.43				