Title	***21 W Standby Power Supply using TNY280P***
Specification	Input: 85 – 295 VAC (110 – 420 VDC) Outputs: 5 V / 4 A; 15 V / 67 mA
Application	General PC-Standby Supply
Author	Power Integrations Applications Department
Document Number	DER-114
Date	June 28, 2006
Revision	1.0

Summary and Features

- High standby efficiency: P_{IN} < 0.70 W @ P_{OUT} = 0.5 W, at 230 VAC input
- Under-voltage lockout (UVLO) function: glitch-free startup and shutdown
- Two means of implementing output overvoltage protection (OVP)
- EEL22 transformer core meets clearance and creepage requirements
- Output overload, short circuit and open feedback loop protection

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a universal input 5 V, 4 A power supply designed around a TNY280P device from the *TinySwitch-III* family of ICs. Although designed as an auxiliary or bias supply for a personal computer (PC) power supply, this design can also be used as a general-purpose evaluation platform for *TinySwitch-III* devices.

Typically, PC power supplies have a power factor corrected (PFC) input stage. However, since the bias supply must operate before the PFC stage is active, this supply has been designed for universal input operation.

Input rectification and input storage capacitance have been included, for evaluation purposes. This stage and the EMI filter components would normally be part of the main PC supply, in an actual application.

This report contains the power supply specification, the circuit diagram, a complete bill of materials (BOM), the *PI Xls* transformer spreadsheet design results, complete transformer documentation, the printed circuit board (PCB) layout and relevant performance data.

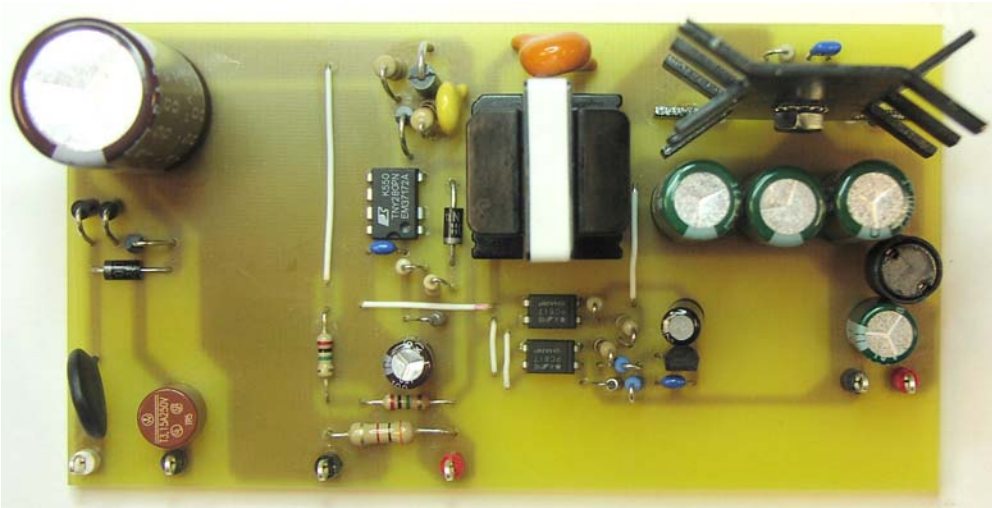

Figure 1– Populated Circuit Board Photograph.

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2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		295	VAC	Equivalent to 100 – 420 VDC
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.3	W	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz bandwidth
Output Current 1	I_{OUT1}			4	A	
Output Voltage 2	V_{OUT2}	12	15	18	V	100 mA minimum load on V_{OUT1}
Output Current 2				67	mA	& 40 mA load on auxiliary output
Total Output Power						
Continuous Output Power	P_{OUT}			21	W	
Efficiency						
Full Load	η		76		%	Measured at P_{OUT} 25 °C
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

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3 Schematic

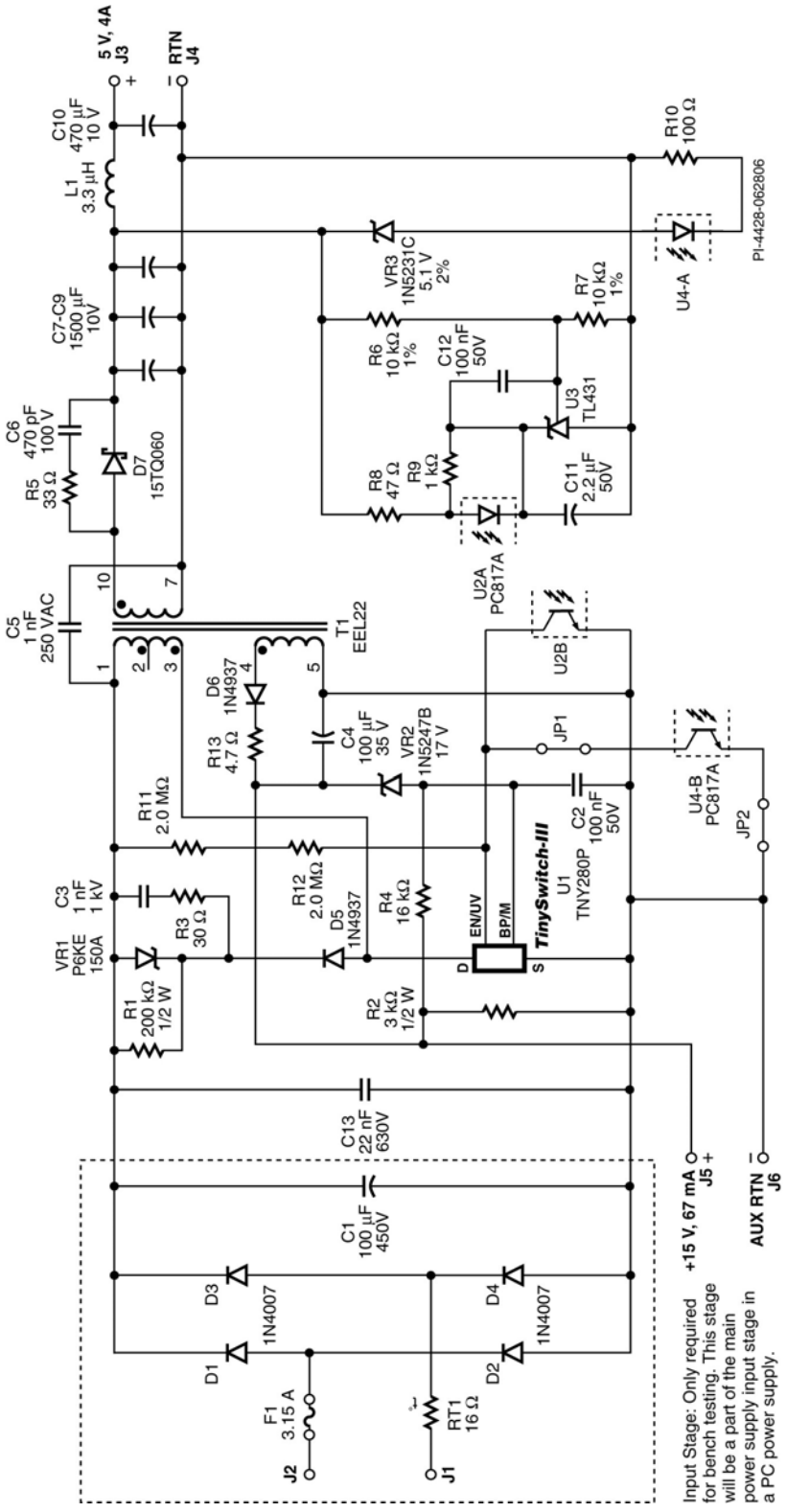

Figure 2 – Circuit Diagram.

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4 Circuit Description

This dual output converter is configured as a Flyback. The main output provides 4 A at 5 V, while the bias winding on transformer T1 is used to generate a 15 V output that can supply up to 67 mA. The converter will operate over an input voltage range of 85 – 295 VAC or 100 – 420 VDC. The 5 V output is referenced to a TL431 located on the secondary side, and feedback is passed back to the primary through optocoupler (U2).

4.1 Input Rectifier & filter

This circuit is designed for standby applications and components F1, RT1, D1-D4 & C1 are only provided for standalone testing. Fuse F1 will effectively isolate the converter from the supply source in the event of short circuit failure. Thermistor RT1 limits the inrush current at startup. Diodes D1, D2, D3 & D4 form a bridge rectifier, which charges the bulk storage capacitor C1.

4.2 TNY280 Primary

The TNY280P device (U1) is an integrated circuit, which includes a power MOSFET, an oscillator, control, start-up and protection functions.

A clamp circuit (D5, VR1, C3, R1 & R3) limits the voltage that appears on the drain of U1 each time its MOSFET turns off. During normal operation VR1 does not conduct and clamping is performed by D5, C3, R1 & R3. Typically, VR1 will only conduct during fault conditions such as overload. This approach allows the RCD clamp (R1, R3, C3 & D5) to be sized for normal operation, which maximizes efficiency at light load.

The output of the bias/auxiliary supply winding is rectified by diode D6 and filtered by capacitor C4. The rectified and filtered output of the bias winding (terminals J5 & J6) can be used to power external circuitry on the primary side, such as the PFC and main converter control circuits. The bias winding is also used to supply current to the TNY280 BYPASS/MULTIFUNCTION (BP/M) pin during steady state operation. The value of R4 is selected to deliver the IC supply current to the BP/M pin, thereby inhibiting the internal high-voltage current source that normally charges the BP/M pin capacitor (C2). This results in reduced input power consumption under light load and no load conditions.

Capacitor C2 provides high frequency decoupling of the internally generated 5.85 V IC supply voltage. Three different capacitor values could be used for C2, which would select one of three internal current limit sets. A 0.1 uF capacitor was used in this design, which selects the standard current limit set for a TNY280P.

The transistor of optocoupler U2 pulls current out of the ENABLE/UNDER-VOLTAGE (EN/UV) pin of U1. The IC keeps switching as long as the current drawn from its EN/UV pin is less than 90 µA. It stops switching whenever the current drawn from the EN/UV pin exceeds that threshold, which ranges from 90 µA to 150 µA (with the typical value being 115 µA). By enabling and disabling switching pulses, the feedback loop regulates the output voltage of the power supply.

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An internal state machine sets the MOSFET current limit to one of four levels, depending on the main output load current. This ensures that the effective switching frequency remains above the audible frequency range. The lowest current limit (used at no-load) makes the transformer flux density so low that dip-varnished transformers produce no perceptible audible noise.

4.3 Output Rectification

Diode D7 rectifies the main output. Low ESR capacitors C7, C8 & C9 attenuate the switching ripple. A post filter (L1 & C10) further reduces switching ripple and noise on the main output.

4.4 Output Feedback

Resistors R6 and R7 form a voltage divider network. A portion of the output voltage is fed into the input terminal of the TL431 (U3). The TL431 varies its cathode voltage in an attempt to keep its input voltage constant (equal to 2.5 V, ±2%). As the cathode voltage changes, the current through the LED and transistor within U2 change. Whenever the EN/UV pin current exceeds its threshold, the next switching cycle is disabled. Whenever the EN/UV pin current falls below the threshold, the next switching cycle is enabled. As the load is reduced, the number of enabled switching cycles decreases, which lowers the effective switching frequency and the switching losses. This results in almost constant efficiency down to very light loads, which is ideal for meeting energy efficiency requirements. Capacitor C12 rolls off the gain of U3 with frequency, to ensure stable operation. Capacitor C11 prevents the output voltage from overshooting at startup.

4.5 UV Lockout

Optional resistors R11 and R12–connected between the DC bus and the EN/UV pin of U1–enable the under-voltage lockout function. When these resistors are used, start-up is inhibited until the current into the EN/UV pin exceeds 25 µA. The values of R11 and R12 sets a startup voltage threshold that prevents output voltage glitches when the input voltage is abnormally low, such as when the AC input capacitor is discharging during shutdown. Additionally, the UVLO status is checked whenever a loss of regulation occurs–such as during an output overload or short-circuit. This effectively latches U1 off until the input voltage is removed and reapplied. With the values of R11 and R12 shown in figure 2, the UVLO threshold is approximately 100 VDC (71 VAC).

4.6 OVP

This supply has two different overvoltage protection circuits. The first OVP function is provided by VR2 and the latching shutdown function built into U1. If the feedback loop became an open circuit–due to the failure of U2, for example–the main output voltage and the bias winding voltage would both rise. Once the bias voltage exceeded the sum of the voltage across VR2 and the BP/M pin voltage, current would flow into the BP/M pin. When that current exceeds the OV shutdown threshold (≈5.5 mA), the latching shutdown function is triggered and MOSFET switching is disabled. MOSFET switching remains disabled until the BP/M pin capacitor (C2) is discharged below 4.8 V.

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The second OVP function is provided by VR3, U4 and R10, and is enabled when jumpers JP1 and JP2 are installed (forms a second feedback loop). If the primary feedback loop became an open circuit, the output voltage would rise. The EN/UV pin would be pulled low once the output voltage exceeded the voltage across VR3 and the LED within U4. The output voltage would then be regulated at a slightly higher voltage than that of the primary feedback loop.

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5 PCB Layout

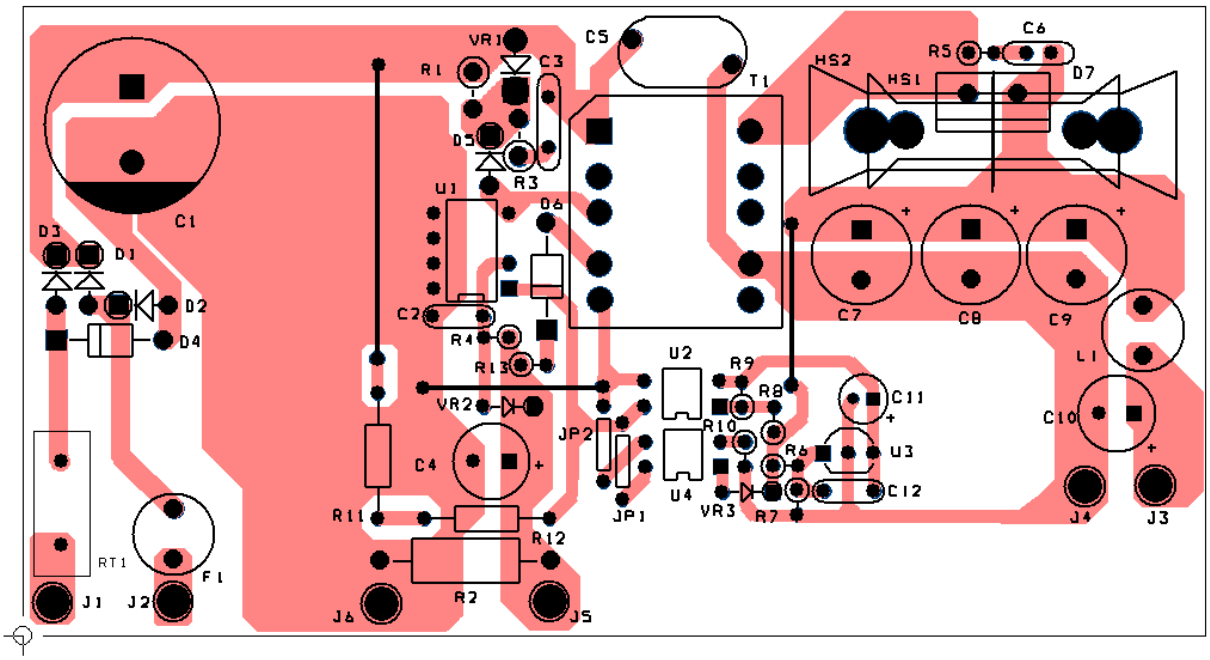

Figure 3 – Printed Circuit Layout.

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6 Bill Of Materials

Item	Qty	Part Ref	Value	Description	Mfg Part Number	Mfg
1	1	C1	100 µF	100 µF, 450 V, Electrolytic, Low ESR, (18 x 30)	EPAG451ELL101MM35S	Nippon Chemi-Con
2	2	C2 C12	100 nF	100 nF, 50 V, Ceramic, X7R	B37987F5104K000 / ECU-S1H104KBB	Epcos/Panasonic
3	1	C3	1 nF	1 nF, 1 kV, Disc Ceramic	ECK-D3A102KBP	Panasonic
4	1	C4	100 µF	100 µF, 35 V, Electrolytic, Gen. Purpose, (8 x 11.5)	KME35VB101M6X11LL	Nippon Chemi-Con
5	1	C5	1 nF	1 nF, Ceramic, Y1	440LD10	Vishay
6	1	C6	470 pF	470 pF, 100 V, Ceramic, X7R	ECU-S2A471KBA	Panasonic
7	3	C7 C8 C9	1500 µF	1500 µF, 10 V, Electrolytic, Very Low ESR, 22 mΩ, (10 x 25)	EKZE100ELL152MJ25S	Nippon Chemi-Con
8	1	C10	470 µF	470 µF, 10 V, Electrolytic, Low ESR, 120 mΩ, (8 x 12)	ELXZ100ELL471MH12D	Nippon Chemi-Con
9	1	C11	2.2 µF	2.2 µF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKME500ELL2R2ME11D	Nippon Chemi-Con
10	1	C13	22 nF	22 nF, 630 V, Film	ECQ-E6223KF	Panasonic
11	4	D1 D2 D3 D4	1N4007	1000 V, 1 A, Rectifier, DO-41	1N4007	Vishay
12	2	D5 D6	1N4937	600 V, 1 A, Fast Recovery Diode, 200 ns, DO-41	1N4937	Vishay
13	1	D7	15TQ060	60 V, 15 A, Schottky, TO-220AC	15TQ060	International Rectifier
14	1	F1	3.15 A	3.15 A, 250 V, Fast, TR5	370 1315 041	Wickmann
15	1	HS1	6032B-TT	HEATSINK, Straight Fin, 8.3 °C/W, TO-220	6032B-TT	AAVID/Thermalloy
16	2	J1 J4	CON1	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
17	3	J2 J5 J6	CON1	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
18	1	J3	CON1	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone
19	2	JP1 JP2	J	Wire Jumper, Non insulated, 22 AWG, 0.2 in	298	Alpha
20	1	L1	3.3 µH	3.3 µH, 5.5 A, 8.5 x 11 mm	R622LY-3R3M	Toko
21	1	R1	200 kΩ	200 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-200K	Yageo
22	1	R2	3 kΩ	3 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-3K0	Yageo
23	1	R3	30 Ω	30 Ω, 5%, 1/2 W, Carbon Film	CFR-50JB-30R	Yageo
24	1	R4	16 kΩ	16 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-16K	Yageo
25	1	R5	33 Ω	33 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-33R	Yageo
26	2	R6 R7	10 kΩ	10 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
27	1	R8	47 Ω	47 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-47R	Yageo
28	1	R9	1 kΩ	1 kΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-1K0	Yageo
29	1	R10	100 Ω	100 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-100R	Yageo
30	2	R11 R12	2.0 MΩ	2.0 MΩ, 5%, 1/4 W, Carbon Film	CFR-25JB-2M0	Yageo
31	1	R13	4.7 Ω	4.7 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-4R7	Yageo
32	1	RT1	16 Ω	NTC Thermistor, 16 Ω, 2.7 A	CL170	Thermometrics
33	1	T1	EEL22	Bobbin, EEL22, Vertical, 10 pins	YC-2207	Ying Chin
34	1	U1	TNY280P	TinySwitch-III, TNY280P, DIP-8C	TNY280P	Power Integrations
35	2	U2 U4	PC817A	Opto coupler, 35 V, CTR 80-160%, 4-DIP	PC817X1	Sharp
36	1	U3	TL431	2.495 V Shunt Regulator IC, 2%, 0 to 70C, TO-92	TL431CLP	Texas Instruments
37	1	VR1	P6KE150A	150 V, 5 W, 5%, TVS, DO204AC (DO-15)	P6KE150A	Vishay
38	1	VR2	1N5247B	17 V, 5%, 500 mW, DO-35	1N5247B	Microsemi
39	1	VR3	1N5231C	5.1 V, 2%, 500 mW, DO-35	1N5231C	Microsemi

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7 Transformer Specification

7.1 Electrical Diagram

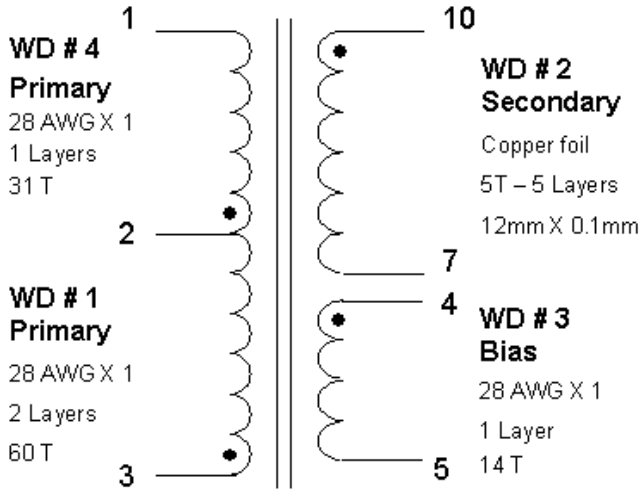

Figure 4 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from Pins 1-5 to Pins 7-10	3000 VAC
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 0.4 VRMS	1084 μH, -/+10%
Resonant Frequency	Pins 1-3, all other windings open	1200 kHz (Min.)
Primary Leakage Inductance	Pins 1-3, with Pins 7-10 shorted, measured at 100 kHz, 0.4 VRMS	28 μH (Max.)

7.3 Materials

Item	Description
[1]	Core: PC40 - EEL22 with air gap GAPPED ALG VALUE- 131nH/T^2
[2]	Bobbin: EEL-22, 10 Pin Bobbin (Ying Chin YC-2207/ Pin Shine P-2204 or equivalent)
[3]	Magnet Wire: #28 AWG Heavy Nyleze
[4]	Copper Foil 12 mm X 0.1 mm
[5]	Tape: 3M #44 Polyester Web Margin Tape 3 mm wide
[6]	Tape, 3M 1298 Polyester Film 18.5 mm, 0.002” Thick
[7]	Tape, 3M 1298 Polyester Film 12.5 mm, 0.002” Thick
[8]	Tape, 3M 1298 Polyester Film 4 mm, 0.002” Thick
[9]	Varnish

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7.4 Transformer Build Diagram

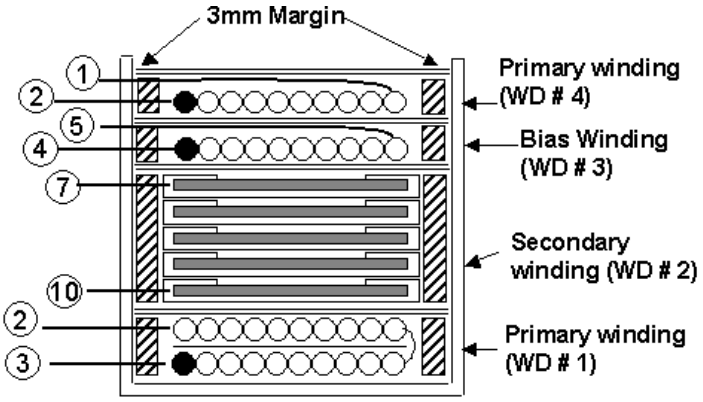

Figure 5a – Transformer Build Diagram.

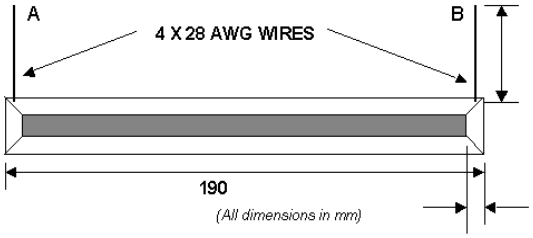

Figure 5b – Secondary Tape Preparation.

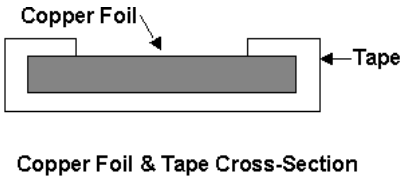

Figure 5c – Secondary Tape Cross-Section

7.5 Transformer Construction

Bobbin Preparation	Set up Bobbin with pins oriented to the left hand side
Primary Margin	Apply 3.0 mm wide margin to both sides of bobbin using item [5]. Match height of primary windings.
Primary WD#1	Start at Pin 3. Wind 30 turns of item [3] in approximately 1 layer. Add 1 Layer of Tape [7] for insulation. Wind remaining 30 primary turns, finish on Pin 2.
Basic Insulation	Use two layers of item [6] for basic insulation.
Secondary Margin	Apply 3.0 mm wide margin to both sides of bobbin using item [5]. Match height of secondary winding.
Secondary WD # 2	Prepare Copper Foil as shown in figure 5b & 5c above. Starting at Pin 10, wind 5 turns of item [4]. Finish at Pin 7.
Basic Insulation	Use two layers of item [6] for basic insulation.
Bias Margin	Apply 3.0 mm wide margin to both sides of bobbin using item [5]. Match height of bias winding
Bias Winding WD # 3	Start at Pins 4. Wind 14 turns of item [3]. Spread turns evenly across bobbin. Finish on Pins 5.
Basic Insulation	Use two layers of item [6] for insulation
Primary Margin	Apply 3.0 mm wide margin to both sides of bobbin using item [5]. Match height of 1 layer of primary winding.
Primary WD#4	Start at Pin 2. Wind 31 turns of item [3] and end at pin 1.
Outer Wrap	Wrap windings with 2 layers of tape item [6].
Core Assembly	Assemble cores item [1] on bobbin and secure using item [8].
Varnish	Dip Varnish using item [9]

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8 Transformer Spreadsheets

(Note – Output current is made 4.20 A in the spreadsheet to account for load on the auxiliary output)

ACDC_TinySwitch-III_020706; Rev.1.6; Copyright Power Integrations 2006	INPUT	INFO	OUTPUT	UNIT	ACDC_TinySwitch-III_020706_Rev1-6.xls; TinySwitch-III Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	295			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage (at continuous power)
IO	4.20			Amps	Power Supply Output Current (corresponding to peak power)
Power			21	Watts	Continuous Output Power
n	0.75				Efficiency Estimate at output terminals. Enter 0.7 if no better data available
Z	0.50				Z Factor. Ratio of secondary side losses to the total losses in the power supply. Use 0.5 if no better data available
tC	3.00			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	100.00		100	uFarads	Input Capacitance
ENTER TinySwitch-III VARIABLES					
TinySwitch-III	**TNY280**		**TNY280**		User defined TinySwitch-III
Chosen Device		*TNY280*			
Chose Configuration	**STD**		Standard Current Limit		Enter "RED" for reduced current limit (sealed adapters), "STD" for standard current limit or "INC" for increased current limit (peak or higher power applications)
ILIMITMIN			0.698	Amps	Minimum Current Limit
ILIMITTYP			0.750	Amps	Typical Current Limit
ILIMITMAX			0.802	Amps	Maximum Current Limit
fSmin			124000	Hertz	Minimum Device Switching Frequency
I^2fmin			66.825	A^2kHz	I^2f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	100.00		100	Volts	Reflected Output Voltage (VOR < 135 V Recommended)
VDS			10	Volts	TinySwitch-III on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
KP			0.49		Ripple to Peak Current Ratio (KP < 6)
KP_TRANSIENT			0.27		Transient Ripple to Peak Current Ratio. Ensure KP_TRANSIENT > 0.25
ENTER BIAS WINDING VARIABLES					
VB	15		15.00	Volts	Bias Winding Voltage
VDB			0.70	Volts	Bias Winding Diode Forward Voltage Drop
NB			13.64		Bias Winding Number of Turns
VZOV			21.00	Volts	Over Voltage Protection zener diode.
UVLO VARIABLES					
V_UV_TARGET			112.88	Volts	Target under-voltage threshold, above which the power supply with start
V_UV_ACTUAL			109.70	Volts	Typical start-up voltage based on standard value of RUV_ACTUAL
RUV_IDEAL			4.43	Mohms	Calculated value for UV Lockout resistor
RUV_ACTUAL			4.30	Mohms	Closest standard value of resistor to RUV_IDEAL
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**EEL22**		**EEL22**		User-Selected transformer core
Core		*EEL22*		*P/N:*	PC40EE22/29/6-Z
Bobbin		*EEL22_BOBBIN*		*P/N:*	EEL22_BOBBIN

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AE			0.358	cm^2	Core Effective Cross Sectional Area
LE			6.32	cm	Core Effective Path Length
AL			1400	nH/T^2	Ungapped Core Effective Inductance
BW			18	mm	Bobbin Physical Winding Width
M	3.20		3.2	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	3.00		3		Number of Primary Layers
NS	5		5		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			103	Volts	Minimum DC Input Voltage
VMAX			417	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Duty Ratio at full load, minimum primary inductance and minimum input voltage
IAVG			0.30	Amps	Average Primary Current
IP			0.6980	Amps	Minimum Peak Primary Current
IR			0.3448	Amps	Primary Ripple Current
IRMS			0.44	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1084	uHenries	Typical Primary Inductance. +/- 10% to ensure a minimum primary inductance of 985 uH
LP_TOLERANCE	10.00		10	%	Primary inductance tolerance
NP			91		Primary Winding Number of Turns
ALG			131	nH/T^2	Gapped Core Effective Inductance
BM			2671	Gauss	Maximum Operating Flux Density, BM<3000 is recommended
BAC			660	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1967		Relative Permeability of Ungapped Core
LG			0.31	mm	Gap Length (Lg > 0.1 mm)
BWE			34.8	mm	Effective Bobbin Width
OD			0.383	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.324	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			364	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			12.69	Amps	Peak Secondary Current
ISRMS			7.75	Amps	Secondary RMS Current
IRIPPLE			6.51	Amps	Output Capacitor RMS Ripple Current
CMS			1550	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			18	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
VOLTAGE STRESS PARAMETERS					
VDRAIN			647	Volts	Maximum Drain Voltage Estimate (Assumes 20% zener clamp tolerance and an additional 10% temperature tolerance)
PIVS			28	Volts	Output Rectifier Maximum Peak Inverse Voltage
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5	Volts	Main Output Voltage (if unused, defaults to

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					single output design)
IO1			4.200	Amps	Output DC Current
PO1			21.00	Watts	Output Power
VD1			0.500	Volts	Output Diode Forward Voltage Drop
NS1			5.00		Output Winding Number of Turns
ISRMS1			7.749	Amps	Output Winding RMS Current
IRIPPLE1			6.51	Amps	Output Capacitor RMS Ripple Current
PIVS1			28	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			**MBR1060**		Recommended Diodes for this output
CMS1			1550	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			18	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			1.03	mm	Minimum Bare Conductor Diameter
ODS1			2.32	mm	Maximum Outside Diameter for Triple Insulated Wire

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency.

9.1 Efficiency

(4 A Load on 5 V Output)

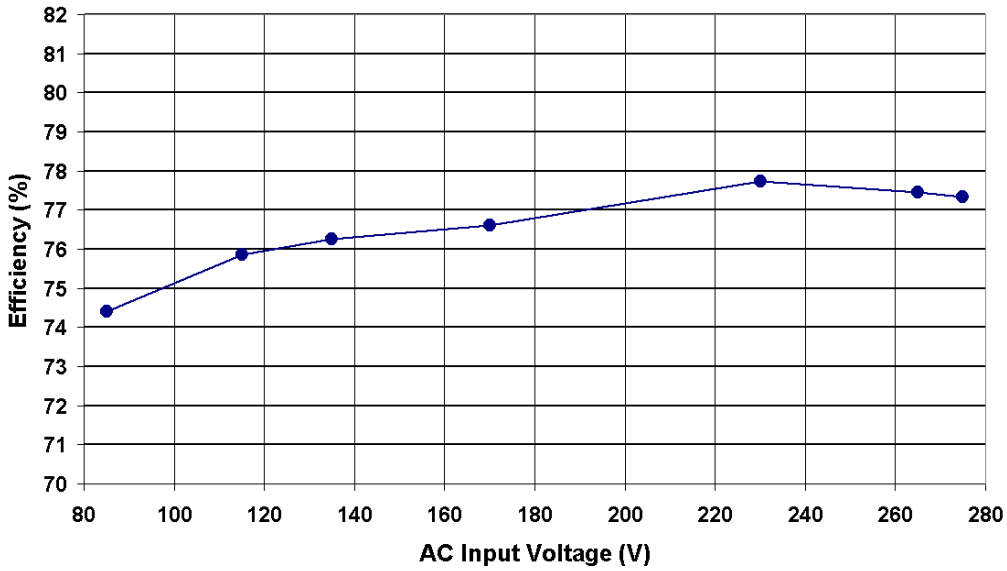

Figure 6 – Efficiency vs. Input Voltage, Room Temperature, 60 Hz.

9.2 No-load Input Power

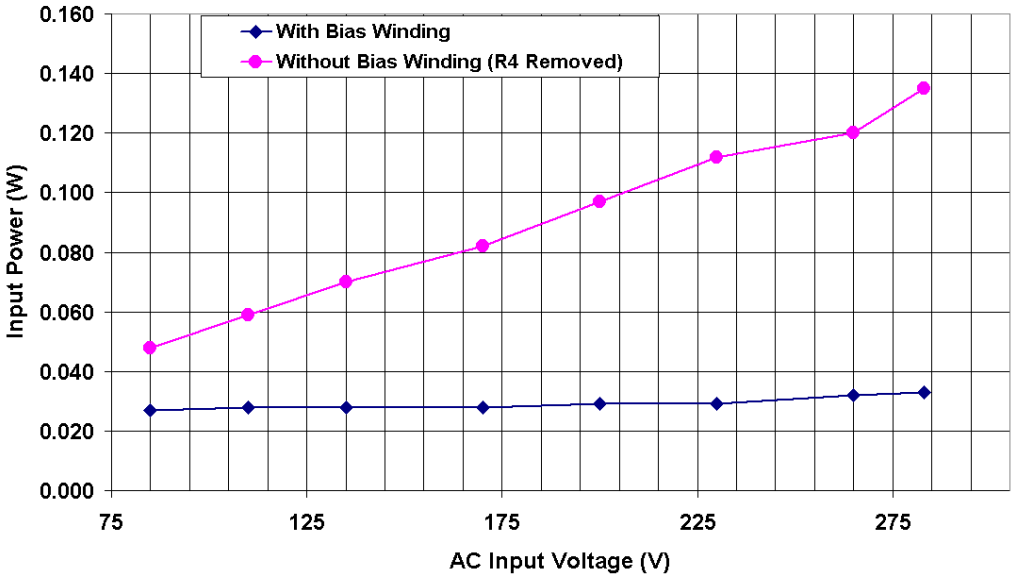

Figure 7 – Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

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9.3 0.5 W (5 V, 0.1 A) Load Input Power

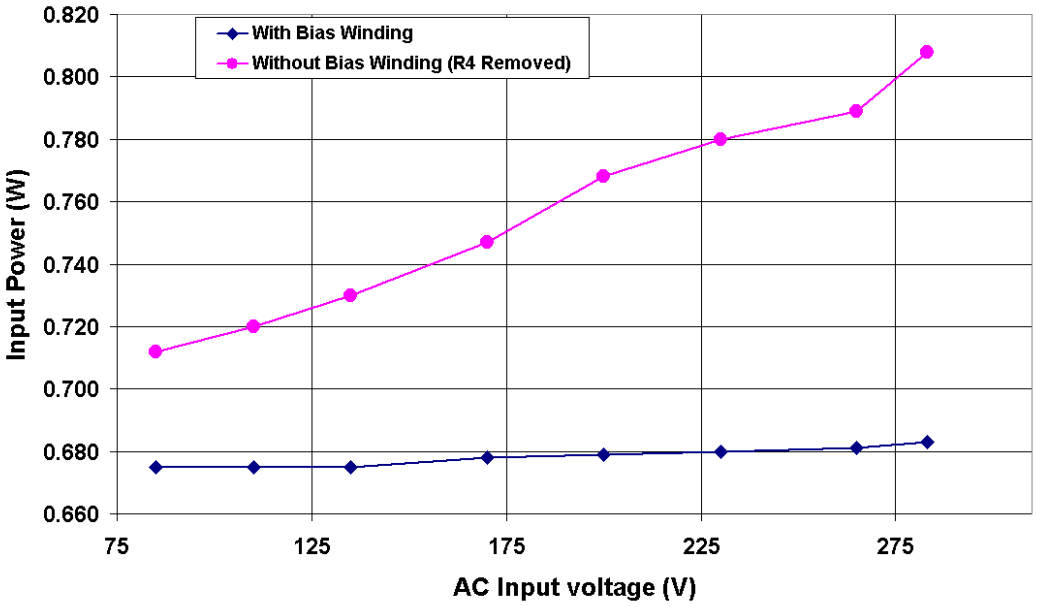

Figure 8 – 0.5 W Load – Input Power with & without bias winding.

9.4 Available Standby Output Power

The chart below shows the available output power vs. line voltage for an input power consumption of 1, 2 & 3 watts respectively. ON/OFF control is valuable in maintaining high efficiency under light load conditions, and helps meet many standby requirements.

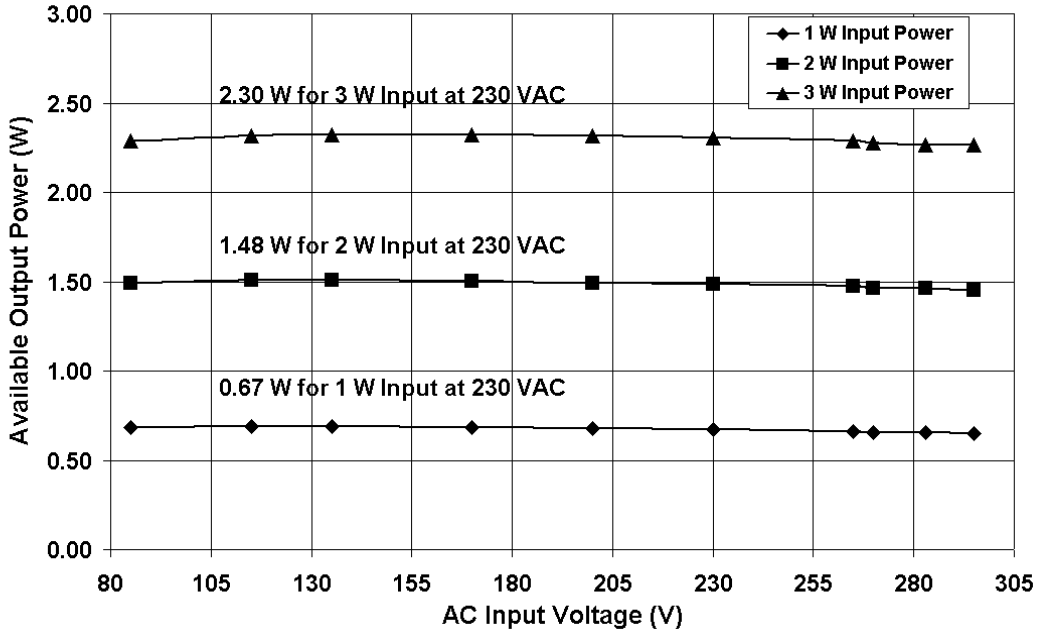

Figure 9 – Available Standby Output Power.

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9.5 Regulation

9.5.1 Load

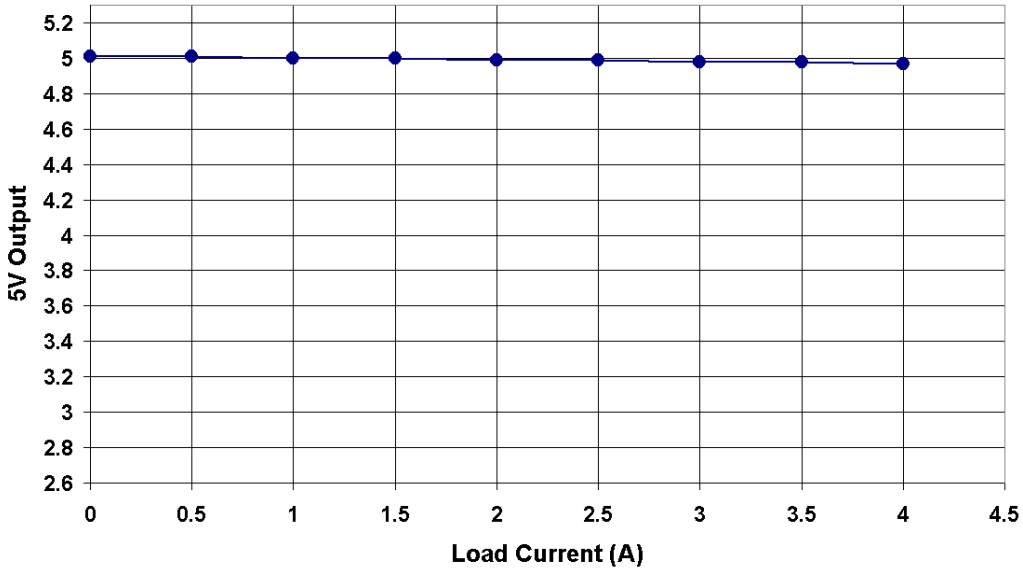

Figure 10 – Load Regulation, Room Temperature.

9.5.2 Line

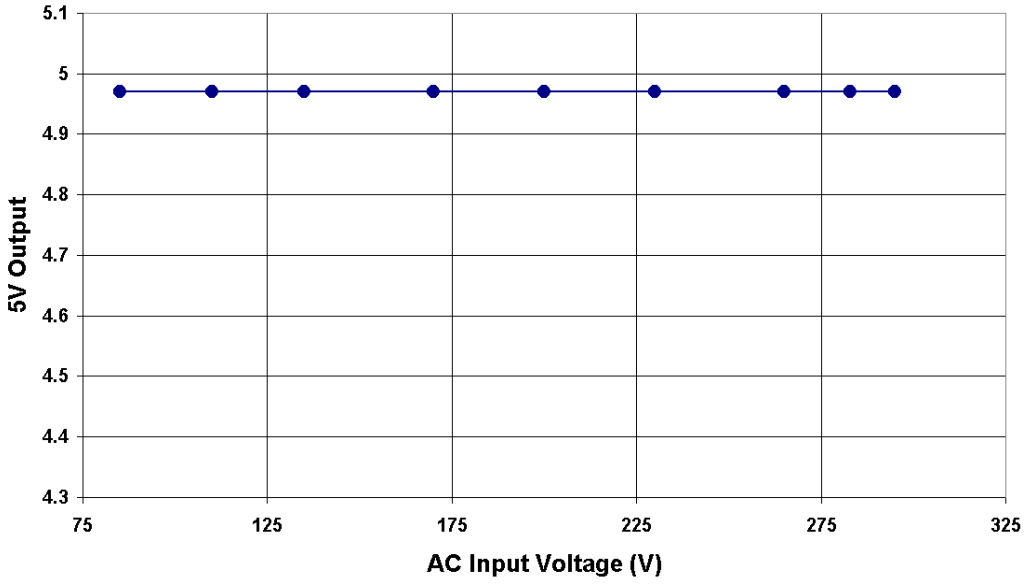

Figure 11 – Line Regulation, Room Temperature, Full Load.

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10 Thermal Performance

Temperature measurement of key components were taken using T-type Thermocouples. The thermocouples were attached directly to the SOURCE pin of the TNY280P device and the case of the output rectifier. The thermocouples were glued to the output capacitor & to the external core and winding surfaces of the transformer T1.

The cooling of the TNY280P is achieved through the copper plane on the PCB. It is necessary to provide adequately large copper area on the PCB attached to the SOURCE pins (5, 6, 7 and 8) of the DIP-8 package, to achieve the required cooling (se figure 3).

These results indicate an acceptable temperature rise of key components when ambient is increased to 50 ºC.

Item	Temperature (ºC)		
	85 VAC	115 VAC	230 VAC
Ambient	25	25	25
Transformer (T1) core	49.9	45	44
Transformer (T1) coil	52.4	50.6	49.6
***Tiny-Switch* (U1)**	62.3	56.3	49
Rectifier (D7) case	75	75	74

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

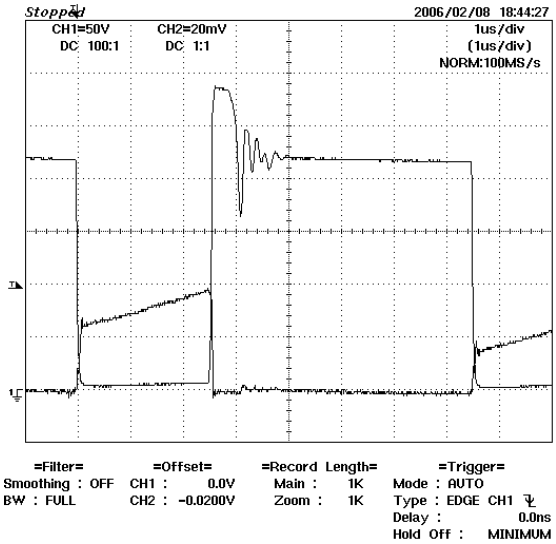

Figure 12 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 50 V / div
Lower: I_{DRAIN}, 0.4 A, 1 µs / div

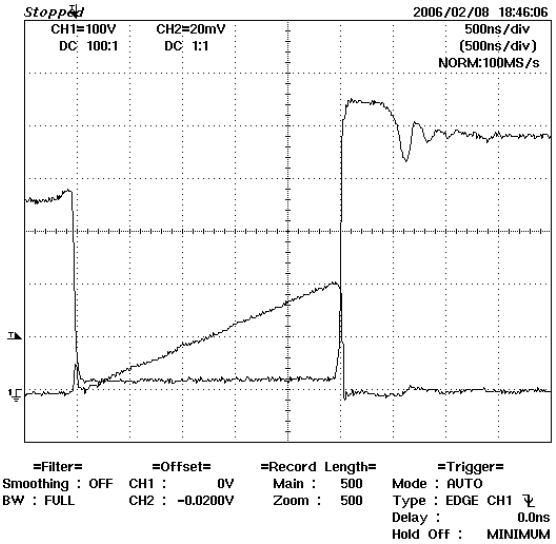

Figure 13 – 283 VAC, Full Load
Upper: V_{DRAIN}, 100 V / div
Lower: I_{DRAIN}, 0.4 A, 0.5 µs / div

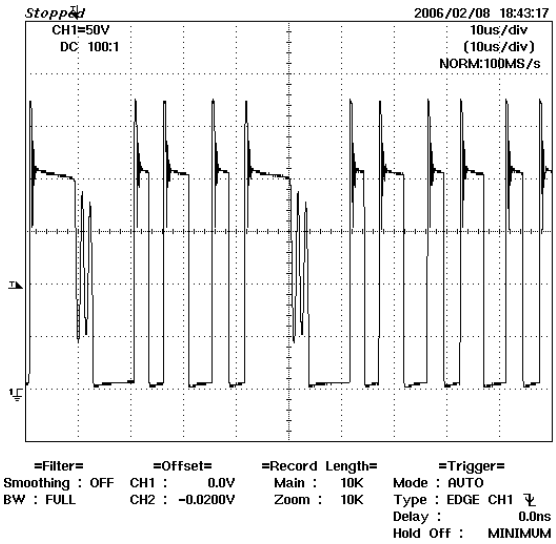

Figure 14 – 90 VAC, Full Load
V_{DRAIN}, 50 V, 10 µs / div.

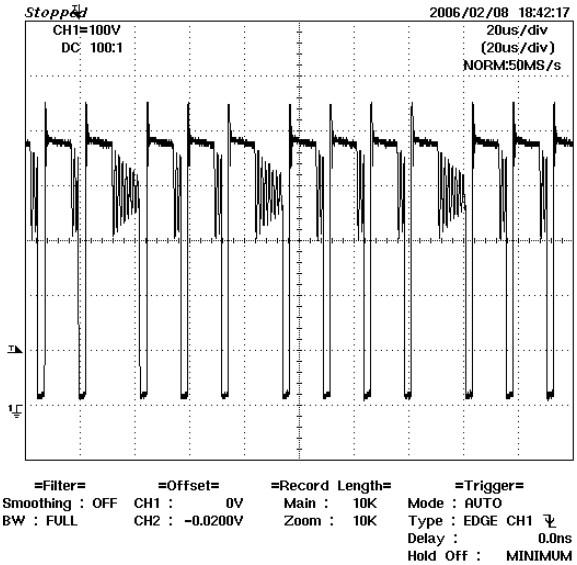

Figure 15 – 283 VAC, Full Load
V_{DRAIN}, 100 V, 20 µs / div.

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11.2 Drain Voltage & Current Startup Profile

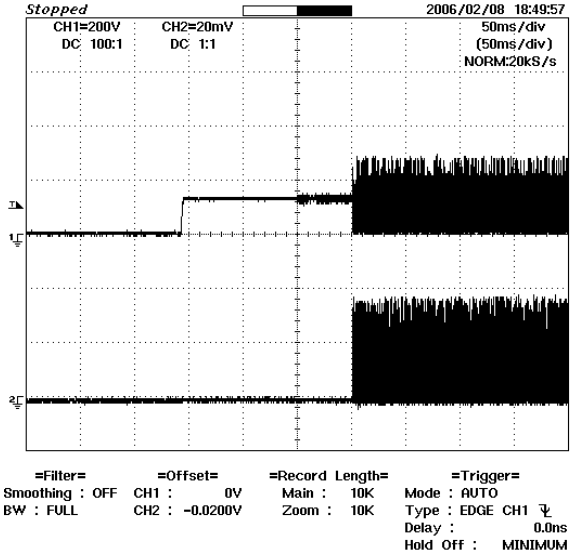

Figure 16 – Start-up Profile, 90 VAC
Upper: V_{DRAIN}, 200 V / div
Lower: I_{DRAIN}, 0.4 A, 50 ms / div

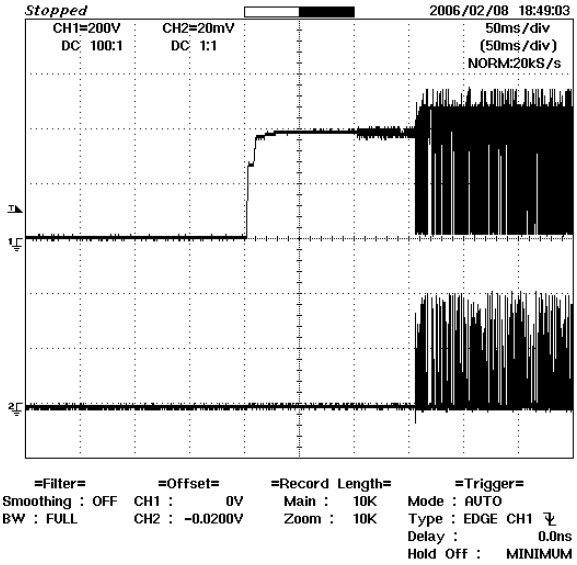

Figure 17 – Start-up Profile, 283 VAC
Upper: V_{DRAIN}, 200 V / div
Lower: I_{DRAIN}, 0.4 A, 50 ms / div

11.3 Output Voltage Startup Profile

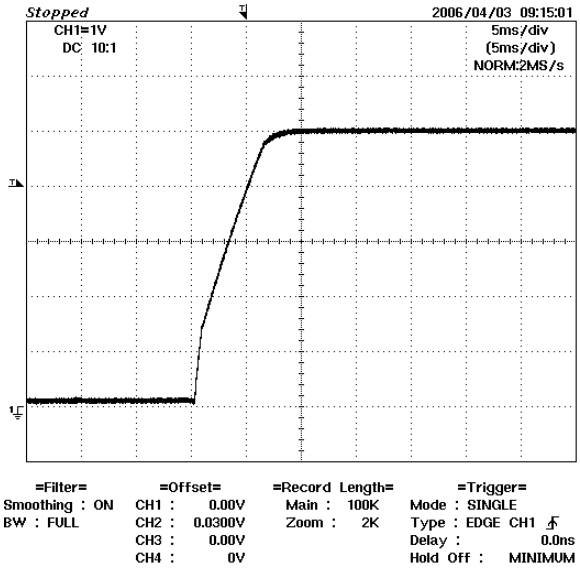

Figure 18 – Start-up Profile, 90 VAC (No Load)
V_{OUT}, 1 V, 5 ms / div.

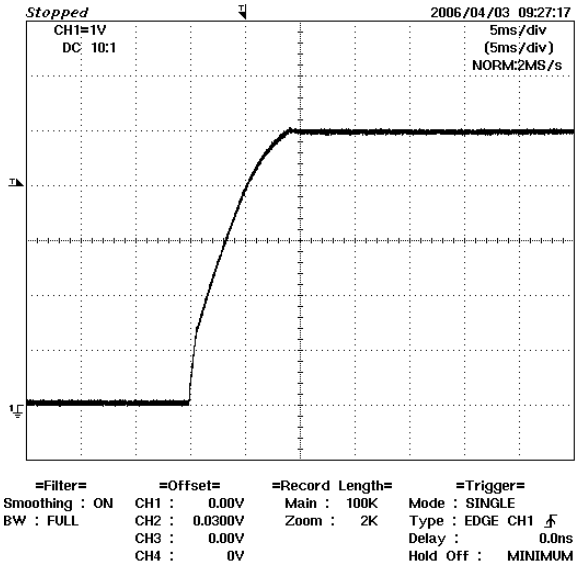

Figure 19 – Start-up Profile, 90 VAC (Full Load)
V_{OUT}, 1 V, 5 ms / div.

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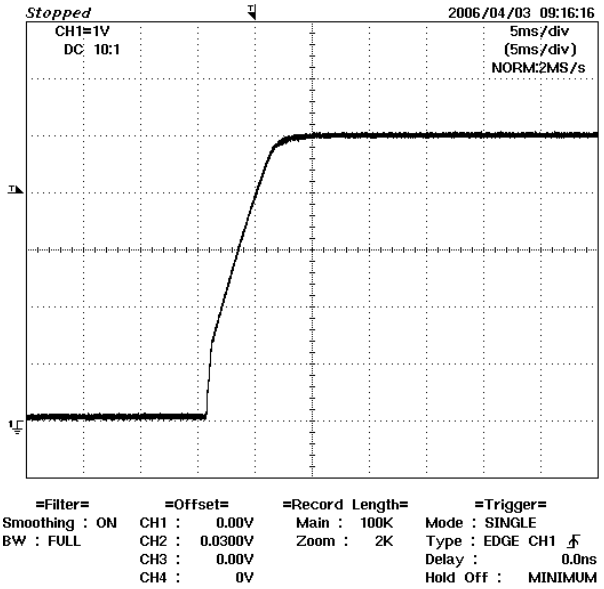

Figure 20 – Start-up Profile, 283 VAC (No Load)
V_{OUT}, 1 V, 5 ms / div

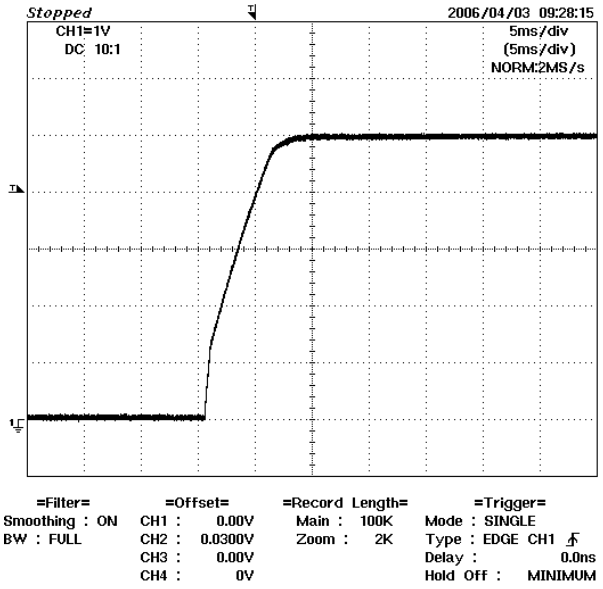

Figure 21 – Start-up Profile, 283 VAC (Full Load)
V_{OUT}, 1 V, 5 ms / div.

11.4 OV Shutdown

Two different OV Protection circuits can be designed with Tiny*Switch-III*. Figure 22 shows operation of primary side OV protection circuit (JP1 and JP2 not installed) and feedback disconnected to cause OV condition at the output.

Figure 23 shows OV protection offered by VR3, U4 & R10 circuit (Feedback disconnected during operation to cause OV condition at output).

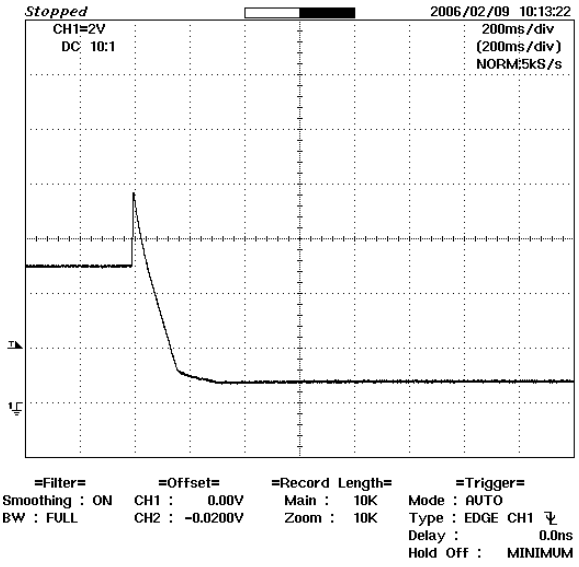

Figure 22 – 5 V Output Voltage.
V_{OUT}, 2 V, 200 ms / div

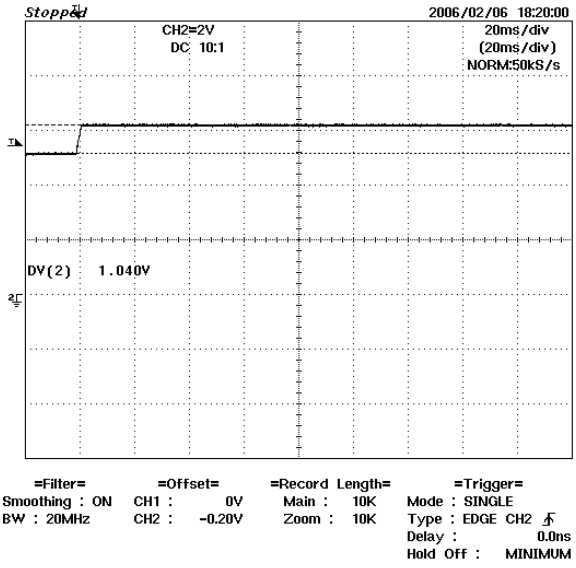

Figure 23 – 5 V Output Voltage.
V_{OUT}, 2 V, 20 ms / div.

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11.5 Load Transient Response (3 A to 4 A Load Step)

In the figures shown below, signal averaging was used to enable better viewing of the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving only the contribution from the load step response.

The waveforms (Figures 24 and 25) show an instantaneous voltage change of 70 mV for a 75% - 100% step load change. Increasing the size of the output filter capacitor minimizes the 70 mV change.

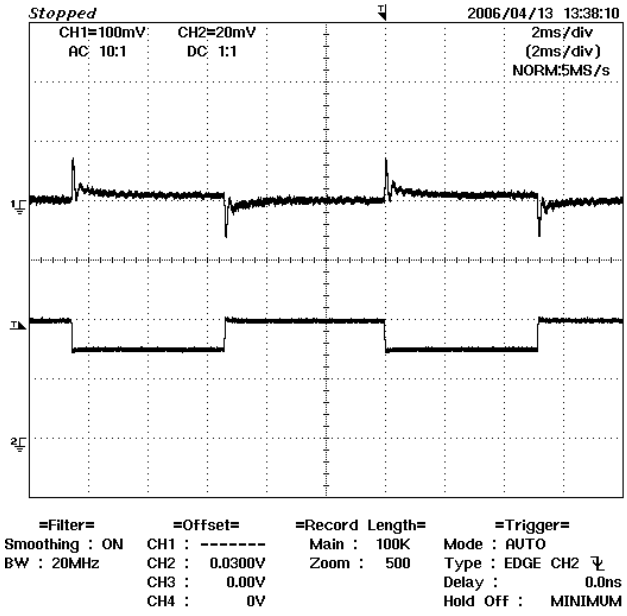

Figure 24 – Transient Response, 90 VAC
Upper: V_{OUT}, 100 mV, 2 ms / div
Lower: I_{OUT}, 3 A to 4 A Load Step

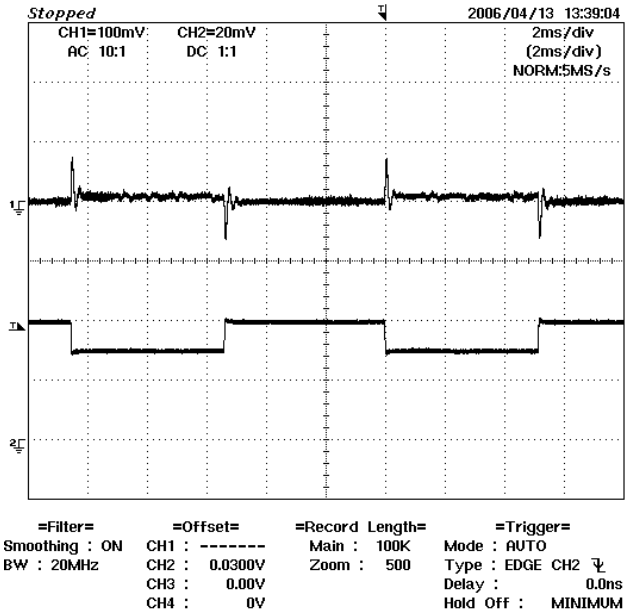

Figure 25 – Transient Response, 283 VAC
Upper: V_{OUT}, 100 mV, 2 ms / div
Lower: I_{OUT}, 3 A to 4 A Load Step

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11.6 Output Ripple Measurements

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 26 and Figure 27.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

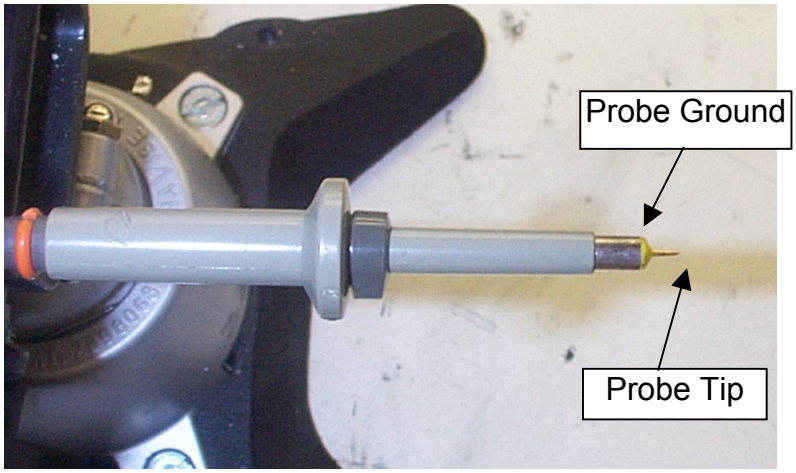

Figure 26 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

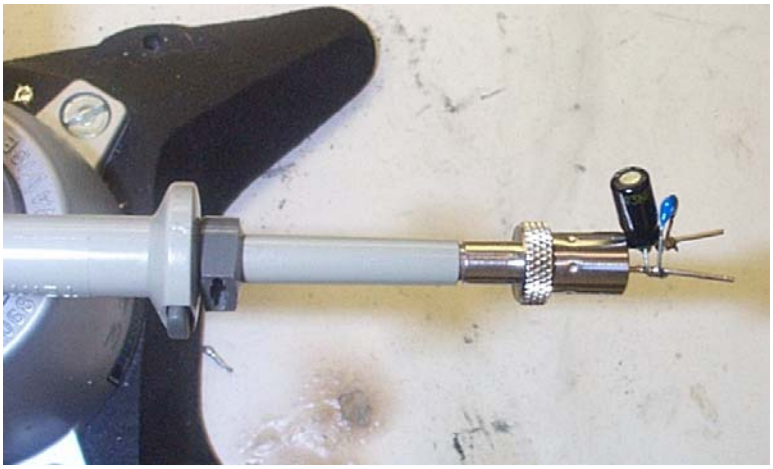

Figure 27 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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11.6.2 Measurement Results

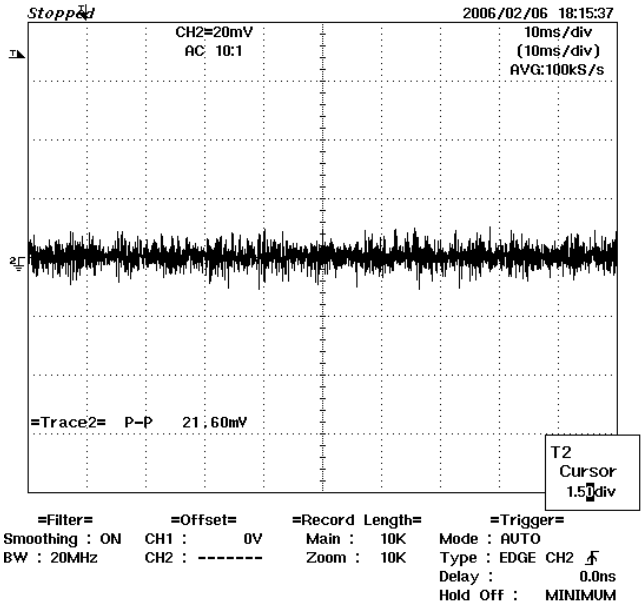

Figure 28 – 5 V Ripple, 90 VAC, Full Load.
V_{OUT}, 20 mV, 10 ms / div

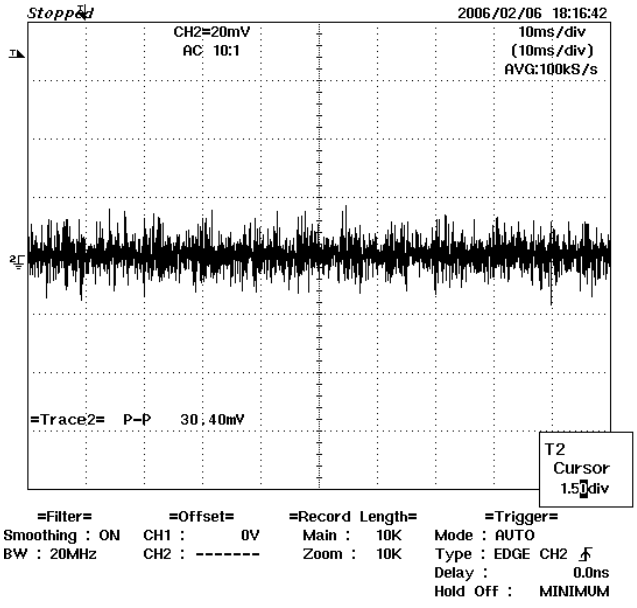

Figure 29 – 5 V Ripple, 283 VAC, Full Load.
V_{OUT}, 20 mV, 10 ms / div

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12 Design Notes:

1. Use of sufficient copper area directly under the TNY280P device, connected to the SOURCE pins of the IC is recommended for effective cooling. Generally, 1 square inch of symmetrical copper (2 oz) should be sufficient. However, actual temperature measurements should be used to determine adequacy. This is especially important when using the *TinySwitch-III* devices at or near the power levels specified on the datasheet output power table.

2. A dummy load (R2 in figure 2) was used in this design to ensure appropriate line & load regulation of the auxiliary output. Since this output is not directly regulated, it has a slightly higher output voltage when unloaded. The value of R13 should be selected, based on the current drawn by the external circuit that loads the auxiliary output. The filtering of the auxiliary output, and the need for an additional filter stage should be carefully evaluated, based on the load circuit's requirements.

3. R13 & C4 form a RC filter to reduce the ripple voltage on the auxiliary output

4. In many applications, the snubber circuit (R3, C3 & R1) can be eliminated, depending on the EMC compliance requirements of the system.

5. The size and specification of the output diode (D7) heat sink depends on load and operating conditions. In some designs, where augmented airflow is available, a small surface-area heat sink may be sufficient.

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13 Revision History

Date	Author	Revision	Description & changes	Reviewed
28-June-06	RJ	1.0	Initial Release	PV / JJ / KM

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