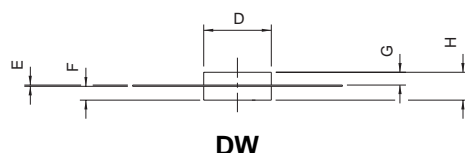
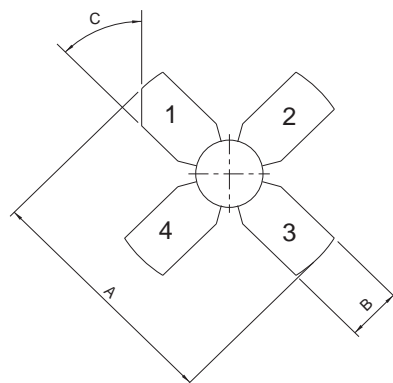


MECHANICAL DATA



PIN 1 DRAIN PIN 2 SOURCE
 PIN 3 GATE PIN 4 SOURCE

DIM	mm	Tol.	Inches	Tol.
A	26.16	0.38	1.030	0.015
B	5.72	0.13	0.225	0.005
C	45°	5°	45°	5°
D	7.11	0.13	0.280	0.005
E	0.13	0.03	0.005	0.001
F	1.52	0.13	0.055	0.005
G	0.43	0.20	0.060	0.008
H	7.67	REF	0.120	REF

**GOLD METALLISED
 MULTI-PURPOSE SILICON
 DMOS RF FET
 10W – 12.5V – 175MHz
 SINGLE ENDED**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS
 from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	50W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	10A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

Semelab Plc reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by Semelab is believed to be both accurate and reliable at the time of going to press. However Semelab assumes no responsibility for any errors or omissions discovered in its use. Semelab encourages customers to verify that datasheets are current before placing orders.

ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
B _V DSS Drain–Source Breakdown Voltage	V _{GS} = 0 I _D = 100mA	40			V
I _D DSS Zero Gate Voltage Drain Current	V _{DS} = 12.5V V _{GS} = 0			1	mA
I _G DSS Gate Leakage Current	V _{GS} = 20V V _{DS} = 0			1	µA
V _{GS(th)} Gate Threshold Voltage*	I _D = 10mA V _{DS} = V _{GS}	1		7	V
g _{fs} Forward Transconductance*	V _{DS} = 10V I _D = 1A	0.8			S
G _{PS} Common Source Power Gain	P _O = 10W	10			dB
η Drain Efficiency	V _{DS} = 12.5V I _{DQ} = 0.4A	50			%
VSWR Load Mismatch Tolerance	f = 175MHz	20:1			—
C _{iss} Input Capacitance	V _{DS} = 0 V _{GS} = -5V f = 1MHz			60	pF
C _{oss} Output Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			40	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = 12.5V V _{GS} = 0 f = 1MHz			4	pF

* Pulse Test: Pulse Duration = 300 µs , Duty Cycle ≤ 2%

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

R _{THj-case}	Thermal Resistance Junction – Case	Max. 3.5°C / W
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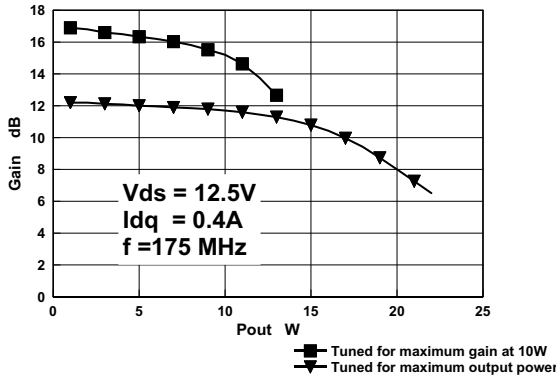


Figure 1 – Gain vs. Power Output.

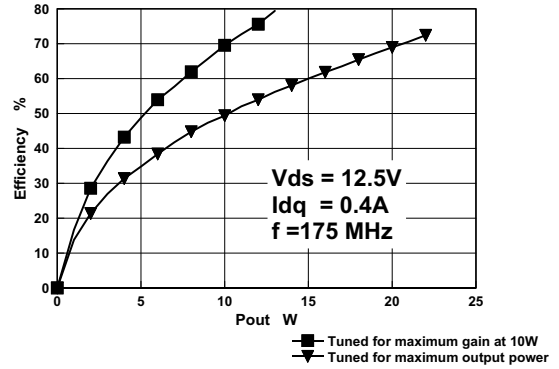


Figure 2 – Efficiency vs. Power Output.

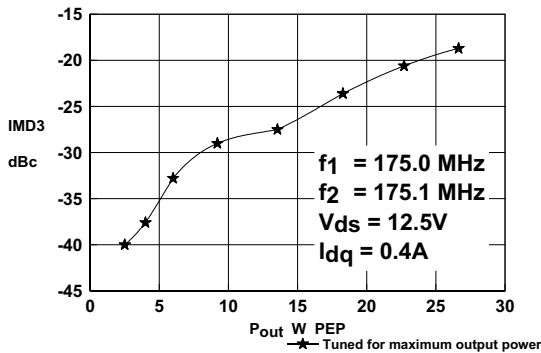


Figure 3 – IMD vs. Power Output.

D1221UK
OPTIMUM SOURCE AND LOAD IMPEDANCE

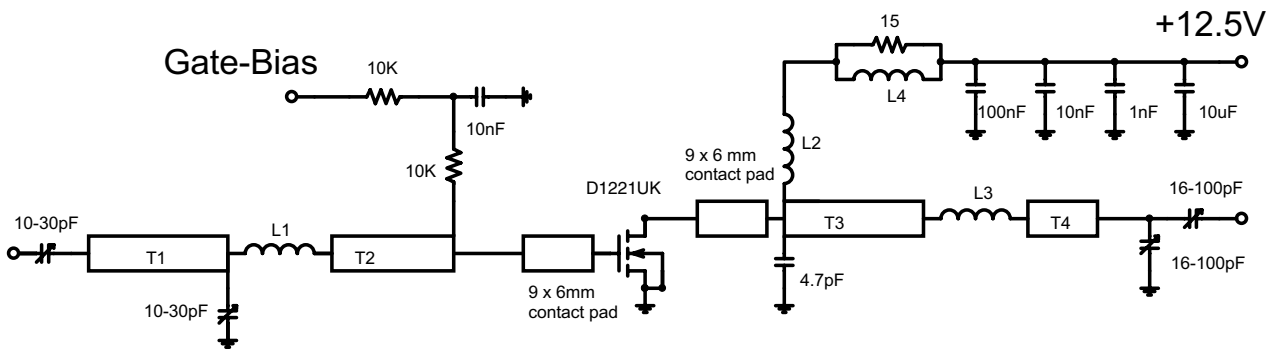
Frequency MHz	Z _S Ω	Z _L Ω
175MHz	7.2 + j15	4.1 - j2.5

Typical S Parameters

! V_{DS} = 12.5V, I_{DQ} = 0.4A
MHz S M A R 50

!Freq !MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
50	0.7	-116.5	14.93	97.9	0.036	15.7	0.64	-108.4
100	0.7	-140	7.42	73.6	0.03	2.7	0.65	-132
150	0.75	-150.2	4.56	58.1	0.02	11	0.71	-143.1
200	0.81	-157.2	3.1	46.5	0.016	52.3	0.78	-151.2
250	0.85	-163.1	2.23	37.4	0.026	82.6	0.83	-157.9
300	0.88	-168.1	1.67	30.3	0.04	90.1	0.86	-163.7
350	0.9	-172.6	1.3	24.7	0.055	90.8	0.89	-168.8
400	0.92	-176.6	1.04	20.3	0.071	89.2	0.91	-173.4
450	0.93	179.7	0.85	17.1	0.086	86.8	0.92	-177.5
500	0.94	176.3	0.71	14.9	0.101	84.2	0.93	178.7
550	0.95	173.1	0.6	13.5	0.115	81.5	0.94	175.2
600	0.9	170.	0.5	13	0.1	78.1	0.9	171.

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Substrate 1.6mm PTFE/glass, $\epsilon_r=2.5$

All microstrip lines $W=4.4\text{mm}$

T1 10mm

T2 13mm

T3 12mm

T4 4mm

L1 1.5 turns 22swg enamelled copper wire, 6mm i.d.

L2 10 turns 19swg enamelled copper wire, 6mm i.d.

L3 1.5 turns 22swg enamelled copper wire, 6mm i.d.

L4 13.5 turns 19swg enamelled copper wire on Siemens B64920A618X830 ferrite core

D1221UK 175MHz TEST FIXTURE