



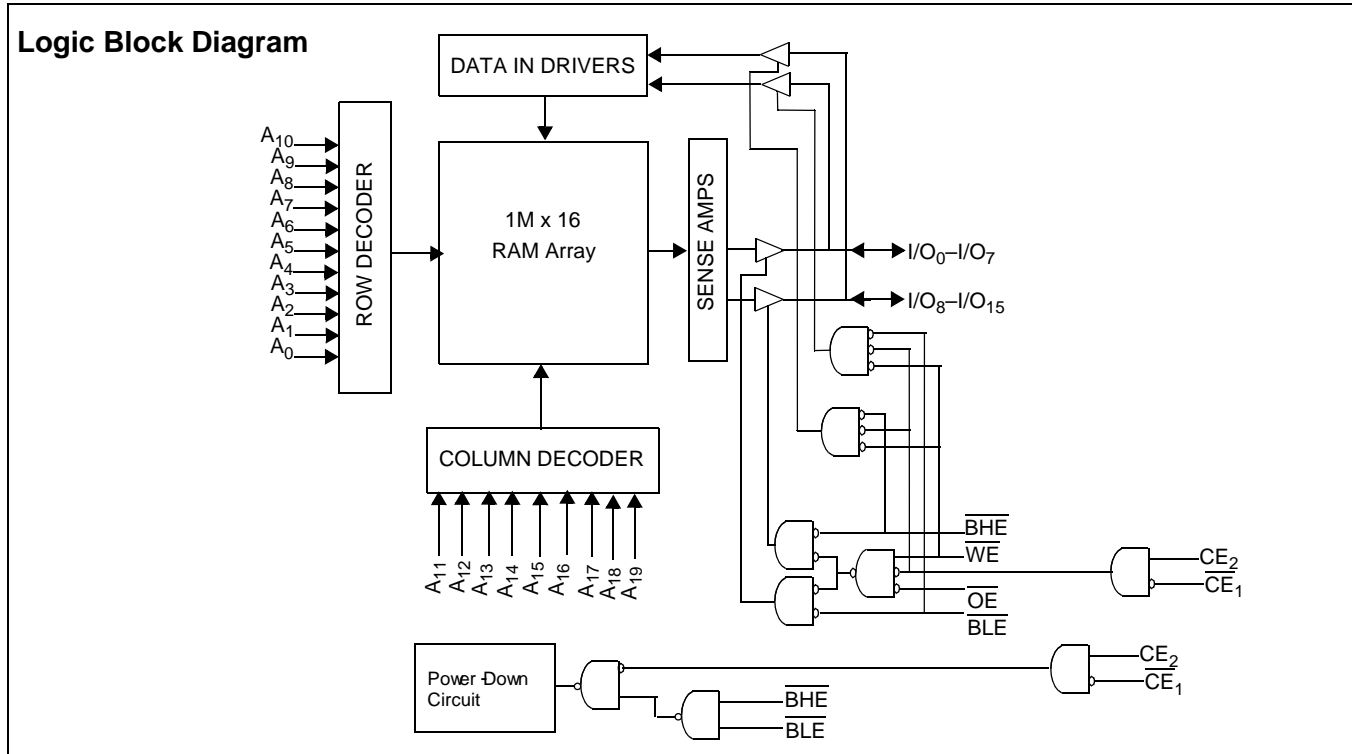
16-Mbit (1M x 16) Pseudo Static RAM

Features

- Advanced low-power MoBL[®] architecture
- High speed: 55 ns, 70 ns
- Wide voltage range: 2.7V to 3.3V
- Typical active current: 3 mA @ f = 1 MHz
- Typical active current: 13 mA @ f = f_{MAX}
- Low standby power
- Automatic power-down when deselected

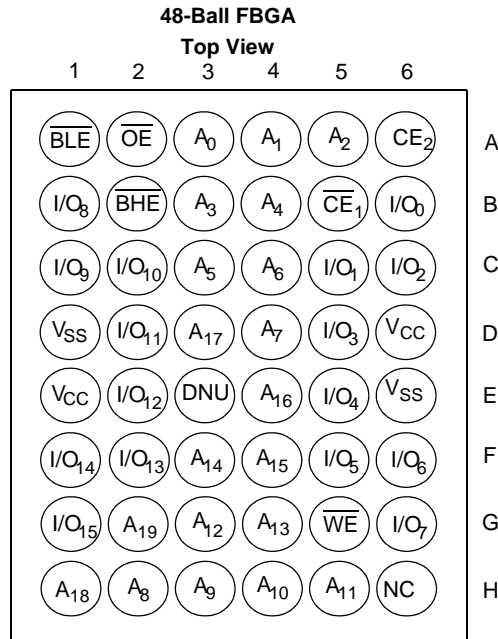
Functional Description^[1]

The CYK001M16SCCA is a high-performance CMOS pseudo static RAM (PSRAM) organized as 1M words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL) in portable applications such as cellular telephones. The device can be put into standby mode, reducing power consumption dramatically when deselected (\overline{CE}_1 LOW, CE_2 HIGH or both \overline{BHE} and \overline{BLE} are HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the chip is deselected (\overline{CE}_1 HIGH, CE_2 LOW) or \overline{OE} is deasserted HIGH, or during a write operation (Chip Enabled and Write Enable \overline{WE} LOW). Reading from the device is accomplished by asserting the Chip Enables (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the Truth Table for a complete description of read and write modes.



Note:

1. For best-practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2, 3, 4]

Product Portfolio^[5]

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	Min.	Typ.	Max.		f = 1 MHz		f = f _{MAX}			
					Typ. ^[5]	Max.	Typ. ^[5]	Max.		
CYK001M16SCCA	2.7	3.0	3.3	55	3	5	13	22	80	150
				70				17		

Notes:

2. DNU pins are to be left floating or tied to V_{SS}.
3. Ball H6 is the address expansion pins for the 32-Mb density.
4. NC "no connect"—not connected internally to the die.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (typ) and T_A = 25°C.



Maximum Ratings^[6, 7, 8]

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -40°C to +85°C
- Supply Voltage to Ground Potential -0.4V to 4.6V
- DC Voltage Applied to Outputs in High-Z State^[6, 7, 8] -0.4V to 3.3V

- DC Input Voltage^[6, 7, 8] -0.4V to 3.3V
- Output Current into Outputs (LOW) 20 mA
- Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature (T _A)	V _{CC}
Industrial	-25°C to +85°C	2.7V to 3.3V

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	CYK001M16SCCA-55			CYK001M16SCCA-70			Unit
			Min.	Typ. ^[5]	Max.	Min.	Typ. ^[5]	Max.	
V _{CC}	Supply Voltage		2.7	3.0	3.3	2.7		3.3	V
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} - 0.4			V _{CC} - 0.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA			0.4			0.4	V
V _{IH}	Input HIGH Voltage		0.8 * V _{CC}		V _{CC} + 0.4	0.8 * V _{CC}		V _{CC} + 0.4	V
V _{IL}	Input LOW Voltage	f = 0	-0.4		0.4	-0.4		0.4	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		13	22		13	17	mA
		f = 1 MHz		3	5		3	5	
I _{SB1}	Automatic CE Power-down Current —CMOS Inputs	CE ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V, f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE and BLE), V _{CC} = 3.3V		100	525		100	525	μA
I _{SB2}	Automatic CE Power-down Current —CMOS Inputs	CE ≥ V _{CC} - 0.2V, CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, f = 0, V _{CC} = 3.3V		80	150		80	150	μA

Capacitance^[9]

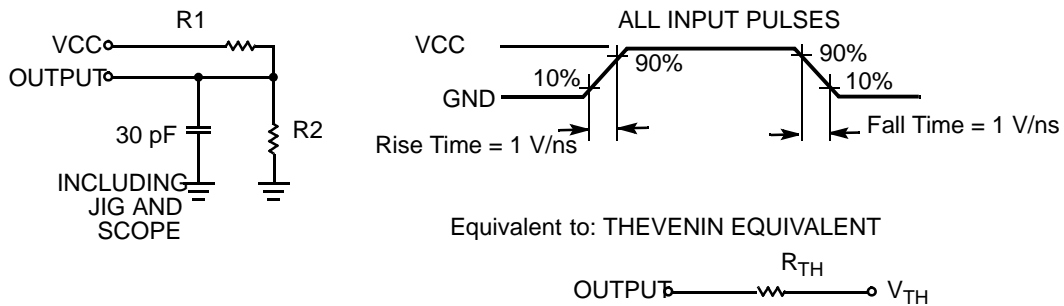
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz	8	pF
C _{OUT}	Output Capacitance	V _{CC} = V _{CC(typ)}	8	pF

Notes:

6. V_{IH(MAX)} = V_{CC} + 0.5V for pulse durations less than 20 ns.
7. V_{IL(MIN)} = -0.5V for pulse durations less than 20 ns.
8. Overshoot and undershoot specifications are characterized and are not 100% tested.
9. Tested initially and after design or process changes that may affect these parameters.

Thermal Resistance^[9]

Parameter	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55	$^{\circ}\text{C}/\text{W}$
θ_{JC}	Thermal Resistance (Junction to Case)		17	$^{\circ}\text{C}/\text{W}$

AC Test Loads and Waveforms


Parameters	3.0V V _{CC}	Unit
R1	22000	Ω
R2	22000	Ω
R _{TH}	11000	Ω
V _{TH}	1.50	V

Switching Characteristics (Over the Operating Range)^[10, 11, 12, 13]

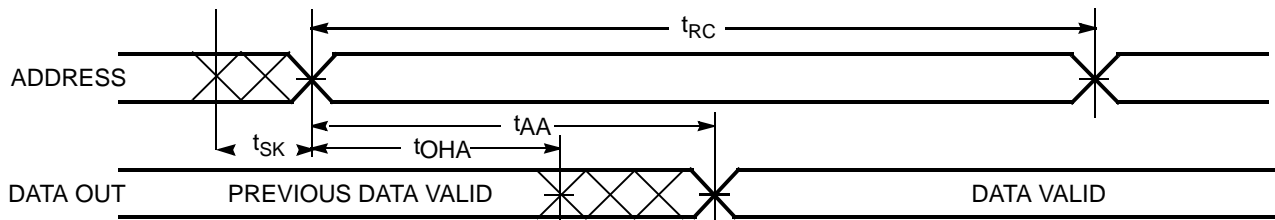
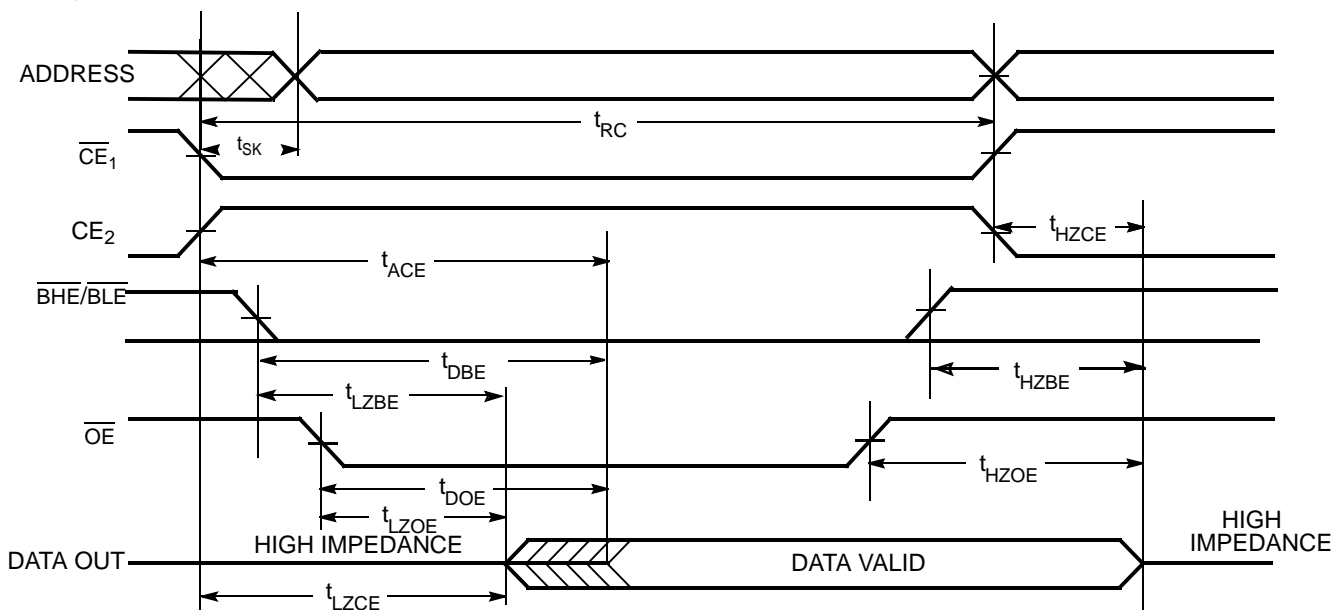
Parameter	Description	CYK001M16SCCA-55		CYK001M16SCCA-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55 ^[14]		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		5		ns
t _{ACE}	$\overline{\text{CE}}_1$ LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z ^[11, 12]	5		5		ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[11, 12]		25		25	ns
t _{LZCE}	$\overline{\text{CE}}_1$ LOW and CE ₂ HIGH to Low Z ^[11, 12]	5		5		ns
t _{HZCE}	$\overline{\text{CE}}_1$ HIGH and CE ₂ LOW to High Z ^[11, 12]		25		25	ns
t _{DBE}	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Data Valid		55		70	ns
t _{LZBE}	$\overline{\text{BLE}}/\overline{\text{BHE}}$ LOW to Low Z ^[11, 12]	5		5		ns
t _{HZBE}	$\overline{\text{BLE}}/\overline{\text{BHE}}$ HIGH to High-Z ^[11, 12]		10		25	ns
t _{SK} ^[14]	Address Skew		0		10	ns

Notes:

- Test conditions assume signal transition time of 1 V/ns or higher, timing reference levels of V_{CC(typ)}/2, input pulse levels of 0V to V_{CC(typ)}, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- The internal write time of the memory is defined by the overlap of $\overline{\text{WE}}$, CE₁ = V_{IL}, CE₂ = V_{IH}, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = \text{V}_{\text{IL}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates write.
- To achieve 55-ns performance, the read access should be $\overline{\text{CE}}$ controlled. In this case t_{ACE} is the critical parameter and t_{SK} is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

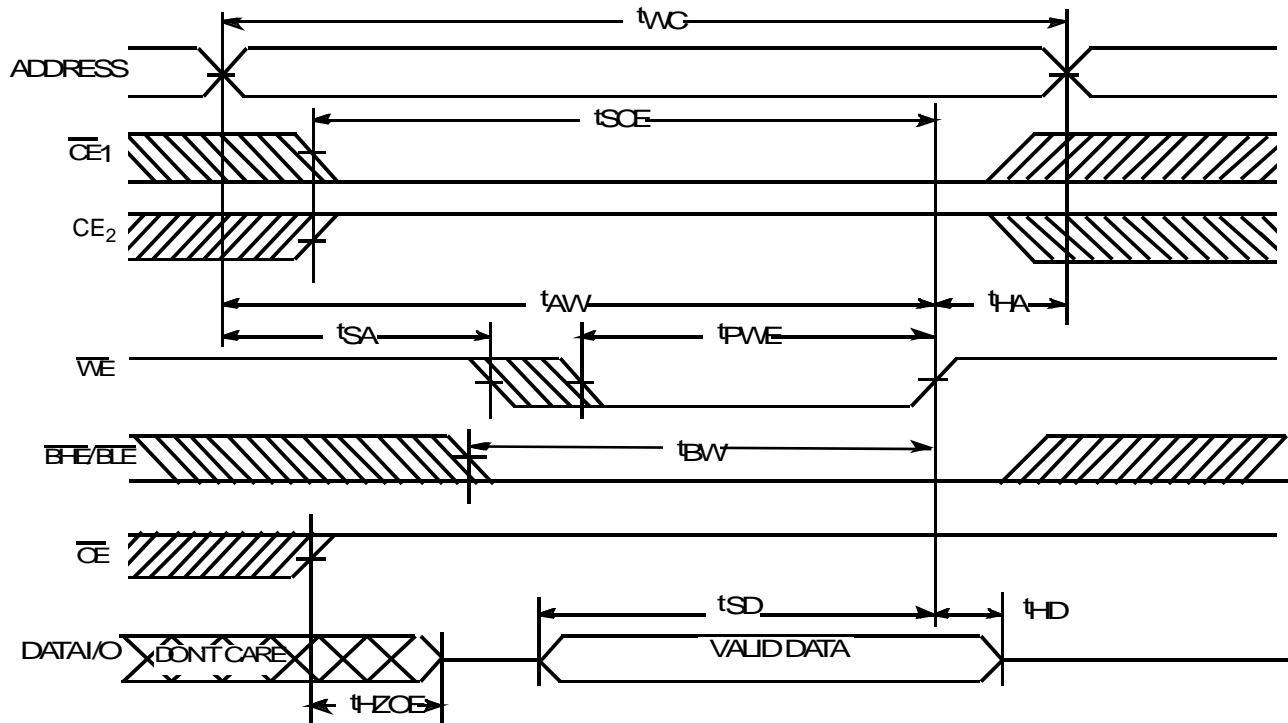
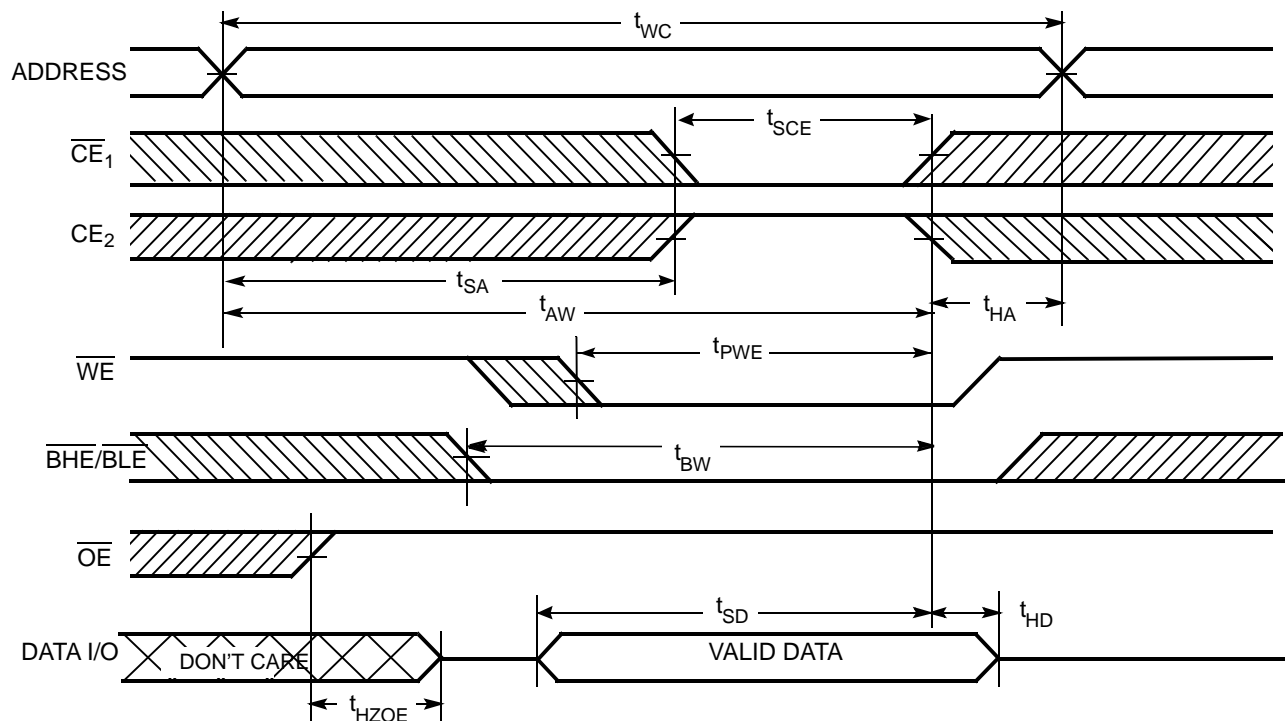
Switching Characteristics (Over the Operating Range)^[10, 11, 12, 13] (continued)

Parameter	Description	CYK001M16SCCA-55		CYK001M16SCCA-70		Unit
		Min.	Max.	Min.	Max.	
Write Cycle^[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	45		55		ns
t_{AW}	Address Set-up to Write End	45		55		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	\overline{WE} Pulse Width	40		55		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	50		55		ns
t_{SD}	Data Set-up to Write End	25		25		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[11, 12]		25		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[11, 12]	5		5		ns

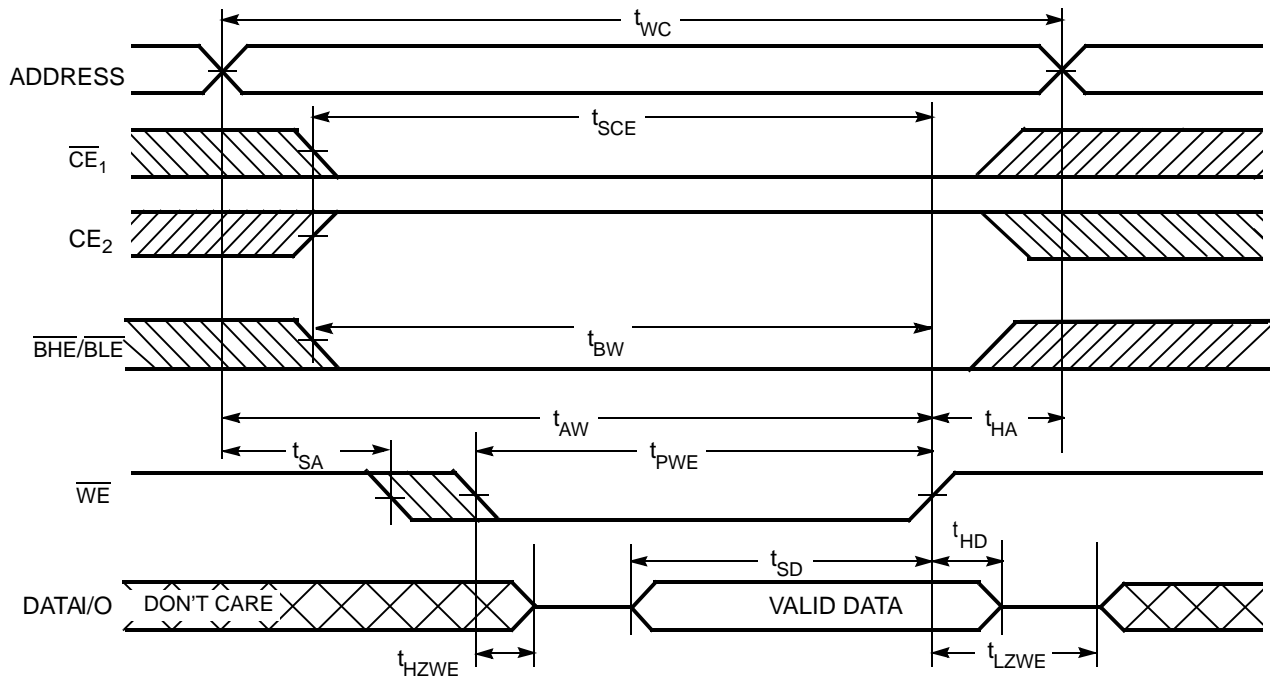
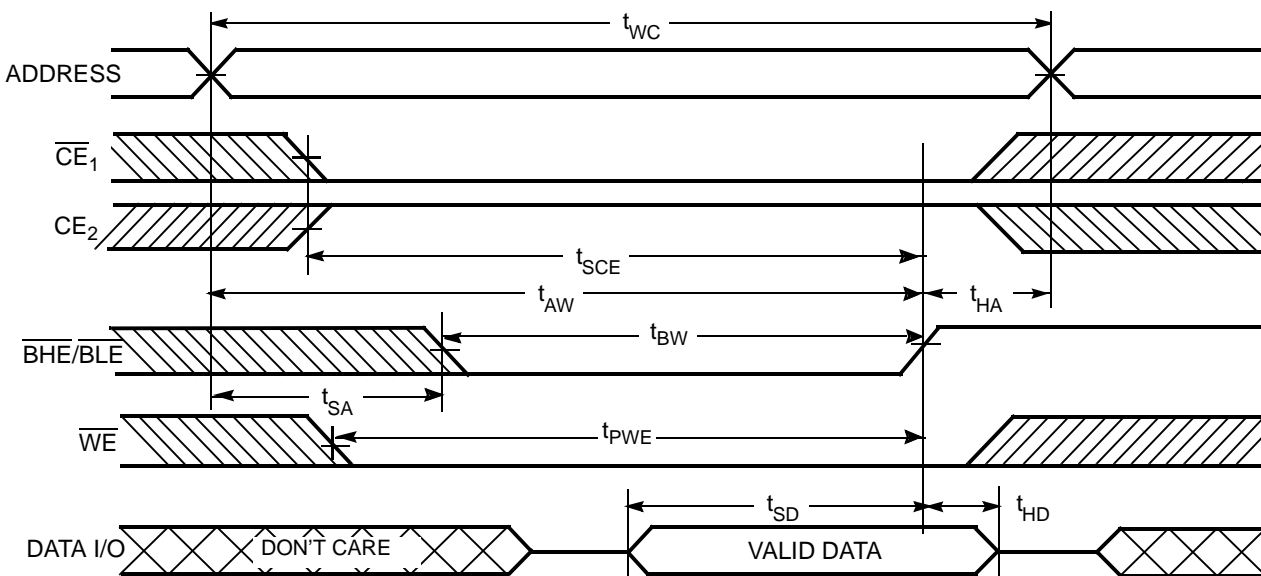
Switching Waveforms
Read Cycle 1 (Address Transition Controlled)^[14, 15, 16]

Read Cycle 2 (\overline{OE} Controlled)^[14, 16]

Notes:

15. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$ and $CE_2 = V_{IH}$.

16. \overline{WE} is HIGH for Read Cycle.

Switching Waveforms (continued)
Write Cycle No. 1 (WE Controlled)^[12, 13, 17, 18, 19]

Write Cycle 2 (CE1 or CE2 Controlled)^[12, 13, 17, 18, 19]

Notes:

17. Data I/O is high impedance if $\overline{OE} \geq V_{IH}$.
18. If Chip Enable goes INACTIVE simultaneously with $\overline{WE} = \text{HIGH}$, the output remains in a high-impedance state.
19. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)^[18, 19]

Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[18, 19]


Truth Table^[20]

\overline{CE}_1	CE_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write (Upper Byte and Lower Byte)	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0 – I/O_7); I/O_8 – I/O_{15} in High Z	Write (Lower Byte Only)	Active (I_{CC})
L	H	L	X	L	H	Data In (I/O_8 – I/O_{15}); I/O_0 – I/O_7 in High Z	Write (Upper Byte Only)	Active (I_{CC})

Ordering Information

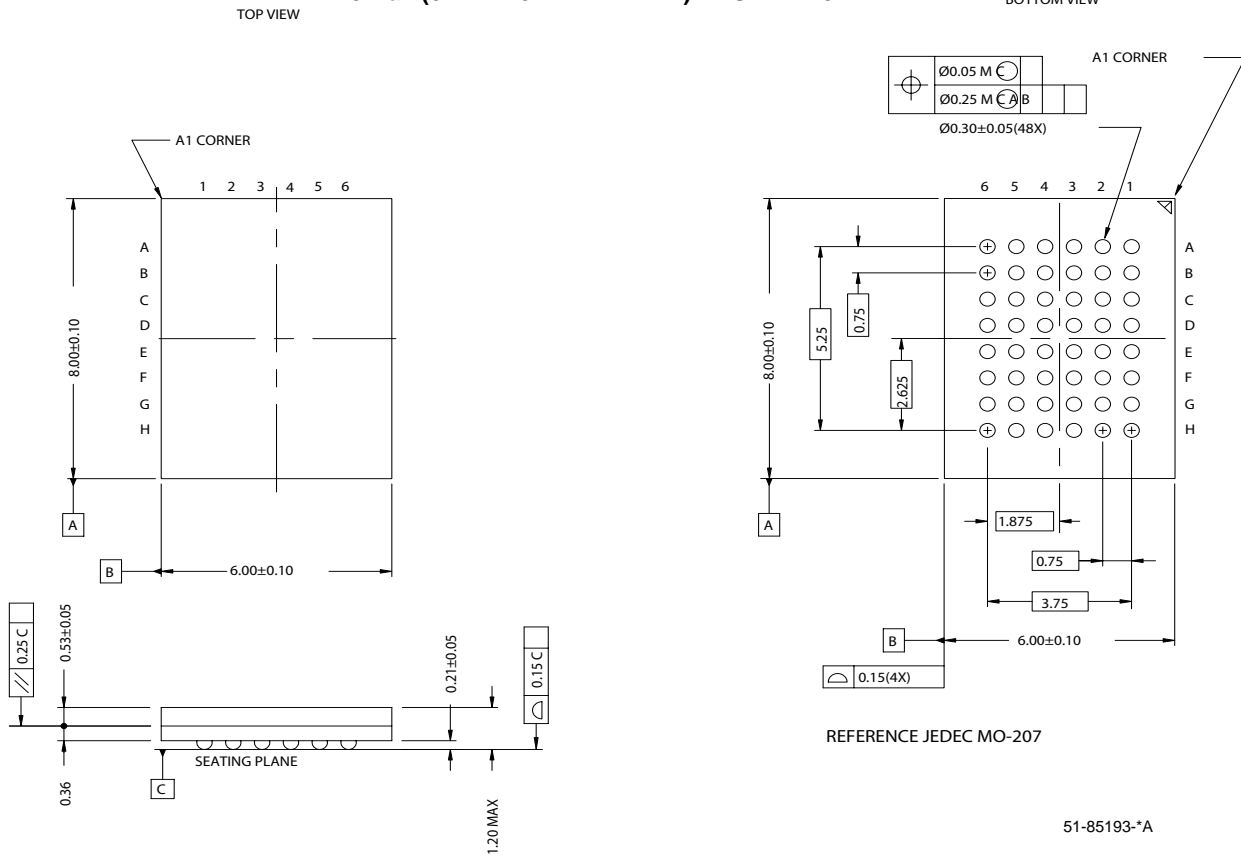
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CYK001M16SCCAU-55BAI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm)	Industrial
70	CYK001M16SCCAU-70BAI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm)	Industrial
55	CYK001M16SCAU-55BAXI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial
70	CYK001M16SCAU-70BAXI	BA48K	48-ball Fine Pitch BGA (6.0 x 8.0 x 1.2 mm) (Pb-Free)	Industrial

Note:

20. H = Logic HIGH, L = Logic LOW, X = Don't Care

Package Diagrams

48-Ball (6 mm x 8mm x 1.2 mm) FBGA BA48K



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Document History Page

Document Title: CYK001M16SCCA 16-Mbit (1M x 16) Pseudo Static RAM				
Document Number: 38-05426				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	130539	01/27/04	AWK	New Data Sheet
*A	216680	03/26/04	REF	Added 55-ns Speed bin Updated from Advance Information to Final data sheet.
*B	220121	See ECN	REF	Changed the t_{OHA} parameter for 70 ns speed grade from 10 ns to 5 ns
*C	225580	See ECN	AJU	Changed Ordering code from CYK001M16SCCA to CYK001M16SCCAU on page 8
*D	313999	See ECN	RKF	Added Pb-Free parts to the Ordering information