

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator**Description**

The CXP84700 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP84716/84720/84724.

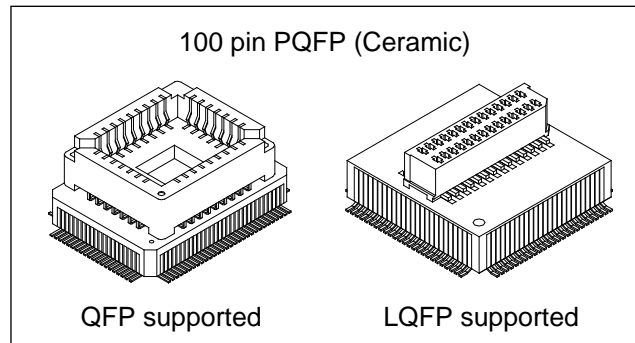
Features

- A wide instruction set (213 instructions) which covers various types of data.
 - 16-bit operation/multiplication and division/
Boolean bit operation instructions
- Minimum instruction cycle 333ns at 12MHz operation (3.0 to 5.5V)
 250ns at 16MHz operation (4.5 to 5.5V)
- Applicable EPROM LCC type 27C512
 (Maximum 60K bytes are available.)
- Incorporated RAM capacity 2144 bytes
- Peripheral functions
 - A/D converter 8 bits, 8 channels, successive approximation method
(Conversion time of 1.6 μ s/16MHz)
 - Serial interface Start-stop sync type (UART), 1 channel
 Incorporated buffer RAM
(Auto transfer for 1 to 32 bytes), 2 channels
8-bit clock sync type (MSB/LSB first selectable), 1 channel
 - Timer 8-bit timer, 8-bit timer/counter,
 19-bit time base timer, 16-bit capture timer/counter
 - High precision timing pattern generator PPG: maximum of 11-pins, 16-stages programmable, 2 channels
 - PWM output 8 bits, 8 channels
 - FRC capture unit Incorporated 24-bit and 6-stage FIFO
- Interruption 19 factors, 15 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP84700. Refer to the Products List for details.

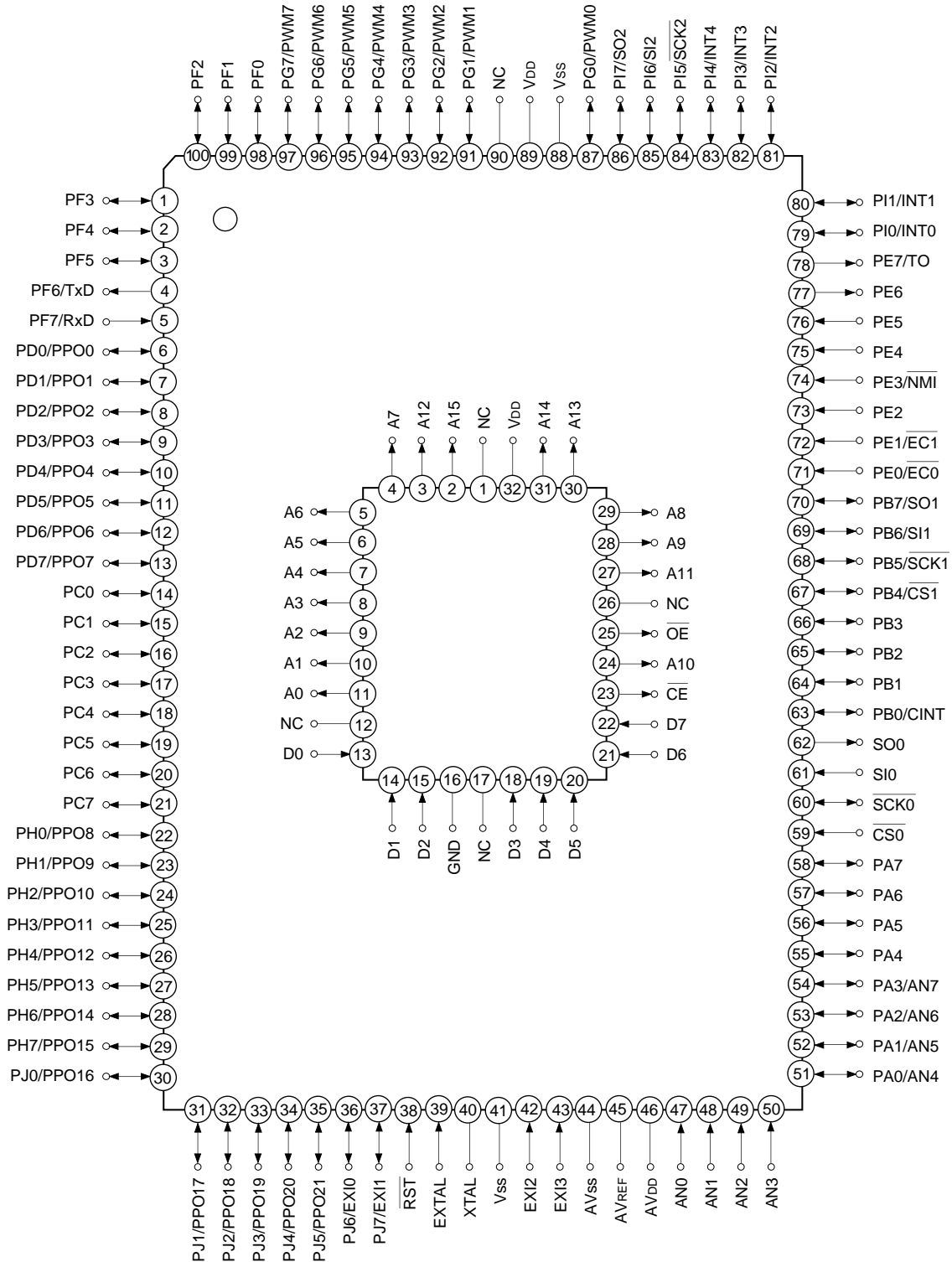
Structure

Silicon gate CMOS IC



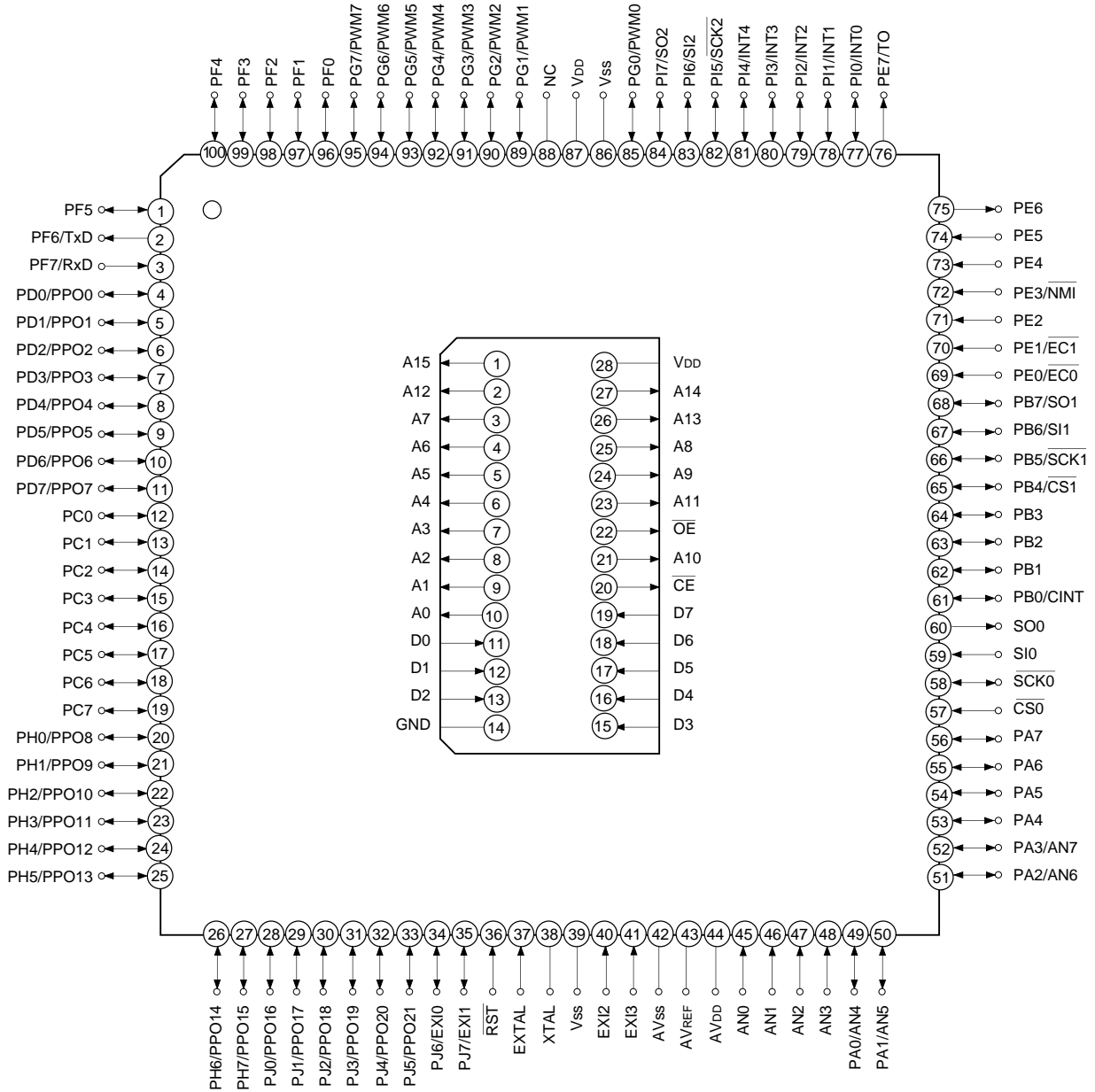
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Pin Assignment in Piggyback Mode (QFP package)



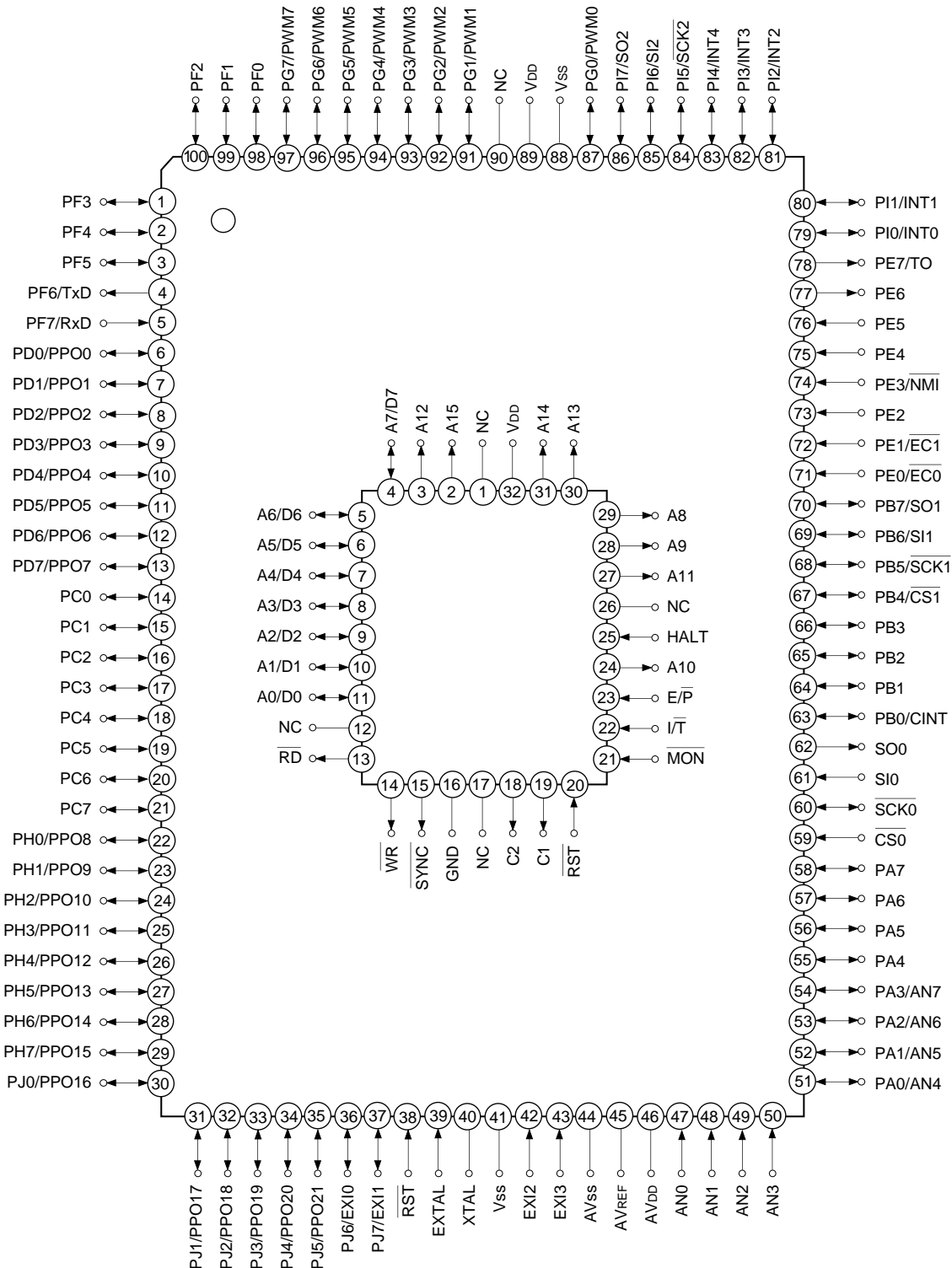
Note) 1. NC (Pin 90) is left open.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment in Piggyback Mode (LQFP package)



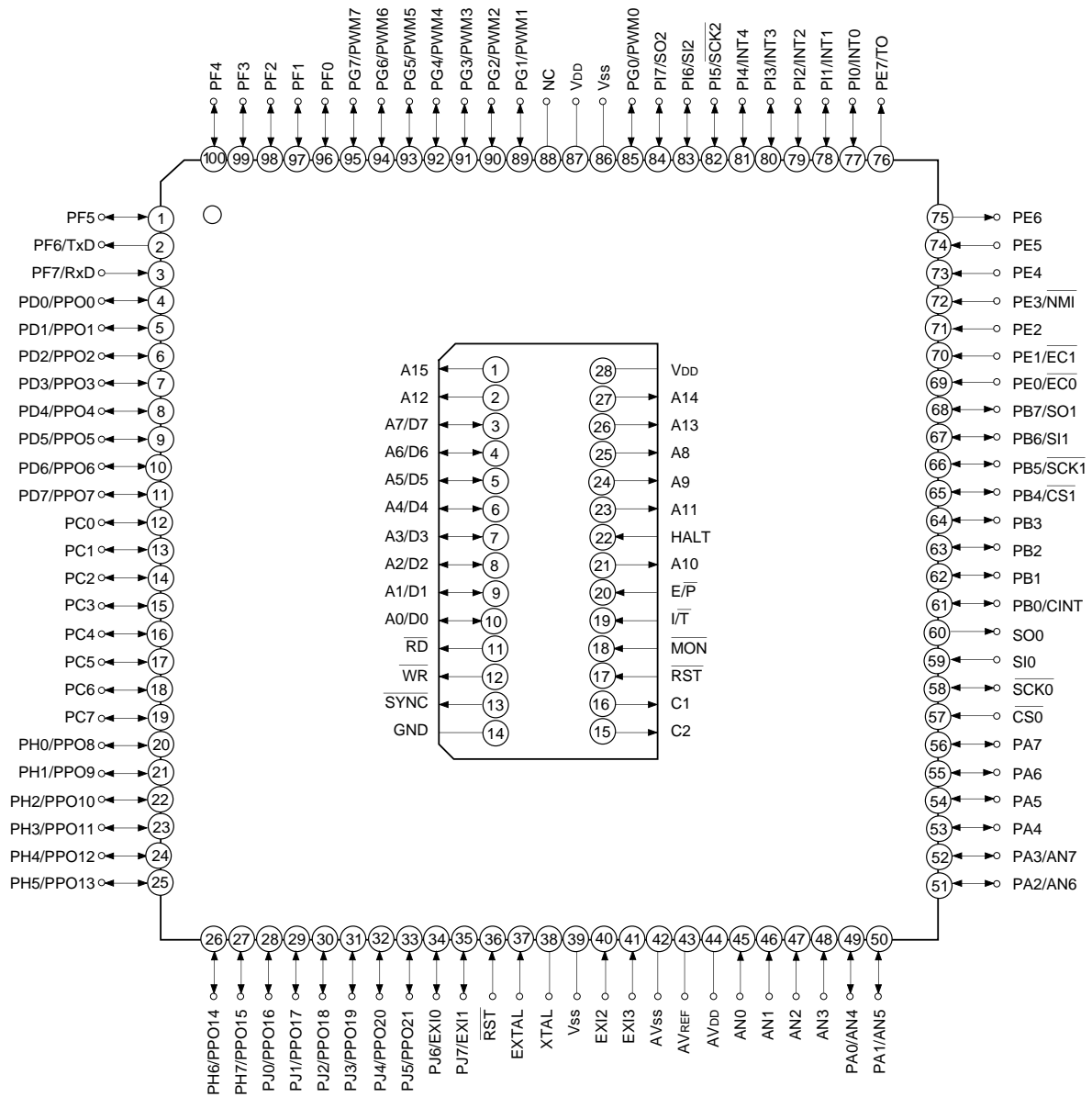
- Note)**
1. NC (Pin 88) is left open.
 2. V_{SS} (Pins 39 and 86) are both connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



- Note)** 1. NC (Pin 90) is left open.
 2. Vss (Pins 41 and 88) are both connected to GND.

Pin Assignment in Evaluator Mode (LQFP package)



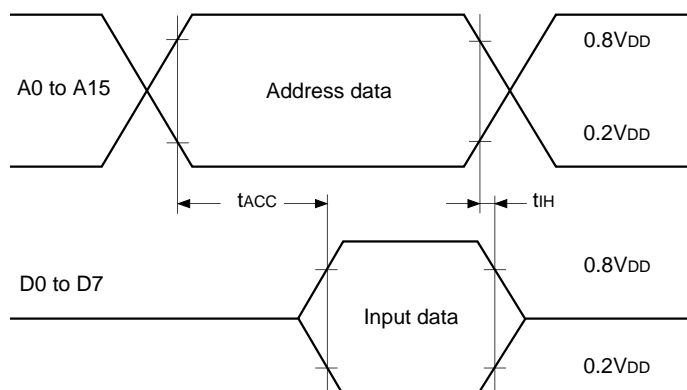
- Note)** 1. NC (Pin 88) is left open.
 2. Vss (Pins 39 and 86) are both connected to GND.

EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1	ns
				75*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

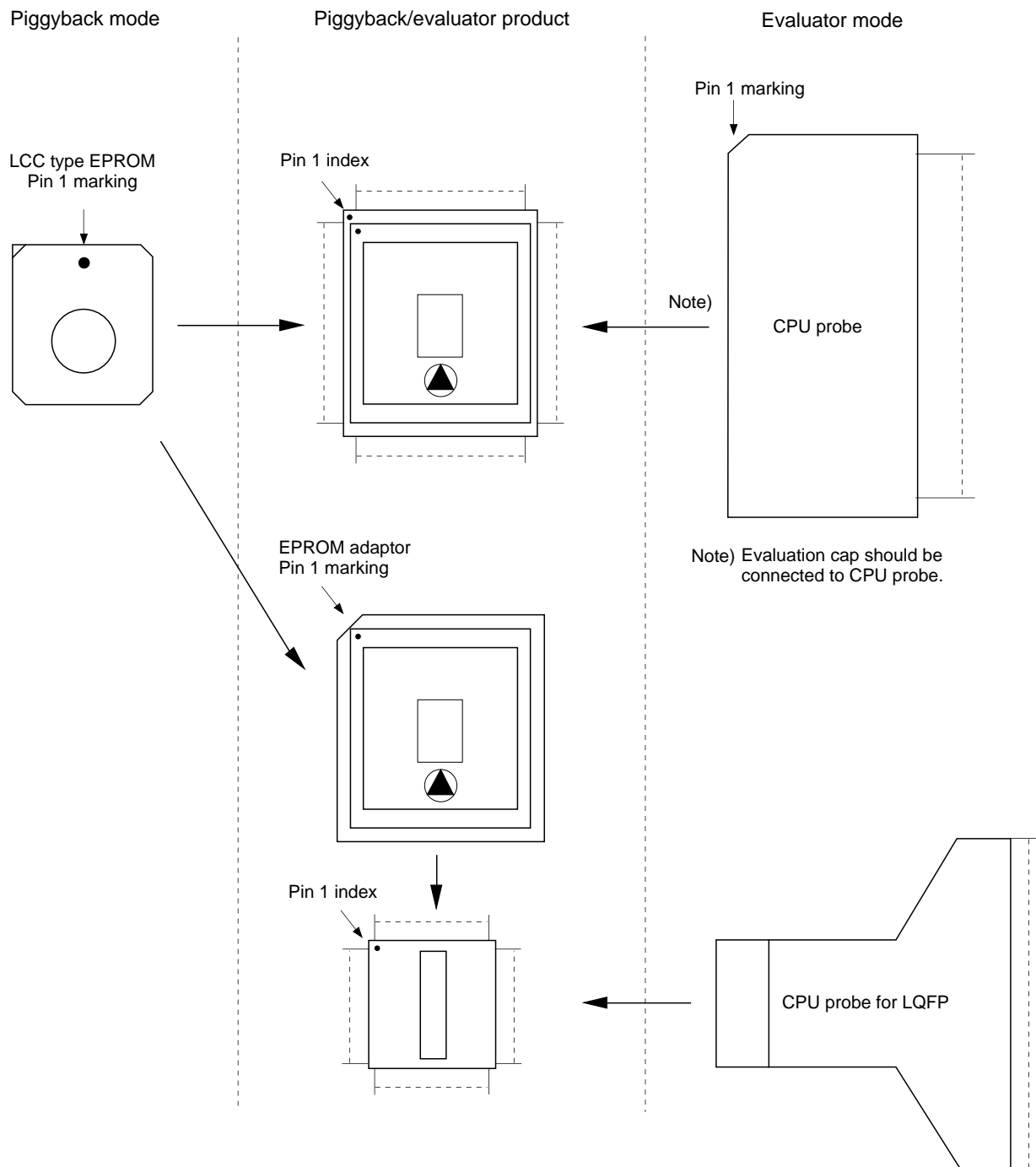
*2 At 12MHz operation ($V_{DD} = 3.0$ to 5.5V), at 16MHz operation ($V_{DD} = 4.5$ to 5.5V)



Products List

Option item	Products			
	Mask product			Piggyback/evaluator product
	CXP84716	CXP84720	CXP84724	
Package	100-pin plastic QFP/LQFP			100-pin ceramic PQFP
ROM capacity	16K bytes	20K bytes	24K bytes	EPROM 60K bytes
	27C512 × 1			
Pull-up resistor for reset pin	Existent/Non-existent			Existent
Power-on-reset circuit	Existent/Non-existent			Existent

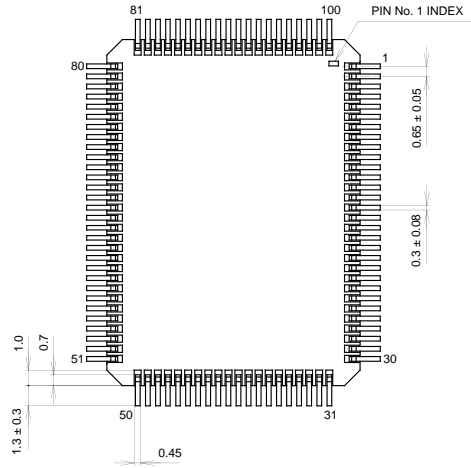
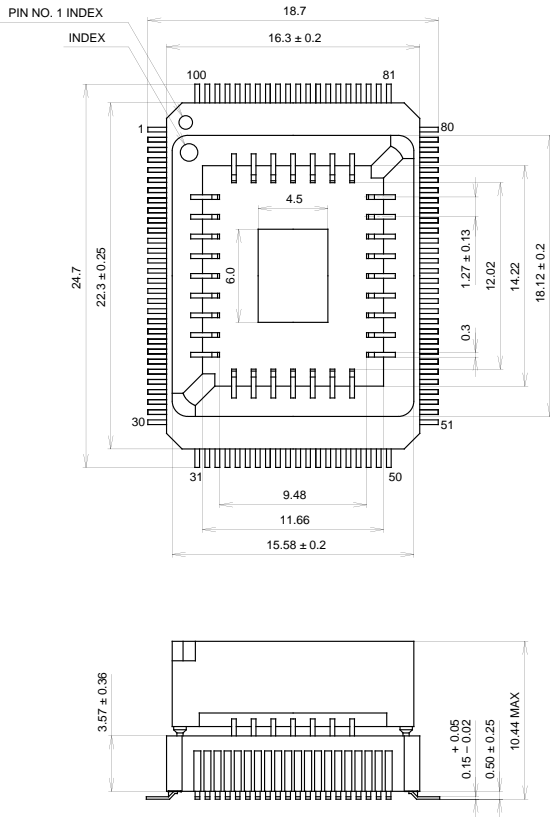
Piggyback mode/evaluator mode can be switched as shown below.



Package Outline

Unit: mm

100PIN PQFP (CERAMIC)

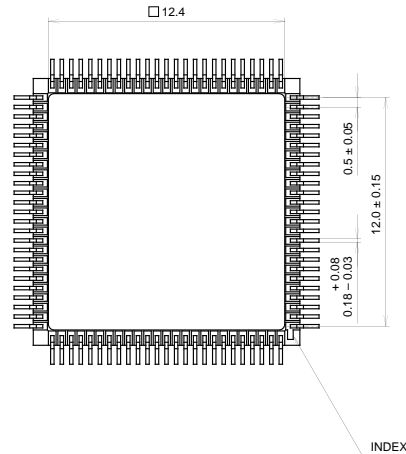
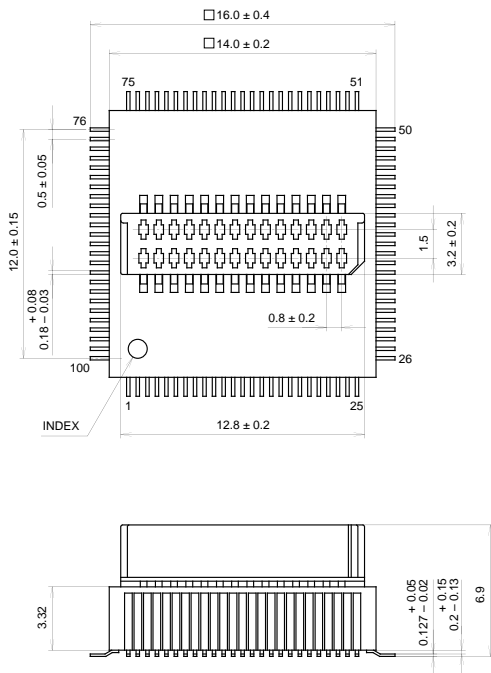


PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	-----

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	-----

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g