Chip Scale DDR Termination Array

Features

- 16 Integrated High frequency Series/Parallel Terminations
- Ultra small footprint Chip Scale Package
- Ceramic substrate
- 0.35mm Eutectic Solder Bumps, 0.65mm Pitch

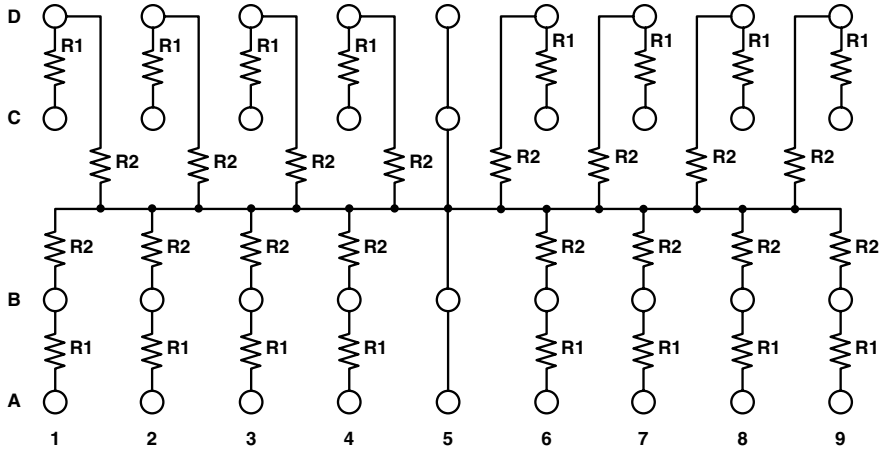
Applications

- DDR Memory bus termination
- SSTL Termination

Product Description

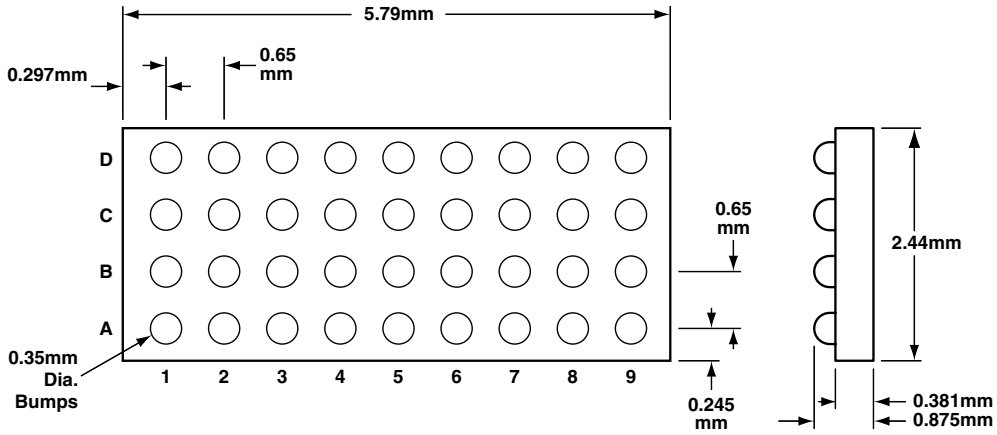
The CSPDDR100 is a high performance Integrated Passive Device (IPD) which provides Series/Parallel terminations suitable for use in SSTL and DDR termination applications. Sixteen (16) Series/Parallel termination channels are provided for a total of 32 integrated resistors. These resistors provide excellent high frequency performance in excess of 3GHz and are manufactured to an absolute tolerance of ±1%. The Chip Scale Package provides an ultra small footprint for this Integrated Passive Device and provides minimal parasitics compared to conventional packaging. Typical bump inductance is less than 25pH. The large solder bumps and ceramic substrate allow for standard attachment to laminate printed circuit boards without the use of underfill. The 4X9 Bump pattern is arranged for easy flow through routing on the pcb.

SCHEMATIC DIAGRAM



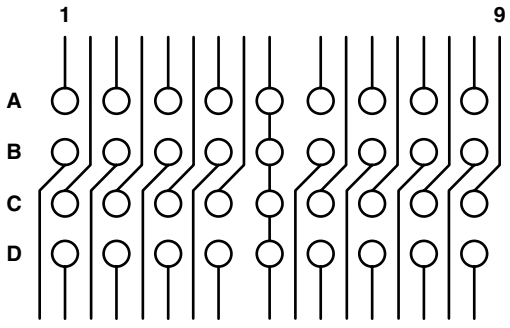
STANDARD PART ORDERING INFORMATION			
Package		Ordering Part Number	
Style	Bumps	Tape & Reel	Part Marking
Chip Scale	36	CSPDDR100	Ink dot to mark bump A1

Package Diagram (Bumps Up View)



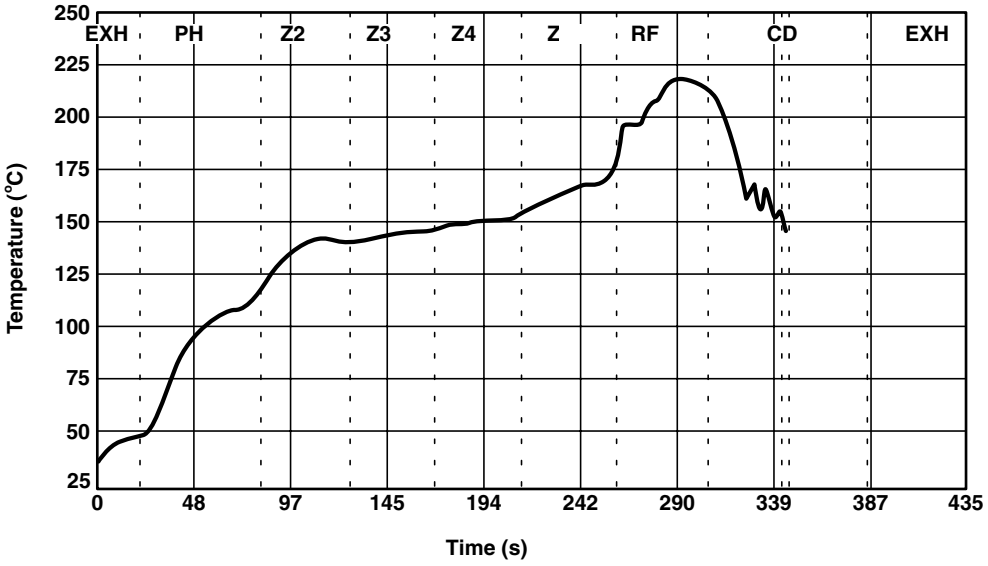
PRINTED CIRCUIT BOARD RECOMMENDATIONS	
Pad Size on PCB	0.300mm
Pad Shape	Round
Pad Definition	Non Solder Mask Defined Pads (NSMD)
Solder Mask Opening	0.350mm
Solder Stencil Thickness	0.152mm
Solder Stencil Aperture Opening	0.360mm (sq.)
Solder Flux Ratio	50/50
Solder Paste	No Clean
Bond Trace Finish	OSP (Entek Cu Plus 106A)

Typical PCB Routing Diagram (Bumps Down View)



Resistor Values (Ω)		
R1(Ω)	R2(Ω)	Code
25	50	100

STANDARD VALUES	
Resistor Value	R1 = 25Ω, R2 = 50Ω,
Absolute Tolerance R	±1%
TCR of Resistors	±100ppm
Power Rating/Resistor	100mW
Operating Temperature Range	–40°C to 85°C



Typical Solder Reflow Thermal Profile (No Clean Flux)

PART NUMBER KEY

CSP DDR 100

PACKAGE TYPE

CSP = Chip Scale Package

APPLICATION

DDR = Double Data Rate Memory Termination

Resistor Value Code

100 = R_1 25Ω; R_2 50Ω

Applications

The CSPDDR100, Chip Scale DDR Termination Array, provides sixteen (16) channels of series/parallel termination for SSTL termination applications such as DDR memory systems. SSTL is the bus standard for DDR SDRAM systems. Applying terminating resistors to DDR SDRAM's interconnections is a necessity to avoid signal integrity problems in the memory system's operation. Improper or no termination on an interconnection that is a transmission line will cause reflections which in turn will affect the performance of the system due to ringing, delays, exceeding IC voltage specifications, or crosstalk. [1]

SSTL has four possible configurations. One of them calls for both a series termination resistor and a parallel termination at one end of the bus, as shown in Figure 1. This is the application that the CSPDDR100 satisfies.

When a full level signal is sent down the transmission line and no reflection is desired, the parallel load resistance should equal the characteristic impedance (Z_0) of the transmission line. When a less than full level signal is sent down a transmission line, it is desirable to have an intentional mismatch of the parallel termination load resistor so that the higher level reflection voltage (resulting from having $R_T > Z_0$) raises the signal to the full signal level so that load switching occurs in only one propagation delay time. The use of a series termination resistor at the source enables the sending of a reduced level signal on the first incident wave. A reduced level signal is beneficial in reducing rise times and EMI.

The values of the resistors for DDR/SSTL terminations are user determined. If values different from the ones in the CSPDDR100 specification are desired, please contact California Micro Devices for quotations on other values.

[1] James Sutherland, "Understanding Transmission Lines, and High Speed Terminations", EDN, October 9, 1999

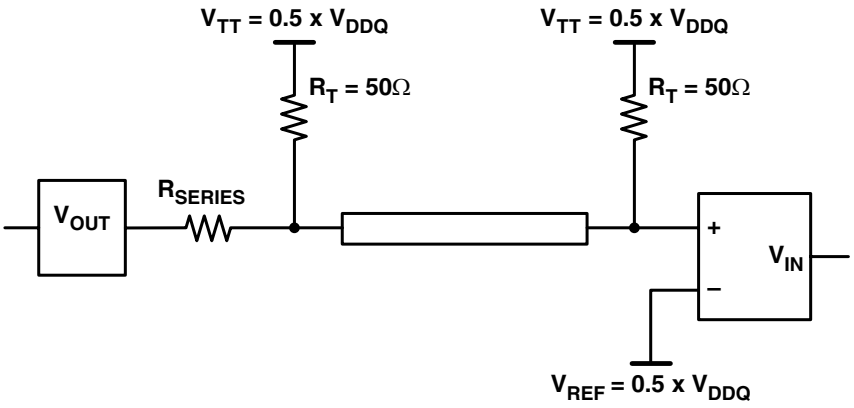


Figure 1. SSTL_2 Class II,
Symmetrically Double Parallel Terminated Output Load with Series Resistor