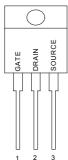


GENERAL DESCRIPTION

This Power MOSFET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

PIN CONFIGURATION

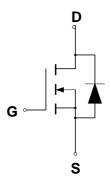




FEATURES

- Dynamic dv/dt Rating
- ◆ Repetitive Avalanche Rated
- ◆ Fast Switching
- ◆ Ease of Paralleling
- Simple Drive Requirements

SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT09N20N220	TO-220

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current — Continuous		9.0	Α
─ Pulsed (Note 1)	I _{DM}	36	
Gate-to-Source Voltage — Continue	V_{GS}	±20	V
Total Power Dissipation	P _D	74	W
Derate above 25℃		0.59	W/°C
Single Pulse Avalanche Energy (Note 2)	E _{AS}	56	mJ
Avalanche Current (Note 1)	I _{AR}	9.0	Α
Repetitive Avalanche Energy (Note 1)	E _{AR}	7.4	mJ
Peak Diode Recovery dv/dt	dv/dt	5.0	V/ns
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to 150	$^{\circ}\mathbb{C}$
Thermal Resistance — Junction to Case	θ_{JC}	1.70	°CW
 Junction to Ambient 	θ_{JA}	62	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	300	$^{\circ}\!\mathbb{C}$



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^{\circ}C$.

			CMT09N20			
Characteristic		Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	200			V
$(V_{GS} = 0 \text{ V}, I_D = 250 \ \mu \text{ A})$						
Drain-Source Leakage Current		I _{DSS}				μ A
(V _{DS} = 200V, V _{GS} = 0 V)					25	
(V _{DS} = 160V, V _{GS} = 0 V, T _J = 125°C)					250	
Gate-Source Leakage Current-Forward		I_{GSSF}			100	nA
$(V_{gsf} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate-Source Leakage Current-Reverse		I_{GSSR}			-100	nA
$(V_{gsr} = -20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage		$V_{GS(th)}$	2.0		4.0	V
$(V_{DS} = V_{GS}, I_{D} = 250 \ \mu A)$						
Static Drain-Source On-Resistance (\	$I_{GS} = 10 \text{ V}, I_D = 5.4 \text{A}) \text{ (Note 4)}$	R _{DS(on)}			0.40	Ω
Forward Transconductance (V _{DS} = 50	IV, I _D = 5.4 A) (Note 4)	g FS	3.8			mhos
Input Capacitance	()/ - 25 \/ \/ - 0 \/	C_{iss}		800		pF
Output Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz)	C_{oss}		240		pF
Reverse Transfer Capacitance	1 = 1.0 WH2)	C_{rss}		76		pF
Turn-On Delay Time		$t_{d(on)}$		9.4		ns
Rise Time	$(V_{DD} = 100 \text{ V}, I_D = 5.9 \text{ A},$	t _r		28		ns
Turn-Off Delay Time	$R_G = 12\Omega, R_D = 16\Omega)$ (Note 4)	$t_{d(off)}$		39		ns
Fall Time		t _f		20		ns
Total Gate Charge	(V _{DS} = 160V, I _D = 5.9A V _{GS} = 10 V) (Note 4)	Q_g			43	nC
Gate-Source Charge		Q_{gs}			7.0	nC
Gate-Drain Charge		Q_{gd}			23	nC
Internal Drain Inductance		L_D		4.5		nH
(Measured from the drain lead 0.25	" from package to center of die)					
Internal Drain Inductance		Ls		7.5		nH
(Measured from the source lead 0.25" from package to source bond pad)						
SOURCE-DRAIN DIODE CHARACT	ERISTICS					
Reverse Recovery Charge	I _F = 5.9A, di/dt = 100A/μs , T _J = 25°C (Note 4)	Q _{rr}		1.1	2.2	μC
Forward Turn-On Time		t _{on}		**		
Reverse Recovery Time		t _{rr}		170	340	ns
Diode Forward Voltage	$I_S = 9.0A$, $V_{GS} = 0 \text{ V}$, $T_J = 25^{\circ}$ C (Note 4)	V _{SD}			1.5	V

Note

- (1) Repetitive rating; pulse width limited by max. junction temperature
- (2) V_{DD} = 100V, V_{GS} = 10V , starting T_J = 25 $^{\circ}$ C, L=1.38mH, R_G = 25 Ω , I_{AS} = 9.0A
- (3) $I_{SD} \leq$ 9.0A, di/dt \leq 120A/ μ s, $V_{DD} \leq$ $V_{(BR)DSS}$, $T_{J} \leq$ 150 $^{\circ}$ C
- (4) Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%
- ** Negligible, Dominated by circuit inductance



TYPICAL ELECTRICAL CHARACTERISTICS

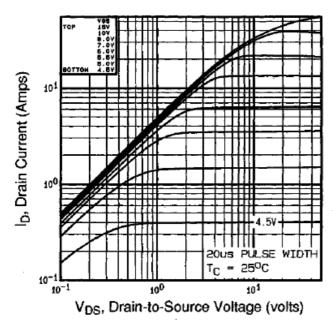


Fig 1. Typical Output Characteristics, Tc=25°C

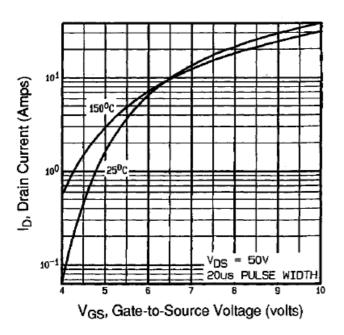


Fig 3. Typical Transfer Characteristics

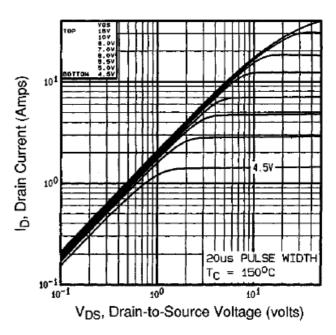


Fig 2. Typical Output Characteristics, Tc=150°C

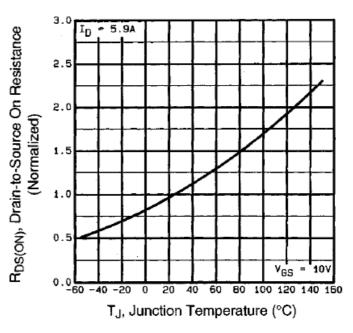


Fig 4. Normalized On-Resistance Vs. Temperature



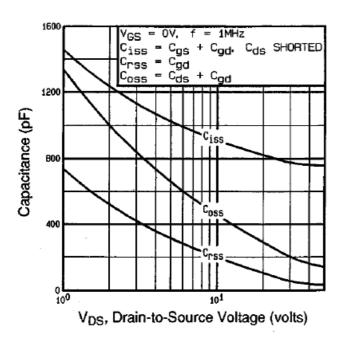


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

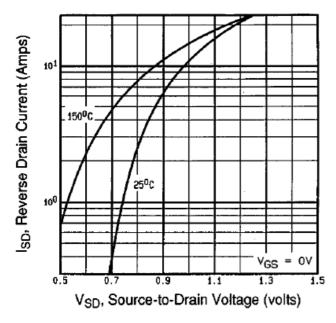


Fig 7. Typical Source-Drain Diode Forward Voltage

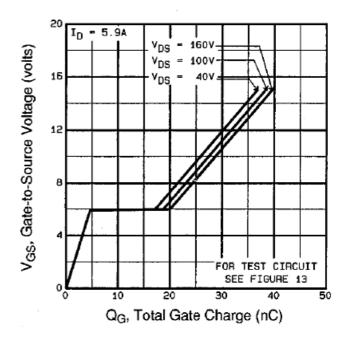


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

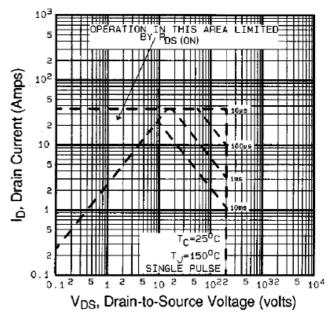


Fig 8. Maximum Safe Operating Area



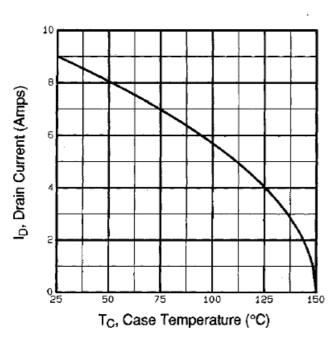


Fig 9. Maximum Drain Current Vs. Case Temperature

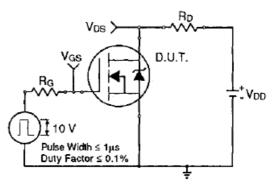


Fig 10a. Switching Time Test Circuit

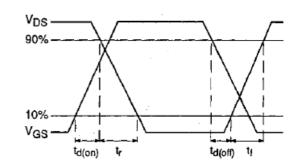


Fig 10b. Switching Time Waveforms

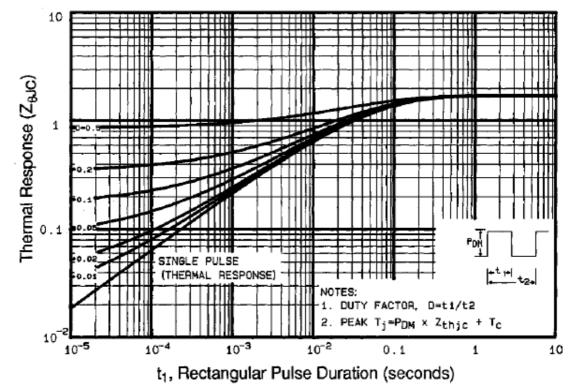


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



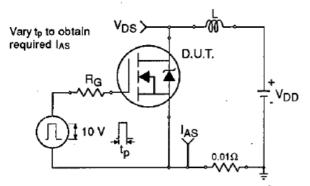


Fig 12a. Unclamped Inductive Test Circuit

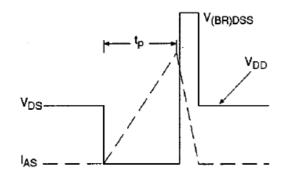


Fig 12b. Unclamped Inductive Waveforms

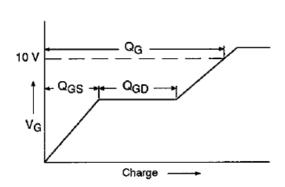


Fig 13a. Basic Gate Charge Waveform

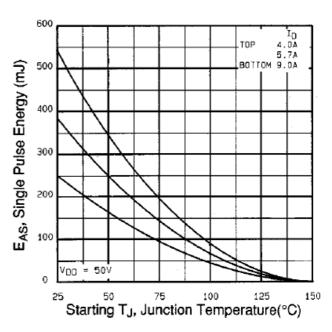


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

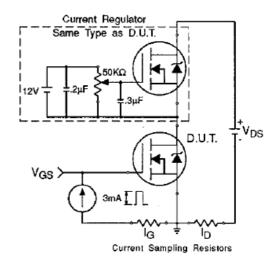
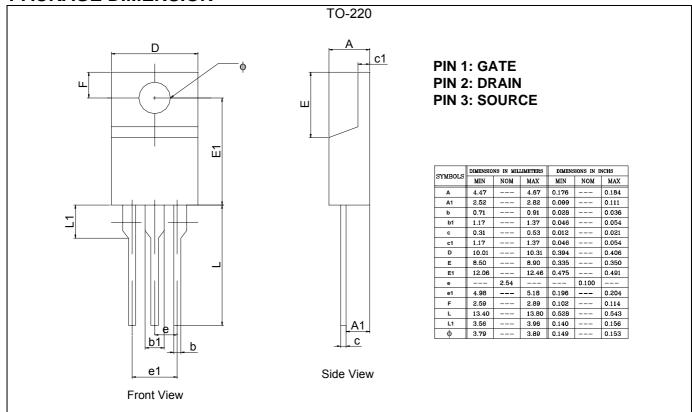


Fig 13b. Gate Charge Test Circuit



PACKAGE DIMENSION





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