6- and 8-Channel Low Capacitance ESD Arrays

Features

- 6 and 8 channels of ESD protection
- Provides ±15 kV ESD protection on each channel per the IEC 61000-4-2 ESD requirements
- Channel loading capacitance of 1.6 pF typical
- Channel I/O to GND capacitance difference of 0.04pF typical
- Mutual capacitance of 0.13pF typical
- Minimal capacitance change with temperature and voltage
- Each I/O pin can withstand over 1000 ESD strikes
- SOIC and MSOP packages
- Lead-free versions available

Applications

- IEEE1394 Firewire® ports at 400Mbps / 800Mbps
- DVI ports, HDMI ports in notebooks, set top boxes, digital TVs, LCD displays
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- General purpose high-speed data line ESD protection

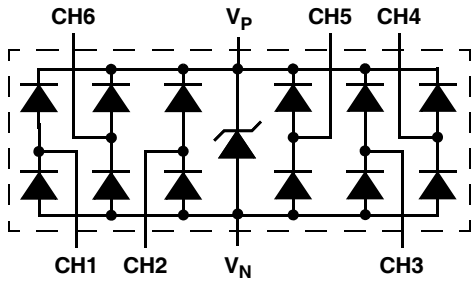
Product Description

The CM1216 family of diode arrays has been designed to provide ESD protection for electronic components or sub-systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. The CM1216 will protect against ESD pulses up to ±15kV per the IEC 61000-4-2 standard.

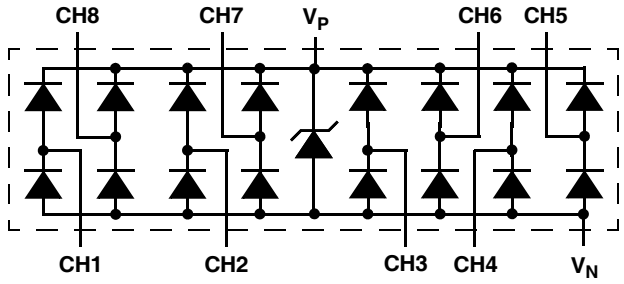
This device is particularly well-suited for protecting systems using high-speed ports such as USB2.0, IEEE1394 (Firewire®, iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

The CM1216 family of devices is available with optional lead-free finishing.

Simplified Electrical Schematic

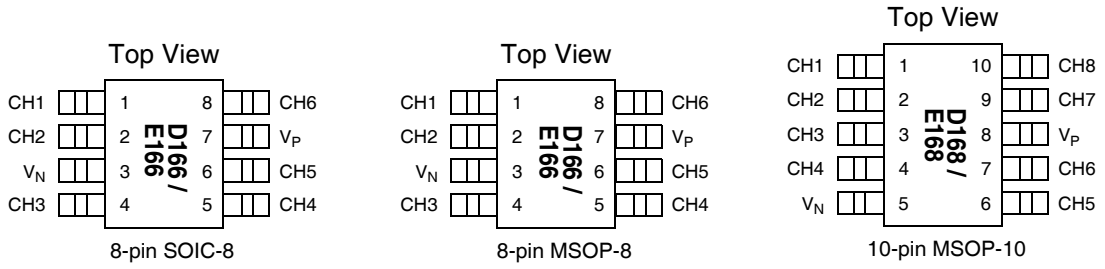


CM1216-06MS/MR
CM1216-06SN/SM



CM1216-08MS/MR

PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale.

Pin Configuration

PIN NAME	MSOP-8 PIN NO.	SOIC-8 PIN NO.	MSOP-10 PIN NO.	TYPE	DESCRIPTION
CH1	**1**	**1**	**1**	**I/O**	**ESD Channel**
CH2	**2**	**2**	**2**	**I/O**	**ESD Channel**
CH3	**4**	**4**	**3**	**I/O**	**ESD Channel**
CH4	**5**	**5**	**4**	**I/O**	**ESD Channel**
V_N	3	3	**5**	**GND**	**Negative voltage supply rail**
CH5	**6**	**6**	**6**	**I/O**	**ESD Channel**
CH6	**8**	**8**	**7**	**I/O**	**ESD Channel**
V_P	7	7	**8**	**PWR**	**Positive voltage supply rail**
CH7	–	–	**9**	**I/O**	**ESD Channel**
CH8	–	–	**10**	**I/O**	**ESD Channel**

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Standard Finish		Lead-free Finish	
		Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
8	SOIC	CM1216-06SN	D166	CM1216-06SM	E166
8	MSOP	CM1216-06MS	D166	CM1216-06MR	E166
10	MSOP	CM1216-08MS	D168	CM1216-08MR	E168

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Operating Supply Voltage (V_P-V_N)	6	V
Diode Forward DC Current (Note 1)	20	mA
DC Voltage at any Channel Input	(V_N-0.5) to (V_P+0.5)	V
Operating Temperature Range		
Ambient	-40 to +85	°C
Junction	-40 to +125	°C
Storage Temperature Range	-40 to +150	°C

Standard Operating Condition

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Temperature Range (Ambient)	-40 to +85	°C
Package Power Rating		
MSOP8 Package (CM1216-06MS/MR)	400	mW
SOIC8 Package (CM1216-06SN/SM)	600	mW
MSOP10 Package (CM1216-08MS/MR)	400	mW

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS NOTE 1						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_P	Operating Supply Voltage (V_P-V_N)			3.3	5.5	V
I_P	Operating Supply Current	(V_P-V_N) = 3.3V			8	µA
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 20mA; T_A=25°C	 0.6 0.6	 0.8 0.8	 0.95 0.95	 V V
I_{LEAK}	Channel Leakage Current	T_A = 25°C; V_P= 5V, V_N = 0V		±0.1	±1.0	µA
C_{IN}	Channel Input Capacitance	At 1 MHz, V_P=3.3V, V_N =0V, V_{IN}=1.65V;Note2		1.6	2.0	pF
ΔC_{IN}	Channel Input Capacitance Matching	Note 2		0.04		pF
C_{MUTUAL}	Mutual Capacitance	(V_P-V_N) = 3.3V; Note 2		0.13		pF
V_{ESD}	ESD Protection Peak Discharge Voltage at any channel input, in system, contact discharge per IEC 61000-4-2 standard	Notes 2, 3, and 4; T_A = 25°C	±15			kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	I_{PP} = 1A, t_P = 8/20µS; T_A=25°C; Notes 2		 +9.0 -1.5		 V V
R_{DYN}	Dynamic Resistance Positive transients Negative transients	I_{PP} = 1A, t_P = 8/20µS; T_A=25°C; Notes 2		 0.6 0.4		 Ω Ω

Note 1: All parameters specified at T_A = -40°C to +85°C unless otherwise noted.

Note 2: These parameters guaranteed by design and characterization.

Note 3: Standard IEC 61000-4-2 with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω, V_P = 3.3V, V_N grounded.

Note 4: From I/O pins to V_P or V_N only. V_P bypassed to V_N with low ESR 0.2µF ceramic capacitor.

Performance Characteristics

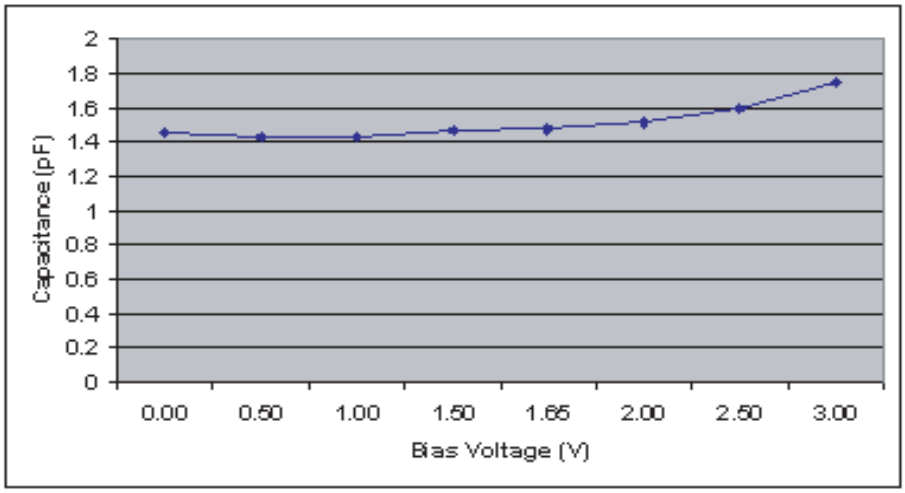


Figure 1. Typical Variation of C_{IN} vs. V_{IN}
(f = 1MHz, V_P= 3.3V, V_N = 0V, 0.1μF chip capacitor between V_P and V_N, T_A = 25°C)

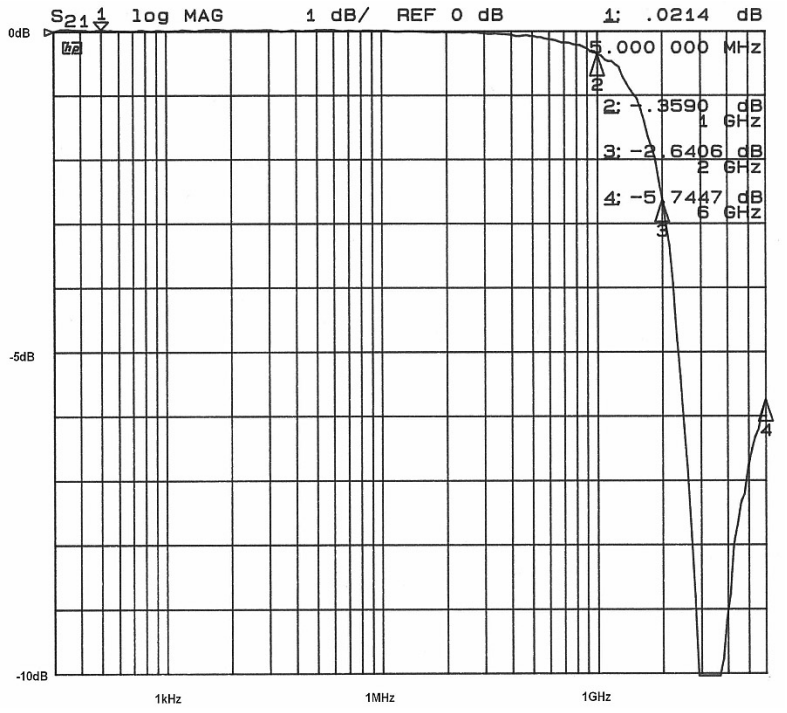


Figure 2. Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment

APPLICATION INFORMATION

Design Considerations

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and the ESD protection device. Refer to Figure 1, which illustrates an example of a positive ESD pulse striking an input channel. The parasitic series inductance back to the power supply is represented by L1 and L2. The voltage VCL on the line being protected is:

$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L1 \times d(I_{ESD}) / dt + L2 \times d(IESD) / dt$$

where IESD is the ESD current pulse, and VSUPPLY is the positive supply voltage.

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1ns. Here d(IESD)/dt can be approximated by $d(_{ESD})/dt$, or 30/(1x10-9). So just 10nH of series inductance (L1 and L2 combined) will lead to a 300V increment in VCL!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply, ground planes and between the signal input and the ESD device to minimize stray series inductance.

Additional Information

See also California Micro Devices Application Note AP-209, “Design Considerations for ESD Protection”, in the Applications section at www.calmicro.com.

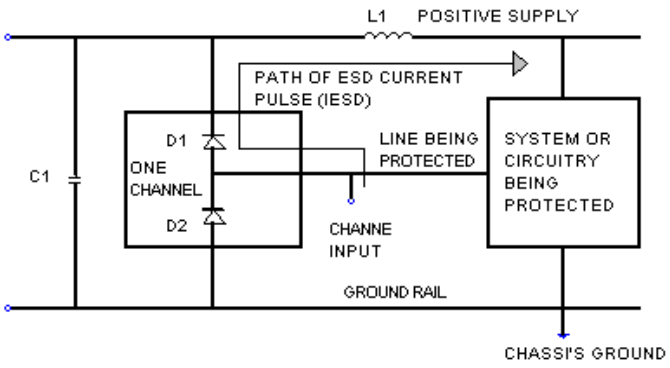


Figure 3. Application of Positive ESD Pulse between Input Channel and Ground

Mechanical Details

The CM1216 is supplied in SOIC-8, MSOP-8 and MSOP-10 packages with a lead-free finishing option. These package drawings are presented on the follow pages.

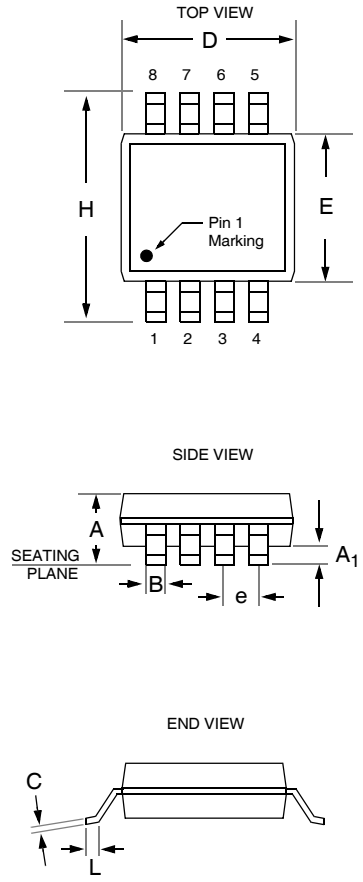
SOIC-8 Mechanical Specifications

CM1216-06SN/SM devices are supplied in 8-pin SOIC packages. Dimensions are presented below.

For complete information on the SOIC-8 package, see the California Micro Devices SOIC Package Information document.

PACKAGE DIMENSIONS				
Package	SOIC			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.19	0.150	0.165
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
# per tape and reel	2500 pieces			
Controlling dimension: inches				

Mechanical Package Diagrams



Package Dimensions for SOIC-8

Mechanical Details

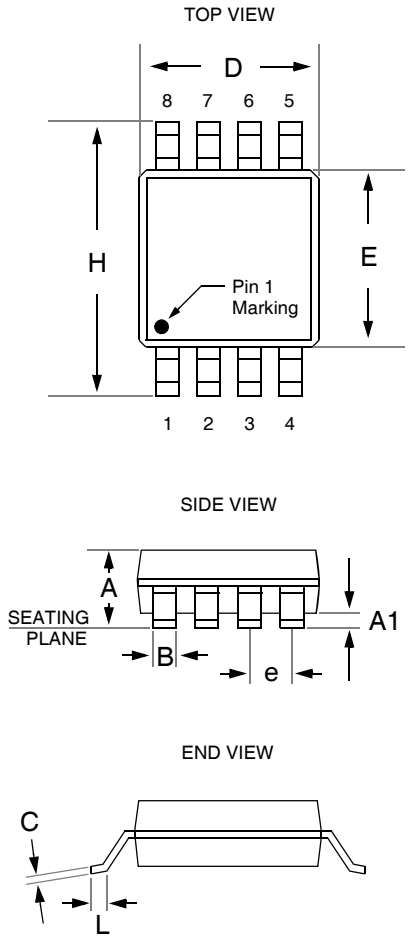
MSOP-8 Mechanical Specifications:

CM1216-06MS/MR devices are supplied in 8-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-8 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	8			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.87	1.17	0.034	0.046
A1	0.05	0.25	0.002	0.010
B	0.30 (typ)		0.012 (typ)	
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.65 BSC		0.025 BSC	
H	4.78	4.98	0.188	0.196
L	0.43	0.64	0.017	0.025
# per tape and reel	4000 pieces			
Controlling dimension: inches				

Mechanical Package Diagrams



Package Dimensions for MSOP-8

Mechanical Details (cont'd)

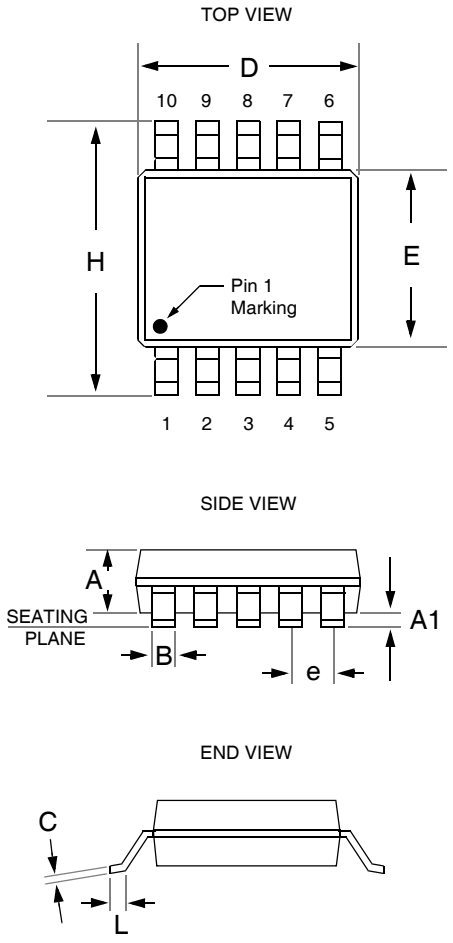
MSOP-10 Mechanical Specifications

CM1216-08MS/MR devices are supplied in 10-pin MSOP packages. Dimensions are presented below.

For complete information on the MSOP-10 package, see the California Micro Devices MSOP Package Information document.

PACKAGE DIMENSIONS				
Package	MSOP			
Pins	10			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	0.75	0.95	0.028	0.038
A1	0.05	0.15	0.002	0.006
B	0.18	0.40	0.006	0.016
C	0.18		0.007	
D	2.90	3.10	0.114	0.122
E	2.90	3.10	0.114	0.122
e	0.50 BSC		0.0196 BSC	
H	4.76	5.00	0.187	0.197
L	0.40	0.70	0.0137	0.029
# per tape and reel	4000			
Controlling dimension: inches				

Mechanical Package Diagrams



Package Dimensions for MSOP-10