

#### **GENERAL DESCRIPTION**

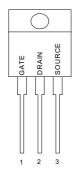
This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

## **FEATURES**

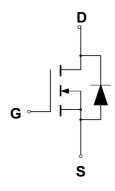
- Robust High Voltage Termination
- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- ♦ I<sub>DSS</sub> and V<sub>DS</sub>(on) Specified at Elevated Temperature

## PIN CONFIGURATION

TO-220 Front View



#### **SYMBOL**



N-Channel MOSFET

# **ABSOLUTE MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Drain to Current — Continuous		2.0	Α
<ul><li>Pulsed</li></ul>	I <sub>DM</sub>	9.0	
Gate-to-Source Voltage — Continue	$V_{GS}$	±20	V
<ul> <li>Non-repetitive</li> </ul>	$V_{GSM}$	±40	V
Total Power Dissipation	P <sub>D</sub>	50	W
Derate above 25℃		0.4	W/°C
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy $-T_J$ = 25 $^{\circ}$ C	E <sub>AS</sub>	190	mJ
$(V_{DD} = 100V, V_{GS} = 10V, I_L = 20A, L = 10mH, R_G = 25\Omega)$			
Thermal Resistance — Junction to Case	$\theta_{JC}$	1.0	°C/W
<ul> <li>Junction to Ambient</li> </ul>	$\theta_{JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	$^{\circ}\!\mathbb{C}$



## **ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $T_J = 25^{\circ}C$ .

Cha	racteristic	Symbol	Min	Тур	Max	Units
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	600			V
$(V_{GS} = 0 \text{ V}, I_D = 250 \ \mu \text{ A})$						
Drain-Source Leakage Current		I <sub>DSS</sub>				mA
$(V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V})$					0.25	
$(V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 125^{\circ}\text{C})$					1.0	
Gate-Source Leakage Current-Forward		I <sub>GSSF</sub>			100	nA
$(V_{gsf} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate-Source Leakage Current-Reverse		I <sub>GSSR</sub>			100	nA
$(V_{gsr} = 20 \text{ V}, V_{DS} = 0 \text{ V})$						
Gate Threshold Voltage	e Threshold Voltage		2.0	3.1	4.0	V
$(V_{DS} = V_{GS}, I_D = 250 \ \mu A)$						
Static Drain-Source On-Resistance (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0A) *		R <sub>DS(on)</sub>		3.3	3.8	Ω
Drain-Source On-Voltage (V <sub>GS</sub> = 10 \	/)	V <sub>DS(on)</sub>			8.2	V
$(I_D = 2.0 \text{ A})$						
Forward Transconductance ( $V_{DS} \ge$	50 V, I <sub>D</sub> = 1.0A) *	<b>g</b> FS	1.0			S
Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0  MHz)	C <sub>iss</sub>		435		pF
Output Capacitance		C <sub>oss</sub>		56		pF
Reverse Transfer Capacitance		$C_{rss}$		9.2		pF
Turn-On Delay Time	$(V_{DD} = 300 \text{ V}, I_D = 2.0 \text{ A},$ $V_{GS} = 10 \text{ V},$ $R_G = 18\Omega) *$	t <sub>d(on)</sub>		12		ns
Rise Time		t <sub>r</sub>		21		ns
Turn-Off Delay Time		$t_{d(off)}$		30		ns
Fall Time		t <sub>f</sub>		24		ns
Total Gate Charge	$(V_{DS} = 400 \text{ V}, I_{D} = 2.0 \text{ A},$ $V_{GS} = 10 \text{ V})^*$	$Q_g$		13	22	nC
Gate-Source Charge		$Q_{gs}$		2.0		nC
Gate-Drain Charge		$Q_{gd}$		6.0		nC
Internal Drain Inductance		L <sub>D</sub>		4.5		nΗ
(Measured from the drain lead 0.2	5" from package to center of die)					
Internal Drain Inductance		Ls		7.5		nH
(Measured from the source lead 0.	25" from package to source bond pad)					
SOURCE-DRAIN DIODE CHARACT	ERISTICS					
Forward On-Voltage(1)	$(I_S = 2.0 \text{ A}, V_{GS} = 0 \text{ V},$	V <sub>SD</sub>		1.0	1.6	V
Forward Turn-On Time		t <sub>on</sub>		**		ns
Reverse Recovery Time	$d_{lS}/d_t = 100A/\mu s)$	t <sub>rr</sub>		340		ns

<sup>\*</sup> Pulse Test: Pulse Width  $\leq$ 300 $\mu$ s, Duty Cycle  $\leq$ 2%

<sup>\*\*</sup> Negligible, Dominated by circuit inductance



## TYPICAL ELECTRICAL CHARACTERISTICS

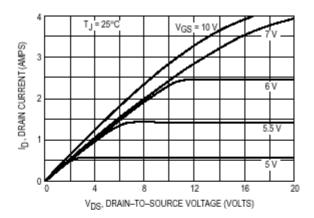


Figure 1. On-Region Characteristics

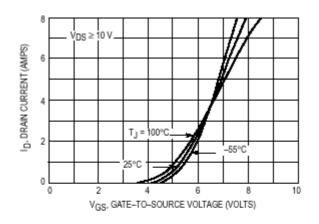


Figure 2. Transfer Characteristics

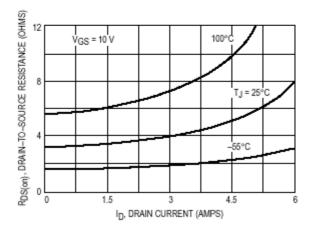


Figure 3. On–Resistance versus Drain Current and Temperature

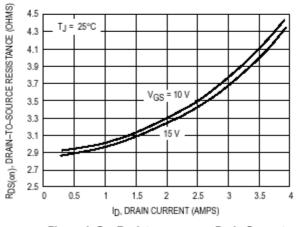


Figure 4. On–Resistance versus Drain Current and Gate Voltage

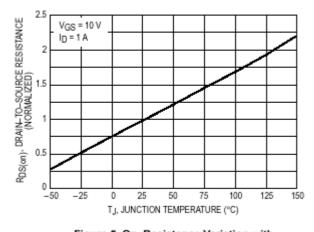


Figure 5. On–Resistance Variation with Temperature

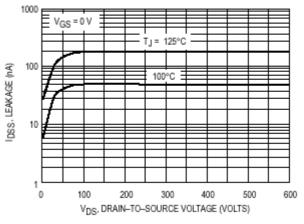


Figure 6. Drain-To-Source Leakage Current versus Voltage