

Process C3015 CMOS 3μm Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT _N	0.6	0.8	1.0	V	100x3μm
Body Factor	γ_{N}		0.6		V1/2	100x3μm
Conduction Factor	βN	42	47	52	μA/V ²	100x100μm
Effective Channel Length	Leff _N	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_N		0.7		μm	Per side
Punch Through Voltage	BVDSS _N	12			V	
Poly Field Threshold Voltage	VTF _{P(N)}	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT _P	-0.6	-0.8	-1.0	V	100x3μm
Body Factor	γ_{P}		0.55		V1/2	100x3μm
Conduction Factor	βР	13	15	19	μ A/V ²	100x100μm
Effective Channel Length	Leff _P	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_P		0.9		μm	Per side
Punch Through Voltage	BVDSS _P	-12			V	
Poly Field Threshold Voltage	VTF _{P(P)}	-12			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{\text{P-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/\square	
N+ Junction Depth	X _{jN+}		0.8		μm	
P+ Sheet Resistance	ρ _{P+}	50	80	100	Ω/\square	
P+ Junction Depth	X _{jP+}		0.7		μm	
Gate Oxide Thickness	T _{GOX}	37.5	40.0	42.5	nm	
Gate Poly Sheet Resistance	ρ _{POLY1}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	$ ho_{M1}$		30	60	mΩ/□	
Passivation Thickness	T _{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	Cox	0.66	0.72	0.78	fF/μm²	
Metal-1 to Poly-1	См1Р		0.0523		fF/μm²	
Metal-1 to Silicon	C _{M1S}	0.026	0.030	0.034	fF/μm²	

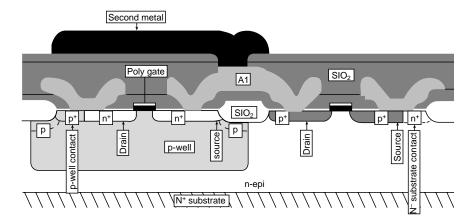
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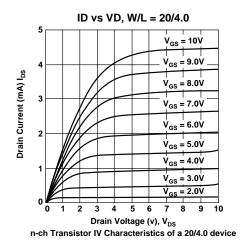
Physical Characteristics

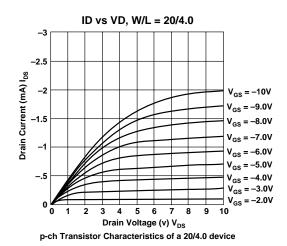
Starting Material	N <100>	N+/P+ Width/Space	3.0 / 3.0μm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12μm
Typ. Operating Voltage	5V	Contact To Poly Space	2.5μm
Well Type	P-well	Contact Overlap Of Diffusion	1.5μm
Metal Layers	1	Contact Overlap Of Poly	1.0μm
Poly Layers	1	Metal-1 Overlap Of Contact	1.0 μm
Contact Size	2.0x2.0μm	Minimum Pad Opening	100x100μm
Metal-1 Width/Space	3.5 / 2.5μm	Minimum Pad-to-Pad Spacing	5.0μm
Gate Poly Width/Space	3.0 / 2.5μm	Minimum Pad Pitch	80.0μm

Special Feature of C3015 Process: 3 μm P-well digital process.



Cross-sectional view of the C3015 process





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