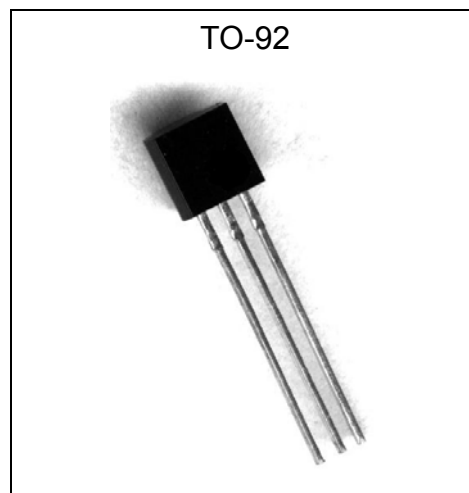
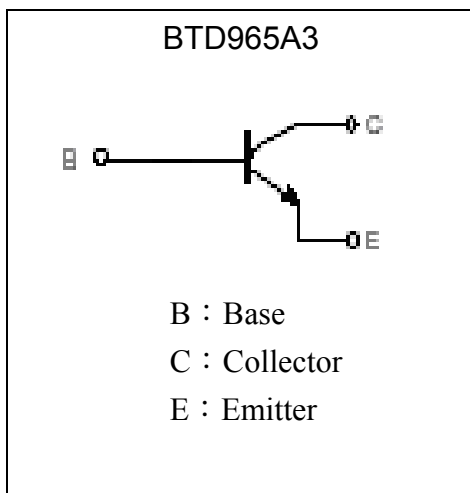


**Low Vcesat NPN Epitaxial Planar Transistor**

# BTD965A3

**Features**

- Low  $V_{CE(sat)}$ , Low  $V_{CE(sat)}=0.35\text{ V}$  (typical), at  $I_C / I_B = 3\text{A} / 0.1\text{A}$
- Excellent DC current gain characteristics
- Complementary to BTB1386A3

**Equivalent Circuit**

**Absolute Maximum Ratings** ( $T_a=25^\circ\text{C}$ )

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	VCBO	40	V
Collector-Emitter Voltage	VCEO	20	V
Emitter-Base Voltage	VEBO	7	V
Collector Current	$I_C$	5	A(DC)
	$I_C(\text{cp})$	8 * 1	A(Pulse)
Power Dissipation	$P_d$	0.75	W
Junction Temperature	$T_j$	150	$^\circ\text{C}$
Storage Temperature	$T_{\text{stg}}$	-55~+150	$^\circ\text{C}$

Note : \*1. Single Pulse  $P_w \leq 380\mu\text{s}$ , Duty  $\leq 2\%$ .



**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BVCEO	20	-	-	V	IC=1mA, IB=0
BVEBO	7	-	-	V	IE=10uA, IC=0
ICBO	-	-	0.1	uA	VCB=10V, IE=0
ICEO	-	-	1	uA	VCB=10V, IE=0
IEBO	-	-	0.1	uA	VEB=7V, IC=0
*VCE(sat)	-	0.35	1.0	V	IC=3A, IB=0.1A
*hFE1	230	-	800	-	VCE=2V, IC=500mA
*hFE2	150	-	-	-	VCE=2V, IC=2.00A
fT	-	150	-	MHz	VCE=6V, IE=50mA, f=200MHz
Cob	-	-	50	pF	VCB=20V, IE=0A, f=1MHz

\*Pulse Test : Pulse Width ≤380us, Duty Cycle≤2%

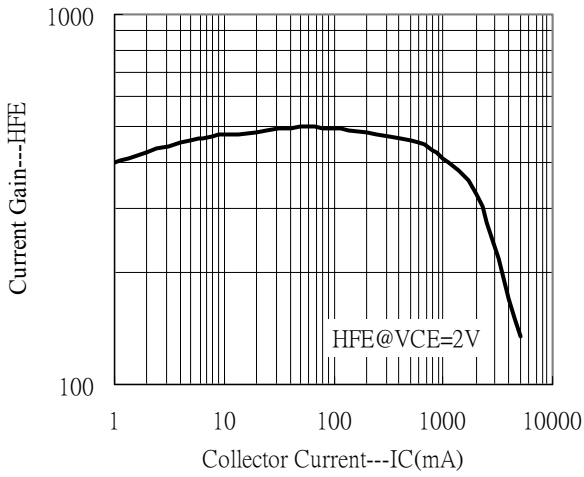
**Classification Of hFE1**

Rank	Q	R	S
Range	230~380	340~600	400~800

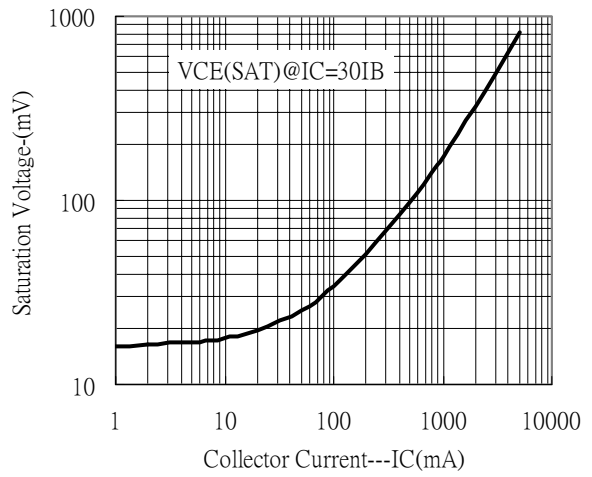


### Characteristic Curves

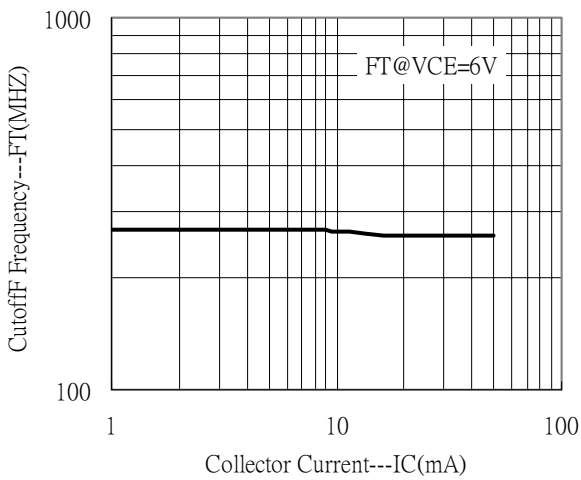
Current Gain vs Collector Current



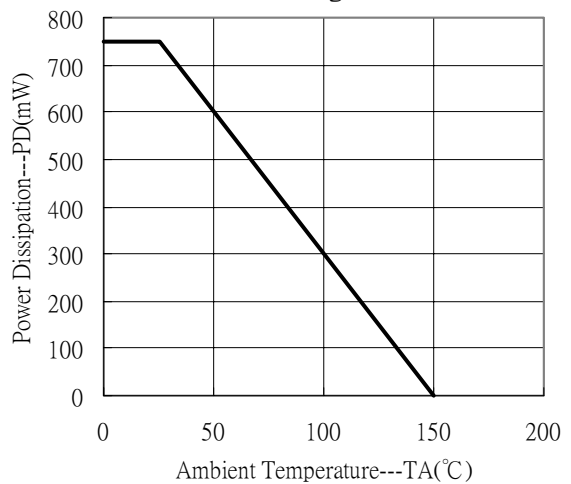
Saturation Voltage vs Collector Current



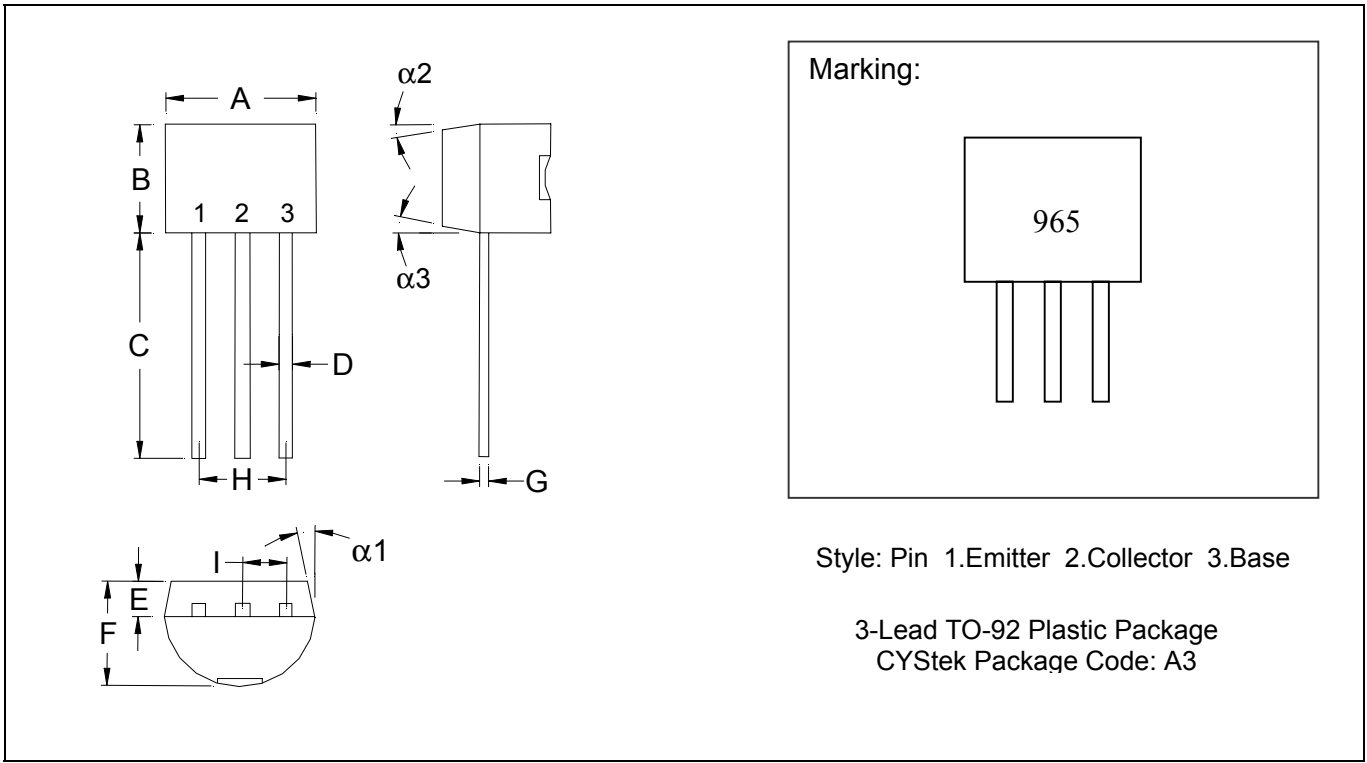
Cutoff Frequency vs Collector Current



Power Derating Curve



**TO-92 Dimension**



\*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.1704	0.1902	4.33	4.83	G	0.0142	0.0220	0.36	0.56
B	0.1704	0.1902	4.33	4.83	H	-	*0.1000	-	*2.54
C	0.5000	-	12.70	-	I	-	*0.0500	-	*1.27
D	0.0142	0.0220	0.36	0.56	$\alpha 1$	-	*5°	-	*5°
E	-	*0.0500	-	*1.27	$\alpha 2$	-	*2°	-	*2°
F	0.1323	0.1480	3.36	3.76	$\alpha 3$	-	*2°	-	*2°

- Notes:** 1. Controlling dimension: millimeters.  
 2. Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.  
 3. If there is any question with packing specification or packing method, please contact your local CYStek sales office.

**Material:**

- Lead: 42 Alloy ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

**Important Notice:**

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.