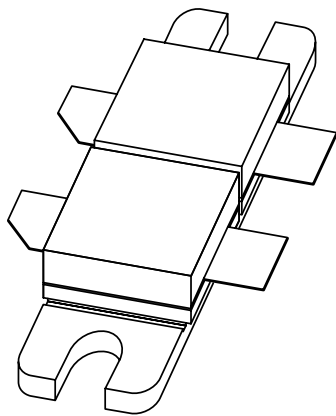


DATA SHEET



BLF368 VHF push-pull power MOS transistor

Product specification
Supersedes data of September 1992

1998 Jul 29

VHF push-pull power MOS transistor

BLF368

FEATURES

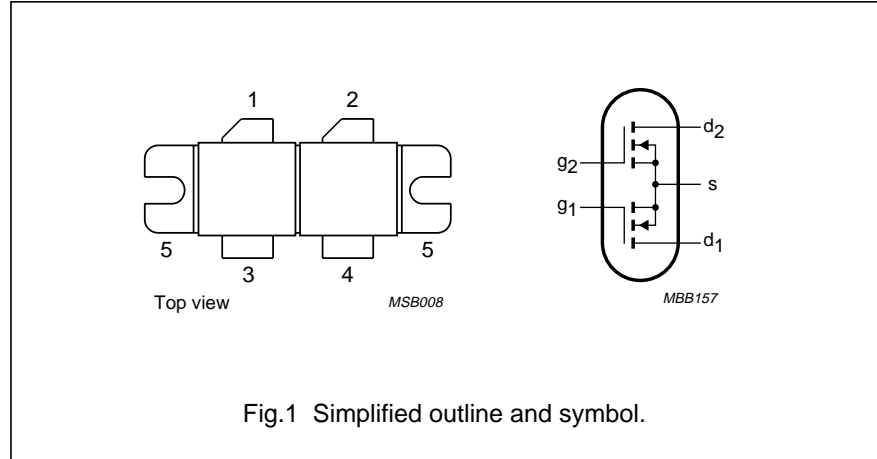
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead SOT262A1 balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PIN CONFIGURATION



CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	300	>12 typ. 13.5	>1 typ. 0.4	>55 typ. 62

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB gain compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

VHF push-pull power MOS transistor

BLF368

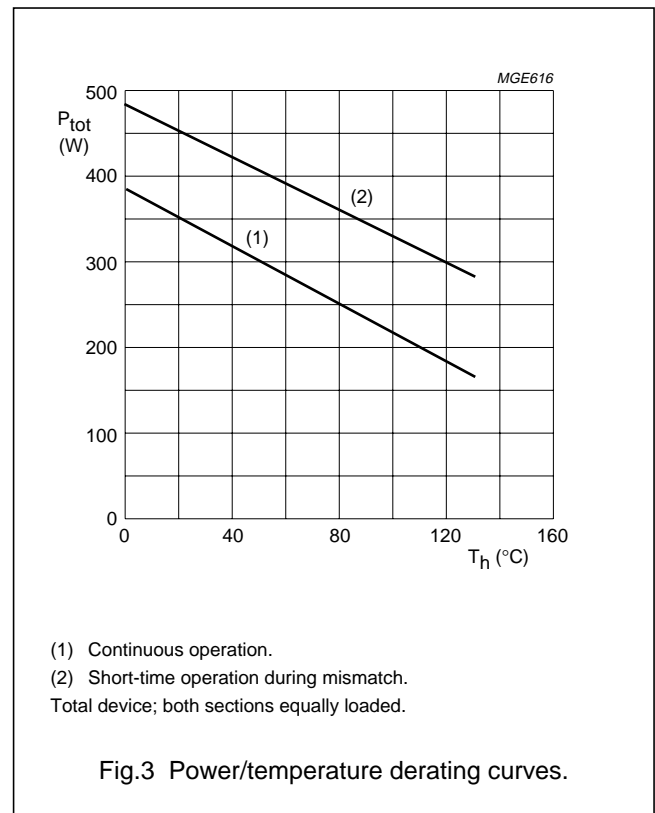
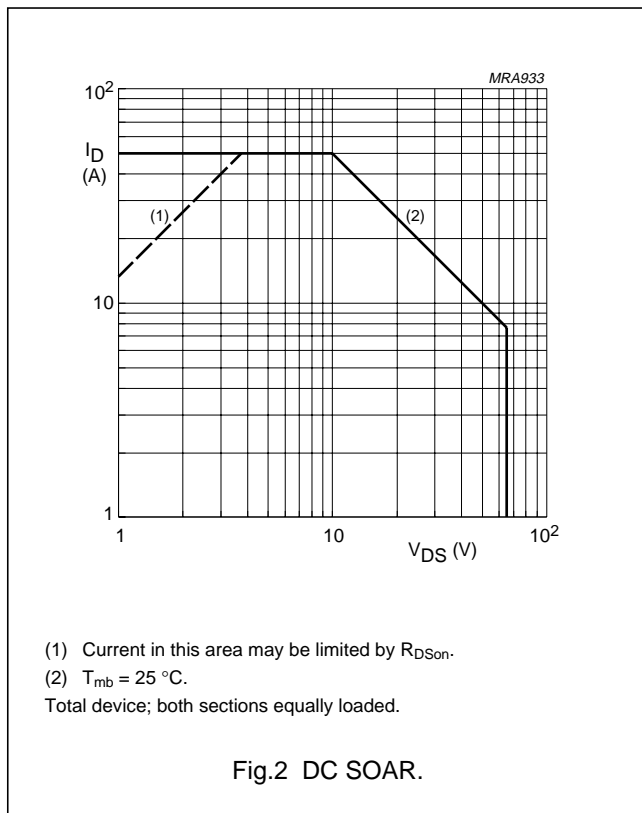
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V _{DSS}	drain-source voltage		–	65	V
V _{GSS}	gate-source voltage		–	±20	V
I _D	drain current (DC)		–	25	A
P _{tot}	total power dissipation	T _{mb} ≤ 25 °C total device; both sections equally loaded	–	500	W
T _{stg}	storage temperature		–65	150	°C
T _j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-mb}	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.35	K/W
R _{th mb-h}	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



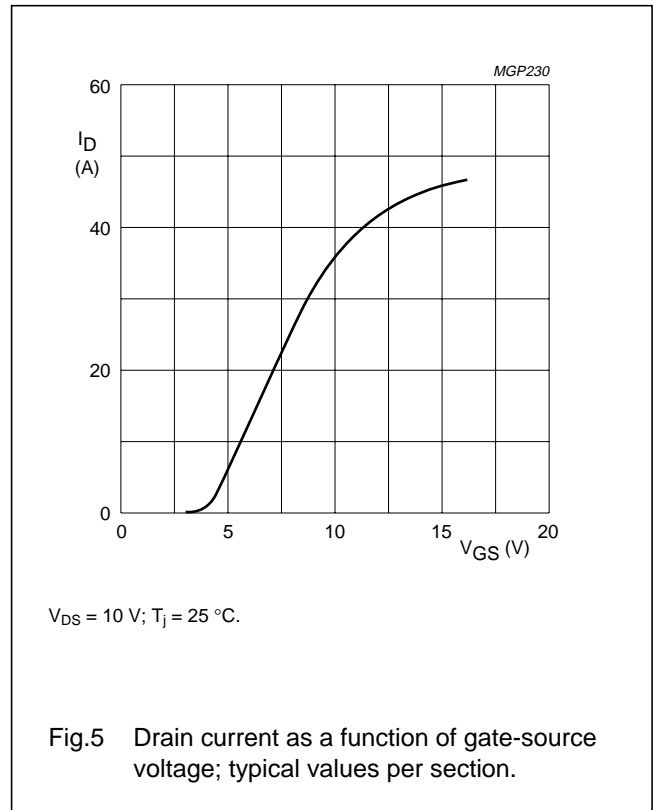
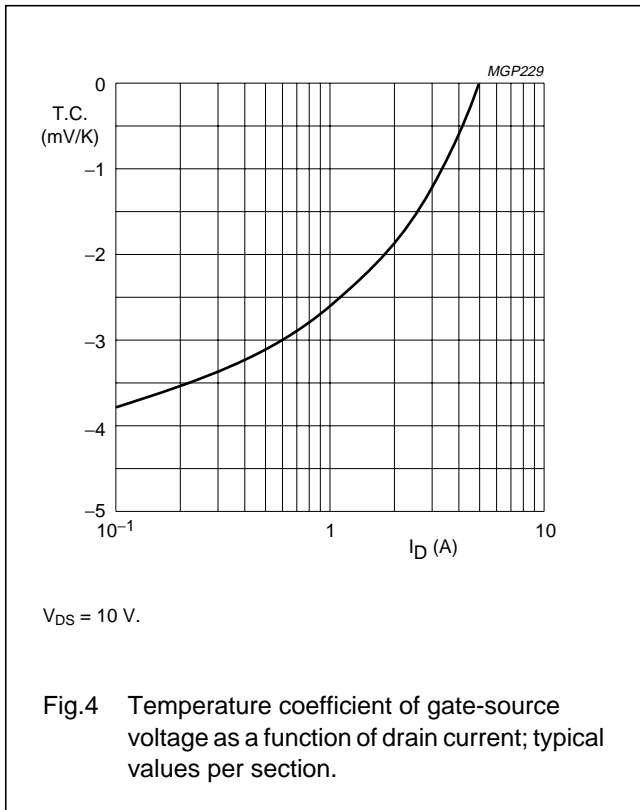
VHF push-pull power MOS transistor

BLF368

CHARACTERISTICS

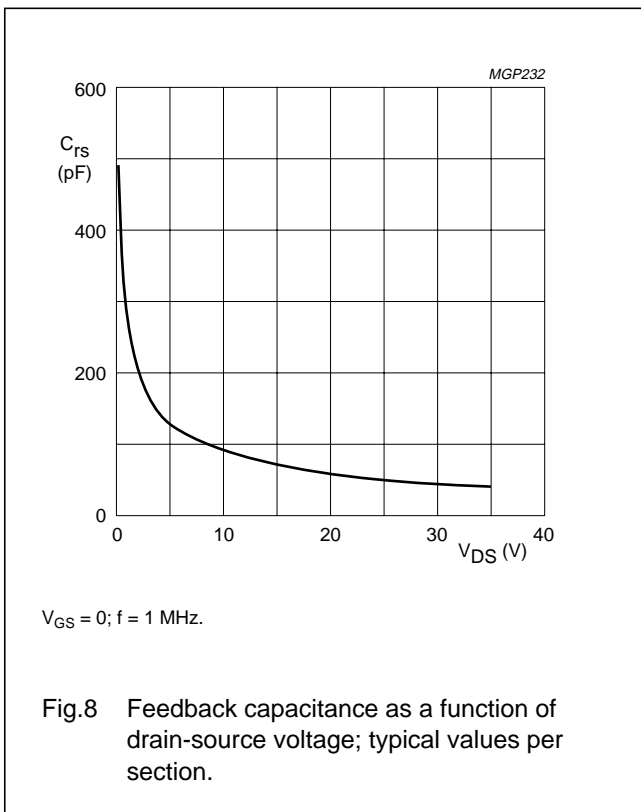
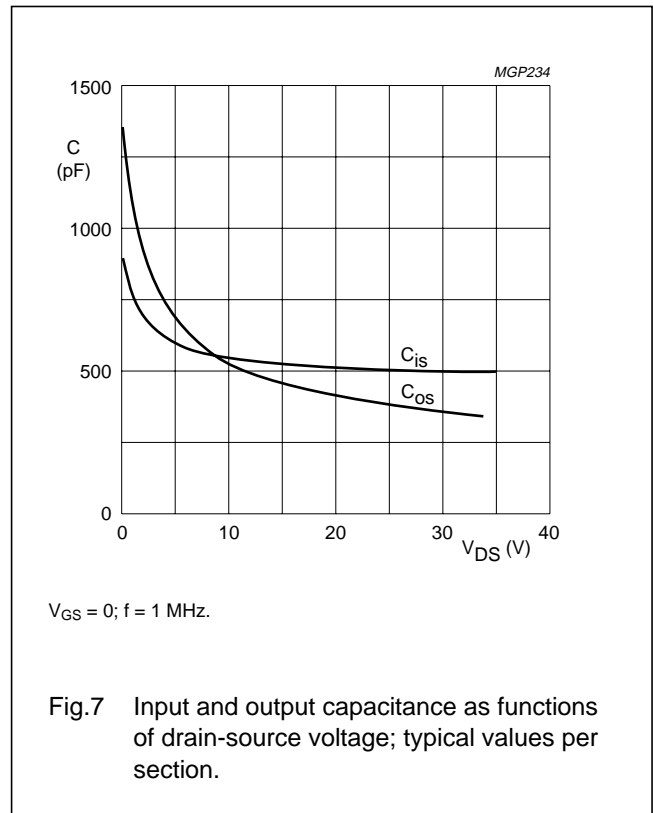
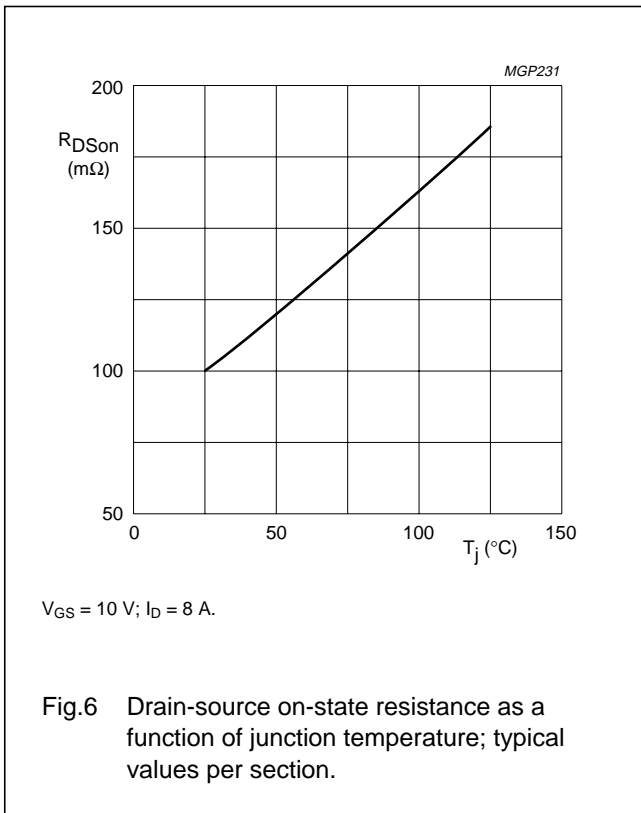
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 100\text{ mA}$	65	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = 32\text{ V}$	–	–	5	mA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0$	–	–	1	μA
V_{GSth}	gate-source threshold voltage	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	2	–	4.5	V
ΔV_{GS}	gate-source voltage difference of both transistor sections	$I_D = 100\text{ mA}; V_{DS} = 10\text{ V}$	–	–	100	mV
g_{fs}	forward transconductance	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	5	7.5	–	S
g_{fs1}/g_{fs2}	forward transconductance ratio of both transistor sections	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	0.9	–	1.1	
R_{DSon}	drain-source on-state resistance	$I_D = 8\text{ A}; V_{DS} = 10\text{ V}$	–	0.1	0.15	Ω
I_{DSX}	on-state drain current	$V_{GS} = 10\text{ V}; V_{DS} = 10\text{ V}$	–	37	–	A
C_{is}	input capacitance	$V_{GS} = 0; V_{DS} = 32\text{ V}; f = 1\text{ MHz}$	–	495	–	pF
C_{os}	output capacitance	$V_{GS} = 0; V_{DS} = 32\text{ V}; f = 1\text{ MHz}$	–	340	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0; V_{DS} = 32\text{ V}; f = 1\text{ MHz}$	–	40	–	pF
C_{d-f}	drain-flange capacitance		–	5.4	–	pF



VHF push-pull power MOS transistor

BLF368



VHF push-pull power MOS transistor

BLF368

APPLICATION INFORMATION FOR CLASS-AB OPERATION

$T_h = 25\text{ }^\circ\text{C}$; $R_{th\text{ mb-h}} = 0.15\text{ K/W}$ unless otherwise specified. RF performance in CW operation in a common source class-AB circuit. $R_{GS} = 536\ \Omega$ per section; optimum load impedance per section = $1.34 + j0.34\ \Omega$; $V_{DS} = 32\text{ V}$.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	ΔG_p (dB) (note 1)	η_D (%)
CW, class-AB	225	32	2×250	300	>12 typ. 13.5	>1 typ. 0.4	>55 typ. 62
	225	28	2×250	300	typ. 13	typ. 0.7	typ. 68
	225	35	2×250	300	typ. 14	typ. 0.2	typ. 60
	175	28	2×250	300	typ. 15	typ. 0.5	typ. 70

Note

1. Assuming a 3rd order amplitude transfer characteristic, 1 dB compression corresponds with 30% synchronized input/25% synchronized output compression in television service (negative modulation, CCIR system).

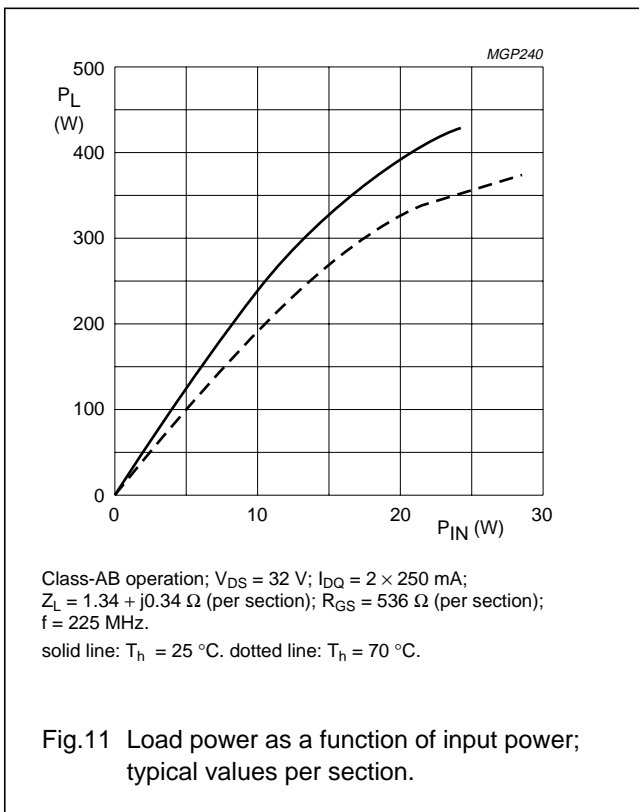
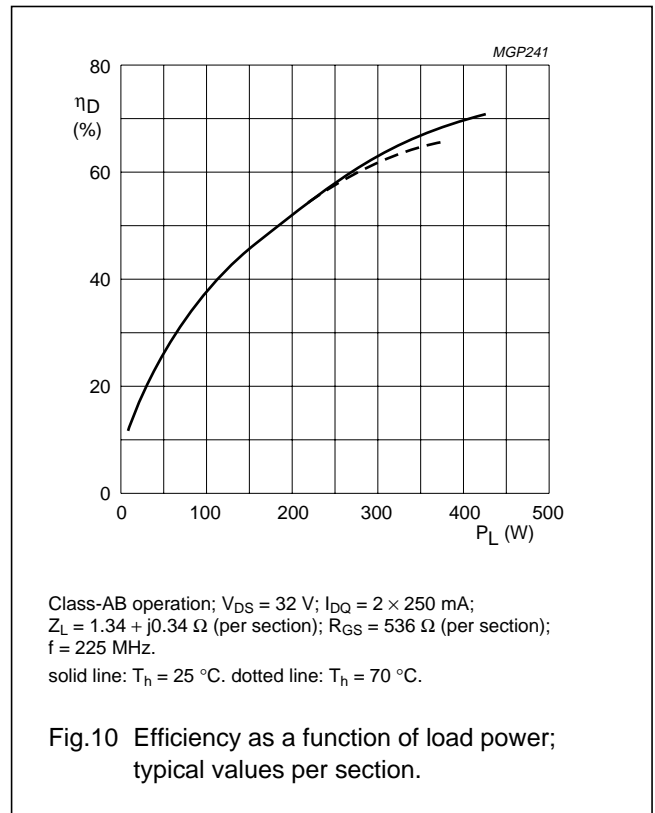
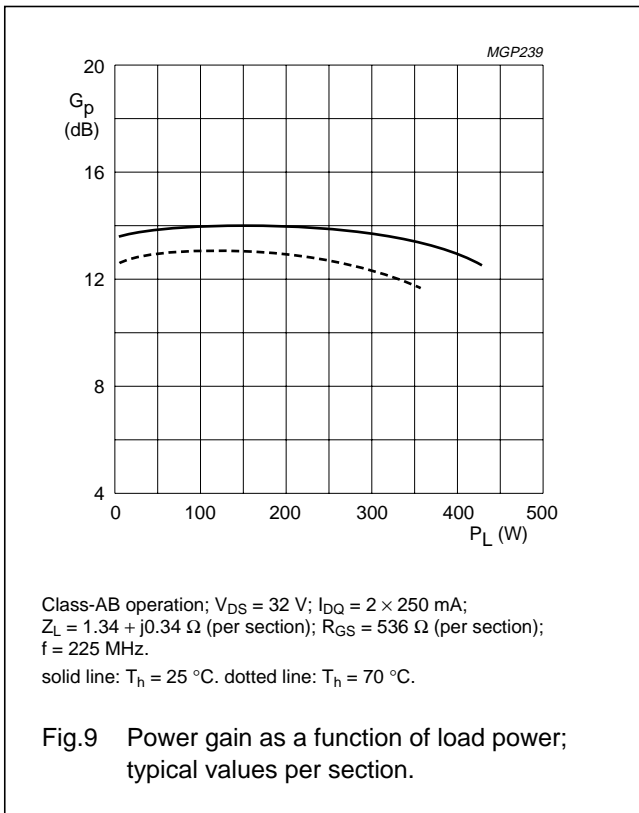
Ruggedness in class-AB operation

The BLF368 is capable of withstanding a load mismatch corresponding to $V_{SWR} = 10$ through all phases under the following conditions:

$V_{DS} = 32\text{ V}$; $f = 225\text{ MHz}$ at rated output power.

VHF push-pull power MOS transistor

BLF368



VHF push-pull power MOS transistor

BLF368

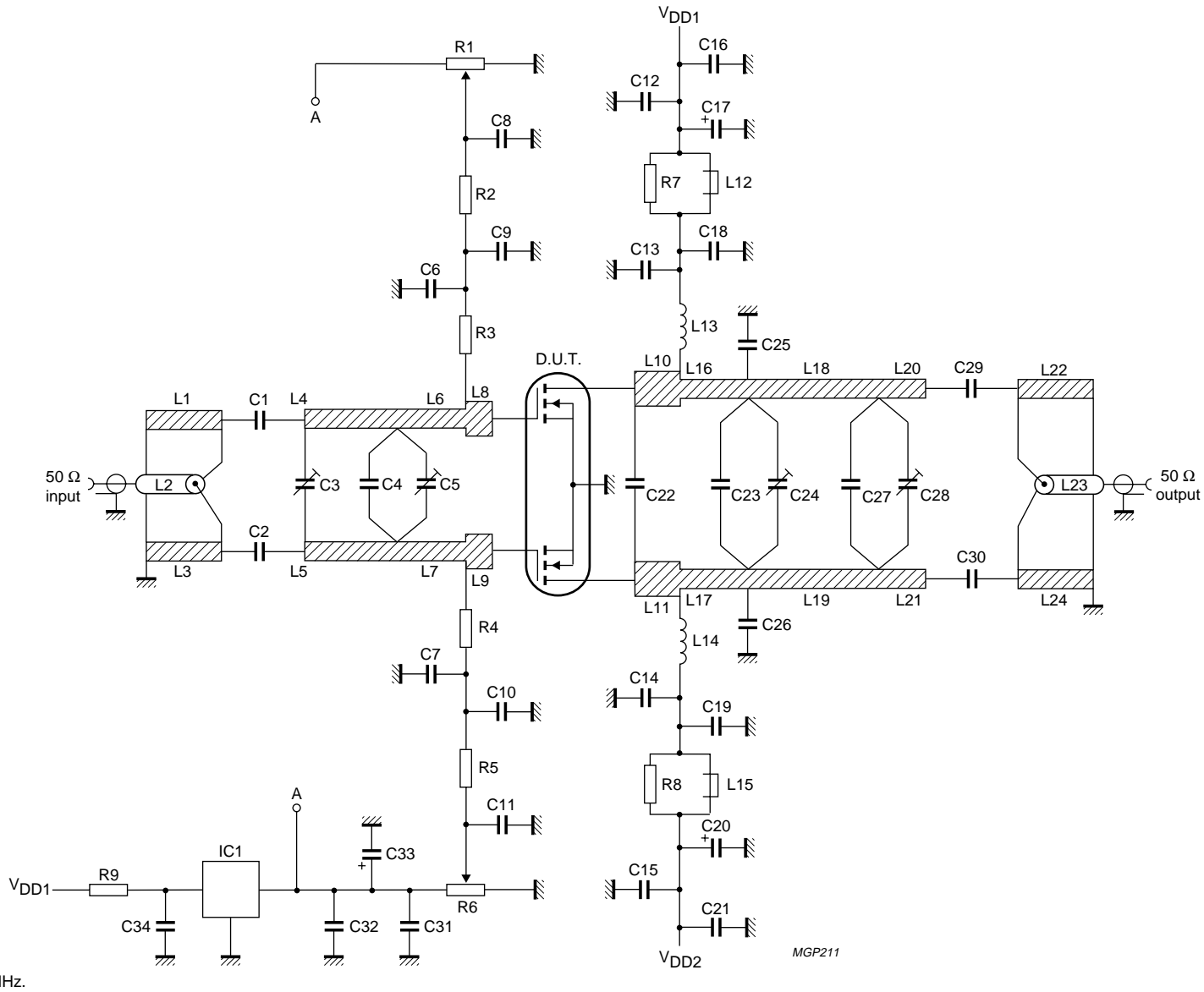


Fig.12 Test circuit for class-AB operation.

f = 225 MHz.

VHF push-pull power MOS transistor

BLF368

List of components class-AB test circuit (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2	multilayer ceramic chip capacitor (note 1)	2 × 56 pF in parallel + 18 pF, 500 V		
C3	film dielectric trimmer	2 to 9 pF		2222 809 09005
C4	multilayer ceramic chip capacitor (note 1)	47 pF, 500 V		
C5	film dielectric trimmer	5 to 60 pF		2222 809 08003
C6, C7, C9, C10, C12, C15, C31, C34	multilayer ceramic chip capacitor (note 1)	1 nF, 500 V		2222 852 47104
C8, C11, C16, C21, C32	multilayer ceramic chip capacitor (note 1)	100 nF, 50 V		
C17, C20, C33	electrolytic capacitor	10 µF, 63 V		
C22	multilayer ceramic chip capacitor (note 1)	82 pF, 500 V		
C23	multilayer ceramic chip capacitor (note 1)	10 pF + 30 pF in parallel, 500 V		
C24, C28	film dielectric trimmer	2 to 18 pF		2222 809 09006
C25, C26	multilayer ceramic chip capacitor (note 1)	39 pF + 47 pF in parallel, 500 V		
C27	multilayer ceramic chip capacitor (note 1)	18 pF, 500 V		
C29, C30	multilayer ceramic chip capacitor (note 1)	3 × 100 pF in parallel, 500 V		
L1, L3, L22, L24	stripline (note 2)	50 Ω	4.8 × 80 mm	
L2, L23	semi-rigid cable (note 3)	50 Ω	ext. conductor length 80 mm ext. dia 3.6 mm	
L4, L5	stripline (note 2)	43 Ω	6 × 32.5 mm	
L6, L7	stripline (note 2)	43 Ω	6 × 10.5 mm	
L8, L9	stripline (note 2)	43 Ω	6 × 3 mm	
L10, L11	stripline (note 2)	43 Ω	6 × 10.5 mm	
L12, L15	grade 3B Ferroxcube wideband HF choke	2 in parallel		4312 020 36642
L13, L14	2 turns enamelled 1.6 mm copper wire	25 nH	space 2.5 mm int. dia. 5 mm leads 2 × 7 mm	
L16, L17	stripline (notes 2 and 4)	43 Ω	6 × 3 mm	
L18, L19	stripline (notes 2 and 4)	43 Ω	6 × 35 mm	
L20, L21	stripline (notes 2 and 4)	43 Ω	6 × 9 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R5	metal film resistor	0.4 W, 1 kΩ		
R3, R4	metal film resistor	0.4 W, 536 Ω		

VHF push-pull power MOS transistor

BLF368

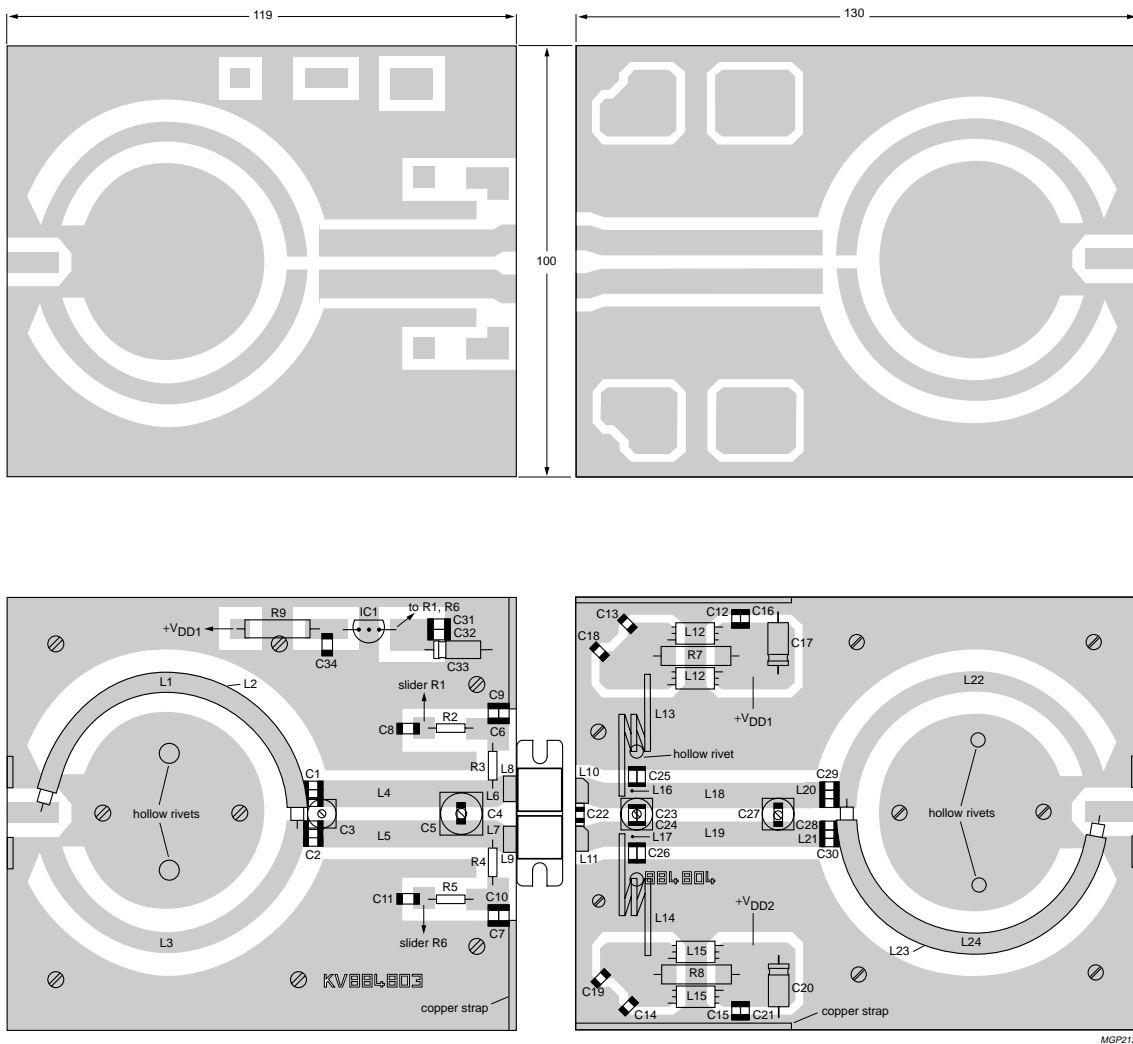
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
R7, R8	metal film resistor	1 W, $\pm 5\%$, 10 Ω		
R9	metal film resistor	1 W, 3.16 k Ω		
IC1	voltage regulator 78L05			

Notes

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L11, L16 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric ($\epsilon_r = 2.2$); thickness $\frac{1}{16}$ inch; thickness of copper sheet $2 \times 35 \mu\text{m}$.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered over the complete striplines L16 - L21 to avoid overheating by large RF currents.

VHF push-pull power MOS transistor

BLF368

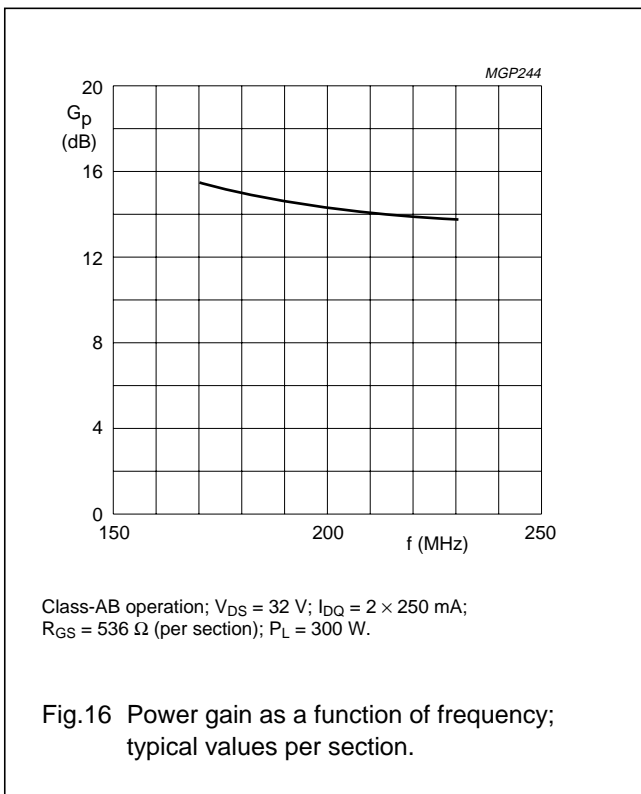
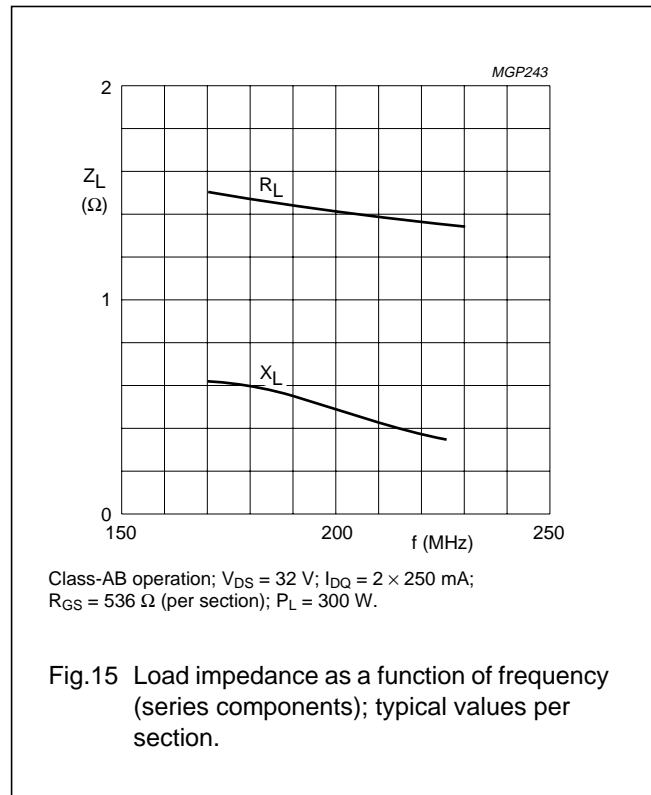
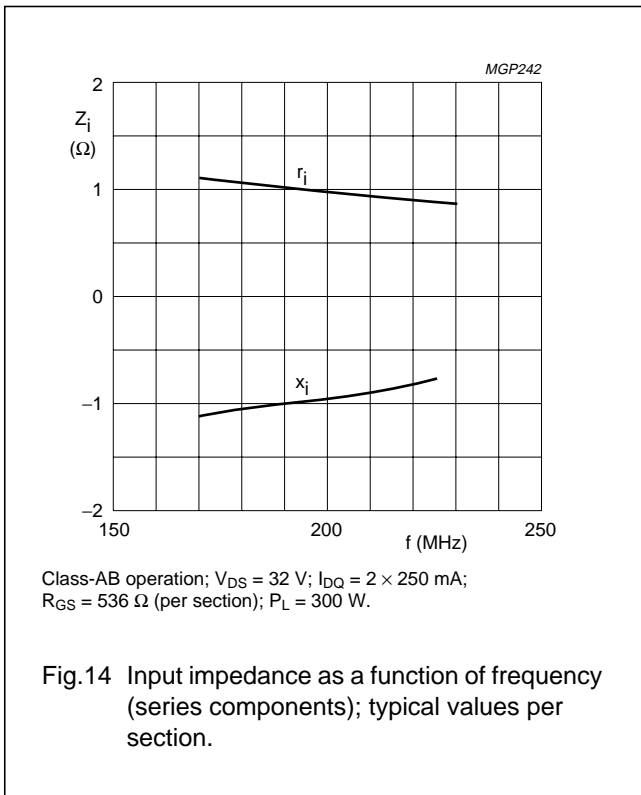


The circuit and components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets. Dimensions in mm.

Fig.13 Component layout for 225 MHz class-AB test circuit.

VHF push-pull power MOS transistor

BLF368



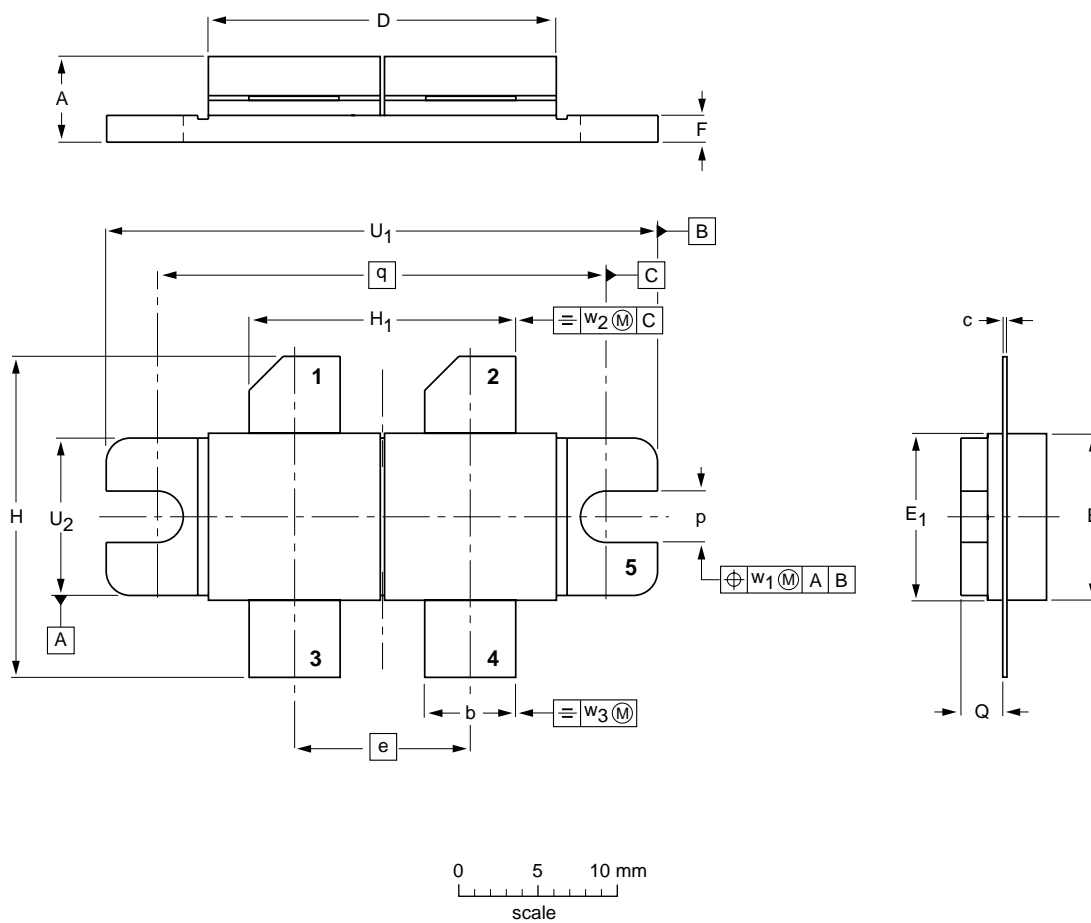
VHF push-pull power MOS transistor

BLF368

PACKAGE OUTLINE

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT262A1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	e	E	E ₁	F	H	H ₁	p	Q	q	U ₁	U ₂	w ₁	w ₂	w ₃
mm	5.77 5.00	5.85 5.58	0.16 0.10	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	20.58 20.06	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.51	1.02	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.865 0.855	0.435	0.404 0.396	0.405 0.395	0.070 0.060	0.81 0.79	0.67 0.65	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						97-06-28

VHF push-pull power MOS transistor

BLF368

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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BLF368

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