8bit 20ch D/A converter

BH2222FV

BH2222FV is an 8bit D/A converter for electronic adjustment. The 20-channel output voltage can be independently controlled by three-wire serial interface from micro-controller. The built-in power on reset circuit keeps the output state Low after the power is on. 4-channel have data register function. Two kinds of set voltage can be retained, and output voltage can be switched by SEL pin.

●Applications

The voltage adjustment for DVC, DSC etc.

●Features

1) 8bit 20-channel D/A converters adopting R-2R system.
2) 3-wire + 1-wire 16-bit serial interface.
3) POWER ON RESET circuit.
4) The full scale output voltage range : 2.7 ~ 5.5V.
5) It is possible to set the two output full scale level independently.
6) 4-channel date Register extension function.
7) SSOP-B28 package.

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	–0.3~+7.0	V
Maximum output voltage	V_{IN}	–0.3~V_{CC}	V
Storage temperature	Tstg	–55~+125	°C
Power dissipation	Pd	640 *	mW

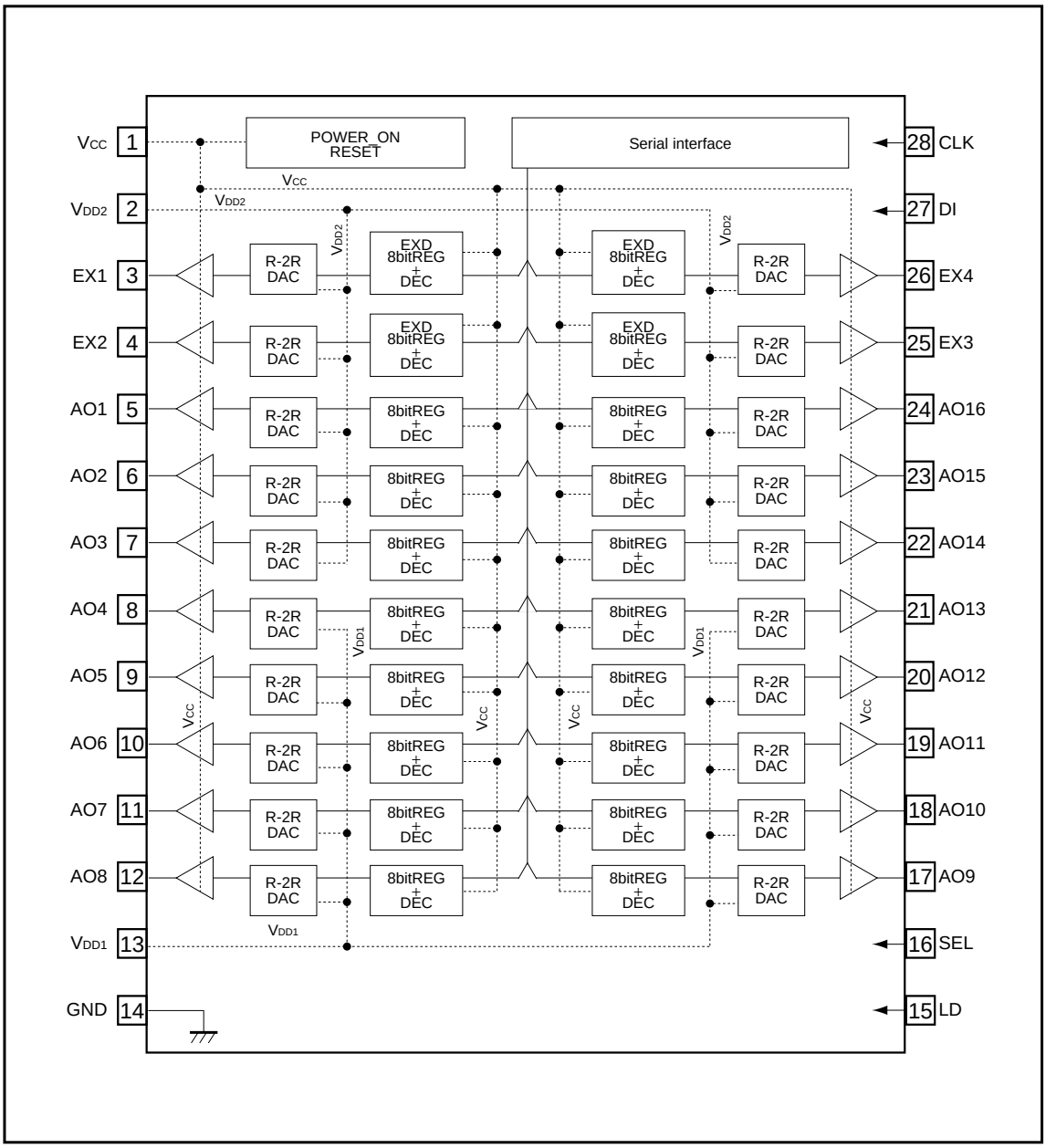
∗Reduced by 6.4mW for each increase in Ta of 1°C over 25°C.
◎This product is not designed for protection against radioactive rays.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{CC} supply voltage	V_{CC}	4.5	–	5.5	V
$V_{DD}1$ supply voltage	$V_{DD}1$	2.7	–	V_{CC}	V
$V_{DD}2$ supply voltage	$V_{DD}2$	2.7	–	V_{CC}	V
Analog output source current	I_{OL}	–	–	1.0	mA
Analog output sink current	I_{OH}	–	–	1.0	mA
Operating temperature range	Topr	–20	–	85	°C
Clock frequency	FSCLK	–	1.0	–	MHz
Limit load capacitance	CL	–	–	0.47	μF

Please set to $V_{CC} \geq V_{DD}1, V_{DD}2$.

●**Block diagram**



●**Pin descriptions**

Pin No.	Pin name	In / Out	Power supply	Functions
1	V_{CC}	–	–	Power supply pin
2	$V_{DD}2$	–	–	Power supply pin
3	EX1	OUT	$V_{DD}2$	Analog output pins (Register extension)
4	EX2	OUT	$V_{DD}2$	
5	AO1	OUT	$V_{DD}2$	Analog output pins
6	AO2	OUT	$V_{DD}2$	
7	AO3	OUT	$V_{DD}2$	
8	AO4	OUT	$V_{DD}1$	
9	AO5	OUT	$V_{DD}1$	
10	AO6	OUT	$V_{DD}1$	
11	AO7	OUT	$V_{DD}1$	
12	AO8	OUT	$V_{DD}1$	
13	$V_{DD}1$	–	–	Power supply pin
14	GND	–	–	Common GND pin
15	LD	IN	–	Serial Load input pin
16	SEL	IN	–	Select extended data register pin
17	AO9	OUT	$V_{DD}1$	Analog output pins
18	AO10	OUT	$V_{DD}1$	
19	AO11	OUT	$V_{DD}1$	
20	AO12	OUT	$V_{DD}1$	
21	AO13	OUT	$V_{DD}1$	
22	AO14	OUT	$V_{DD}2$	
23	AO15	OUT	$V_{DD}2$	
24	AO16	OUT	$V_{DD}2$	
25	EX3	OUT	$V_{DD}2$	Analog output pins (Register extension)
26	EX4	OUT	$V_{DD}2$	
27	DI	IN	–	Serial Data input pin
28	CLK	IN	–	Serial Clock input pin

●**Electrical characteristics** (unless otherwise noted, Ta=25°C, V_{CC}=V_{DD}2=5.0V, V_{DD}1=3.0V, R_L=OPEN, C_L=0pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<Operating current> (80H set)						
V_{CC} system	I_{CC}	–	1.1	2.5	mA	CLK=1MHz
V_{DD}1 system	I_{DD1}	–	1.0	2.0	mA	
V_{DD}2 system	I_{DD2}	–	1.5	3.0	mA	
<Logic interface>						
Input low voltage	V_{IL}	GND	–	0.6	V	
Input high voltage	V_{IH}	2.4	–	V_{CC}	V	
Input low current	I_{IL}	–	–	10	μA	
Input high current	I_{IH}	–	–	10	μA	
<Buffer amplifier>						
Minimum output voltage	ZS1	GND	–	0.1	V	00H set I_{OH}=0.0mA
	ZS2	GND	–	0.2	V	00H set I_{OH}=0.5mA
	ZS3	GND	–	0.3	V	00H set I_{OH}=1.0mA
Maximum output voltage	FS1	V_{CC} –0.1	–	V_{CC}	V	FFH set I_{OL}=0.0mA
	FS2	V_{CC} –0.2	–	V_{CC}	V	FFH set I_{OL}=0.5mA
	FS3	V_{CC} –0.3	–	V_{CC}	V	FFH set I_{OL}=1.0mA
<DAC accuracy>						
Resolution	RES	–	8	–	bit	
Differential nonlinearity error	DNL	–1.0	–	1.0	LSB	Input code 02H~FDH
Nonlinearity error	INL	–1.5	–	1.5	LSB	Input code 02H~FDH

●**Circuit operation**

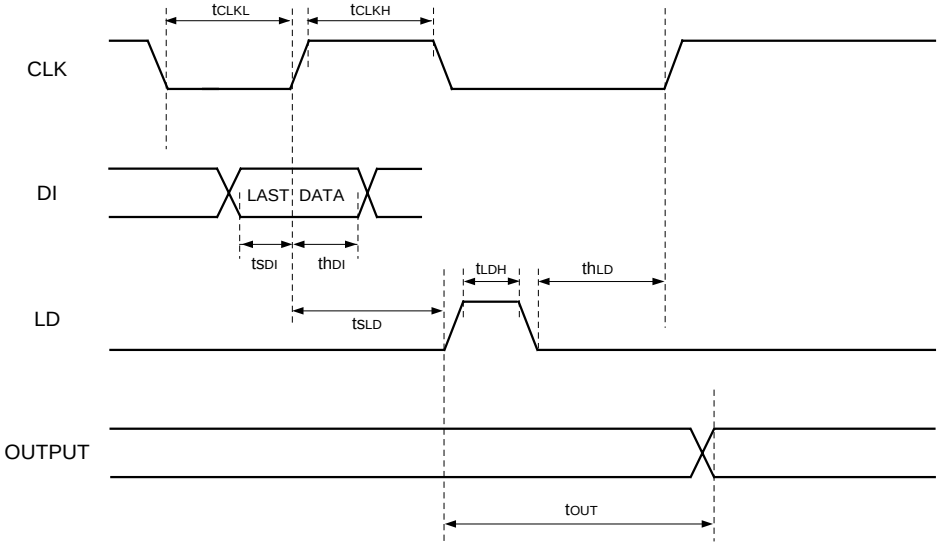
(1) Power on reset

This LSI has a power on reset circuit that sets an analog output to low level in V_{CC} power stand-up.
Please be sure that the time constant meets below condition, because the output is undefined when V_{CC} power stand up too rapidly.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} supply voltage rise time	trVcc	10	–	–	ms	V_{CC}=0→4.5V
Power on reset voltage	VPOR	–	2.1	–	V	

(2) Conditions of operating timing (unless otherwise noted,Ta=25°C, V_{CC}=5.0V, V_{DD}1=3.0V, V_{DD}2=5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK L level pulse width	t_{CLKL}	200	–	–	ns	
CLK H level pulse width	t_{CLKH}	200	–	–	ns	
DI setup time	t_{SDI}	30	–	–	ns	
DI hold time	t_{HDI}	60	–	–	ns	
LD setup time	t_{SLD}	200	–	–	ns	
LD hold time	t_{HLD}	100	–	–	ns	
LD "H" level pulse width	t_{LDH}	100	–	–	ns	
Analog output delay time	t_{OUT}	–	–	200	µs	C_L=50pF, R_L=10kΩ



(3) Command sending

Control command is 3+1wire 16bit serial interface. (LSB first)

Data is taken in with the rise edge of the CLK and output data is fixed in the LD high section.

Data is maintained in the LD low section.

Please change SEL mode in the LD low section.

MSB (LAST) LSB (FIRST)

Data set								Channel select							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

•Data set

D15	D14	D13	D12	D11	D10	D9	D8	Analog output voltage level
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(V_{DD}1, 2-GND) / 256×1
0	0	0	0	0	0	1	0	(V_{DD}1, 2-GND) / 256×2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	((V_{DD}1, 2-GND) / 256×254
1	1	1	1	1	1	1	1	((V_{DD}1, 2-GND) / 256×255

•Channel select

D7	D6	D5	D4	D3	D2	D1	D0	Function	SEL	Output pin
×	×	×	0	0	0	0	0	Don't Care	×	×
×	×	×	0	0	0	0	1	AO1	×	AO1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
×	×	×	1	0	0	0	0	AO16	×	AO16
×	×	×	1	0	0	0	1	EX1_0	0	EX1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
×	×	×	1	0	1	0	0	EX4_0	0	EX4
×	×	×	1	0	1	0	1	EX1_1	1	EX1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
×	×	×	1	1	0	0	0	EX4_1	1	EX4
×	×	×	1	1	0	0	1	Don't Care	×	×
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
×	×	×	1	1	1	1	1	Don't Care	×	×

× : Don't Care

●**Operation notes**

(1) Regarding to the DNL & INL

This item is guaranteed under below condition.

Input code 02H~FDH

(2) Regarding to the early stage condition

With the power on reset, the output is fixed to low level in power stand-up.

But the output is undefined when only LD signal is inputted. Input the LD signal after setting data.

(3) Regarding to the setting of the each voltage

Set the V_{CC}, $V_{DD}1$, $V_{DD}2$ to become the following condition. When not satisfied, unnecessary current flows.

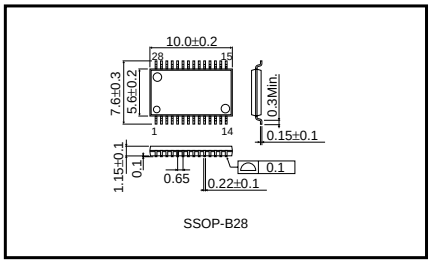
$V_{CC} \geq V_{DD}1, V_{DD}2$

(4) Regarding to the power on reset function

This function operates detecting the voltage level of the V_{CC}.

So, if the voltage level of the V_{CC} become less than power on reset voltage when working, it is a possibility that the outputs become reset condition.

●**External dimensions** (Units : mm)



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