BCM8212

PRODUCT Brief

TRANSCEIVER WITH INTERNAL LOOP TIMING AND PHASE DETECTOR

FEATURES

- 2.488-Gbps SONET/SDH transceiver with dual differential serial I/O
- Fully integrated CDR, MUX, DEMUX, and CMU with 16-bit, 155.52-MHz LVPECL interface
- On-chip, PLL-based clock generator
- Internal phase detector and charge pump for cleanup PLL
- Line and system loopback modes
- Loss-of-signal output (LOSB) and input (LOSIB)
- TX and RX lock detect
- Elastic buffering with FIFO overflow alarm
- Selectable 77.76/155.52-MHz reference clock
- Selectable RX clock and RX data squelch on LOS
- Selectable loop timing mode
- Dual 2.5V/3.3V supplies
- Power dissipation: 1.2W typical
- Selectable divide-by-32 or divide-by-16 receiver/ transmitter low-speed parallel output clock
- Standard CMOS fabrication process
- 23 ¥ 23 mm, 208-pin BGA package

SUMMARY OF BENEFITS

- Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.
- Supports SONET dual-fiber ring architecture.8212-PB05-R
- High integration reduces design cycle and time to market.
- Provides increased port density per board and system.
- Features low jitter: 3 mUI$_{RMS}$ typical.
- CMOS-based device uses the most effective silicon economy of scale.
- Exceeds SONET jitter requirements, which allows the use of low-cost optics.
- Target applications:
  - OC-48/STM-16 transmission equipment
  - SONET/SDH optical modules
  - ADD/DROP multiplexers
  - Digital cross-connects
  - ATM switch backboneONET/SDH test equipment
  - SONET/SDH test equipment
  - Terabit and edge routers

Application Block Diagram