nLiten BBT3421 Quad Multi-rate Re-Timer

Data Sheet | August, 2002 | FN7482

4 Channel Multi-rate Intelligent CMOS Re-Timer

Features

- 4 channels of clock & data recovery and retiming
- Multi-Speed Operation for OC-48, InfiniBand, XAUI, 10GFC-SN4 rate
  - 2.488Gbps to 3.187Gbps with half-rate support
- IEEE 802.3ae Compliant
  - 10GBASE-LX4 (WWDM)
  - Random jitter 2.5ps (typical)
- 250mW typical power consumption per channel
- 1.8V power supply with 3.3V I/O tolerant
- Drive up to 40” FR-4 traces and 500 meters of MMF fiber
- Single-ended or differential input reference clock
  - Data rate/20 for multi-rate data
- Intelligent Retiming
- Deskewing and Channel-to-Channel Alignment
- Clock Compensation
  - Tx/Rx Rate Matching via IDLE Insertion/Deletion
  - Received Data Aligned to Local Reference Clock for Transmission
  - Accommodate up to ±100ppm clock frequency offset
- CML Rx with Signal Detect and Programmable Transmission Medium Equalization
- CML Tx with Adjustable Pre-emphasis
- Long Run Length (512 bit) frequency lock ideal for proprietary encoding schemes
- Extensive configuration and status reporting via 802.3 compliant MDC/MDIO serial interface
- MDIO Interface Compliant with IEEE 802.3ae Clause 45 and Clause 22 Frame Formats
- 10 x 10mm 144 pin 0.8mm pitch LFBGA package

Applications

- Intelligent Retimer required for 10Gigabit Ethernet compliance (10GBASE-LX4)
- Support 10Gigabit Fibre Channel
- Support OC-48 Rate
- Support InfiniBand
- Ideal for parallel optics Backplane Extension of up to 40 inches

Benefits

- Industry-leading power performance
- Programmable Receiver Equalization and preemphasis increase link distance and design flexibility
  - Reduced EMI, cross-talk
- Link distances greater than 40” FR-4 traces and two connectors
- Proven Interoperability with various backplanes, optical modules and semiconductors
- Ease of testing
  - PRBS (both 2^{23}-1 and 13458 byte) Built-In Self Tests, error code output
  - JTAG Boundary Scan, Support for Built-In Self Test
- Complete applications collateral
  - Evaluation Board
  - Applications Note
  - Verilog Model; SPICE Model
  - High-Speed System Engineering technical support

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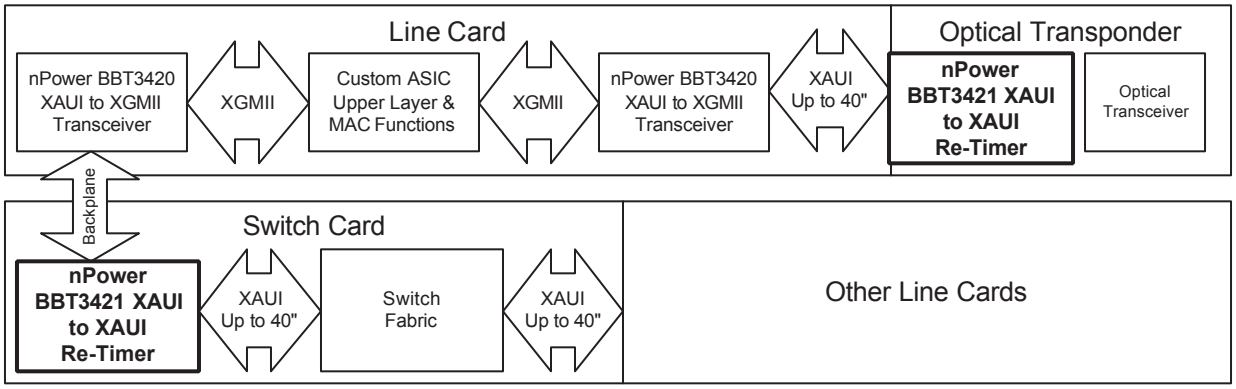

FIGURE 1. BBT3421 APPLICATIONS

Data Flow

The BBT3421 re-timer accepts serial data from the CML pins, performs clock and data recovery on the bit stream, optionally scans the data for the “comma” patterns, Byte-Aligns the data on either ‘disparity’ comma pattern, and de-serializes the data. The data is then fed into the receive FIFO, where clock compensation, and optional channel alignment are performed. The parallel data is then resynchronized into the Transmit FIFO using the local reference clock, serialized to this local reference clock, and sent out to the differential CML, XAUIcompatible TX pins.

In addition, several other facilities are provided to ease system testing. Loop-back of the serial signals is available under external pin or MII control. Suitable control and status registers are available through the IEEE standard MDIO/MDC system. If the Built-in-Self-Test function (BIST) is in use, the serial TX data instead is derived from a PRBS 2^23 -1 pattern generator. In this BIST mode, the received serial data is checked against the PRBS pattern transmitted and, if an error is found, a flag signal is provided.

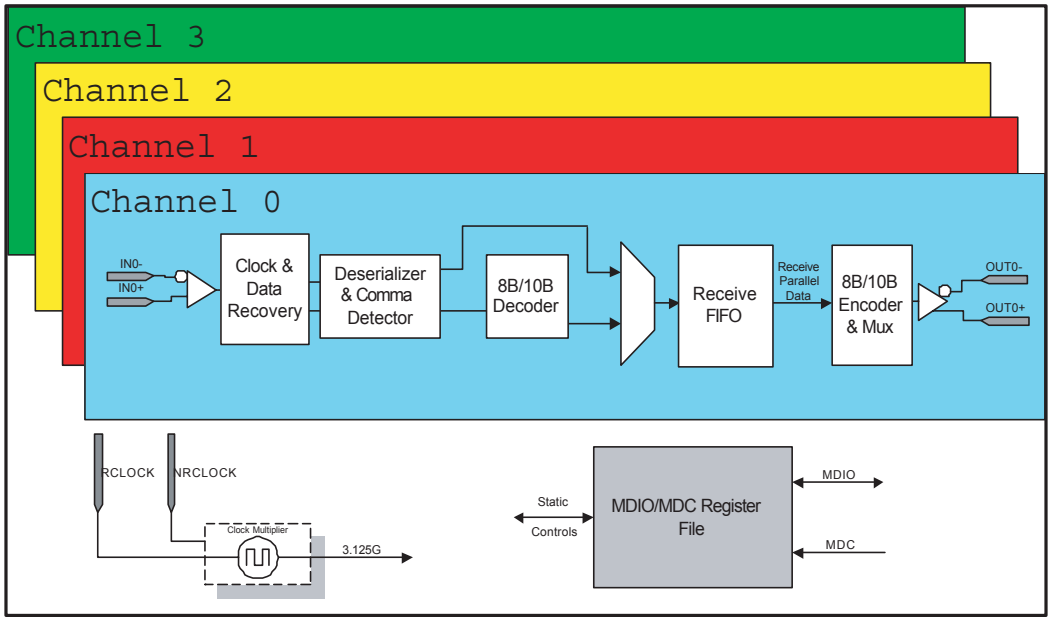

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM OF BBT3421