# 2.5V or 3.3V, 200 MHz, 9-Output Zero Delay Buffer

## Features

- Output frequency range: 25 MHz to 200 MHz
- Input frequency range: 25 MHz to 200 MHz
- 2.5V or 3.3V operation
- Split 2.5V/3.3V outputs
- ± 2.5% max Output duty cycle variation
- Nine Clock outputs: Drive up to 18 clock lines
- Two reference clock inputs: LVPECL or LVCMOS
- 150-ps max output-output skew
- Phase-locked loop (PLL) bypass mode
- 'SpreadTrak'
- Output enable/disable
- Pin-compatible with MPC9351 and CY29351.
- Industrial temperature range: –40°C to +85°C
- 32-pin 1.0mm TQFP & LQFP Package.

## Functional Description

The ASM5I9351 is a low voltage high performance 200MHz PLL-based zero delay buffer designed for high speed clock distribution applications.

The ASM5I9351 features LVPECL and LVCMOS reference clock inputs and provides 9 outputs partitioned in 4 banks of 1, 1, 2, and 5 outputs. Bank A divides the VCO output by 2 or 4 while the other banks divide by 4 or 8 per SEL(A:D) settings, see Table.2. These dividers allow output to input ratios of 4:1, 2:1, 1:1, 1:2, and 1:4. Each LVCMOS compatible output can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:18.

The PLL is ensured stable given that the VCO is configured to run between 200 MHz to 500 MHz. This allows a wide range of output frequencies from 25 MHz to 200 MHz. For normal operation, the external feedback input, FB_IN, is connected to one of the outputs. The internal VCO is running at multiples of the input reference clock set by the feedback divider, see the Table 1.

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply.

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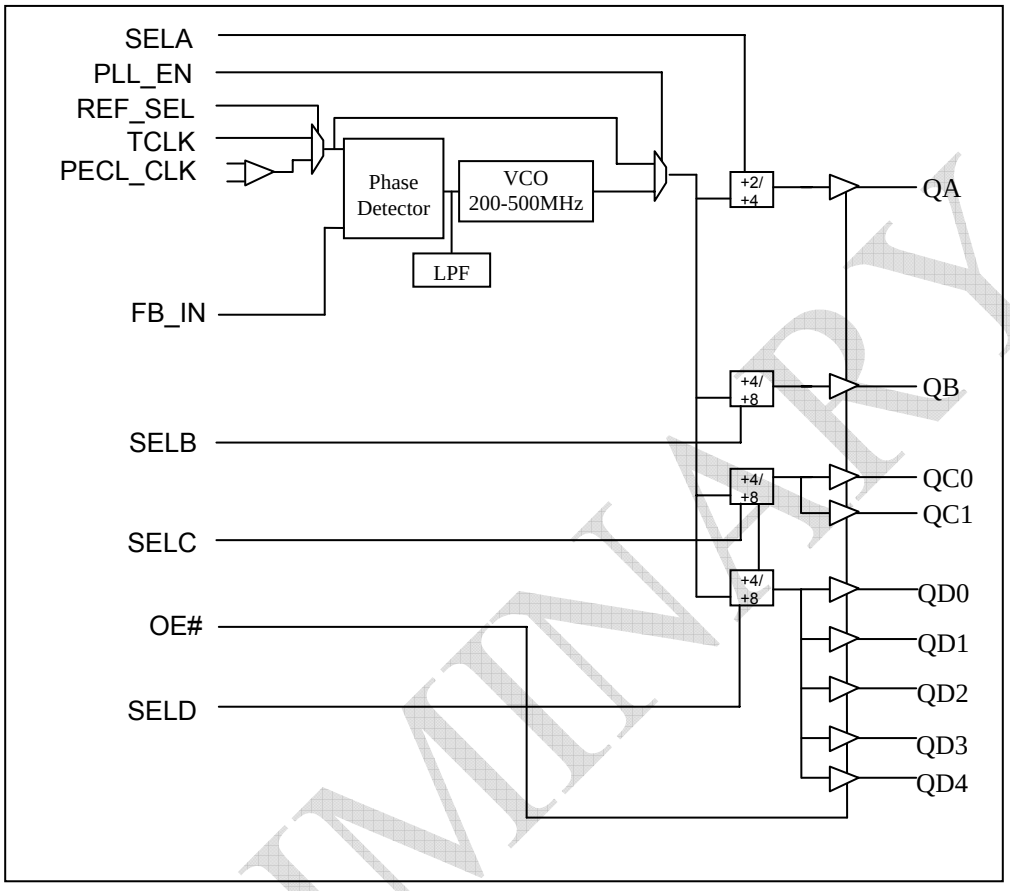
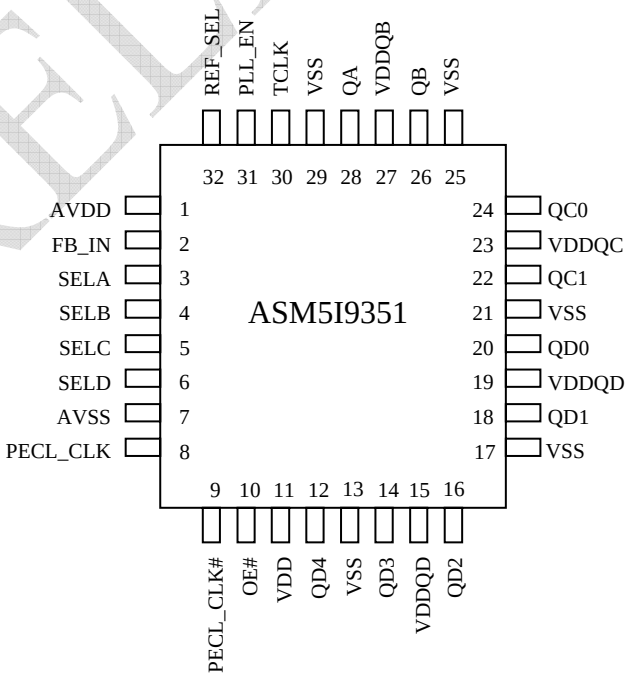
## Block Diagram




## Pin Configuration

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## Pin Configuration[1]

| Pin # | Pin Name | I/O | Type | Description |
|---|---|---|---|---|
| 8 | PECL_CLK | I, PU | Analog | **LVPECL reference clock input**. |
| 9 | PECL_CLK# | I, PU/PD | Analog | **LVPECL reference clock input**. Weak pull-up to VDD/2. |
| 30 | TCLK | I, PD | LVCMOS | **LVCMOS/LVTTL reference clock input** |
| 28 | QA | O | LVCMOS | **Clock output bank A** |
| 26 | QB | O | LVCMOS | **Clock output bank B** |
| 22, 24 | QC(1:0) | O | LVCMOS | **Clock output bank C** |
| 12, 14, 16, 18, 20 | QD(4:0) | O | LVCMOS | **Clock output bank D** |
| 2 | FB_IN | I, PD | LVCMOS | **Feedback clock input**. Connect to an output for normal operation. This input should be at the same voltage rail as input reference clock. See *Table 1*. |
| 10 | OE# | I, PD | LVCMOS | **Output enable/disable input**. See *Table 2*. |
| 31 | PLL_EN | I, PU | LVCMOS | **PLL enable/disable input**. See *Table 2*. |
| 32 | REF_SEL | I, PD | LVCMOS | **Reference select input**. See *Table 2*. |
| 3, 4, 5, 6 | SEL(A:D) | I, PD | LVCMOS | **Frequency select input, Bank (A:D)**. See *Table 2*. |
| 27 | VDDQB | Supply | VDD | **2.5V or 3.3V Power supply for bank B output clock**[2,3] |
| 23 | VDDQC | Supply | VDD | **2.5V or 3.3V Power supply for bank C output clocks**[2,3] |
| 15, 19 | VDDQD | Supply | VDD | **2.5V or 3.3V Power supply for bank D output clocks**[2,3] |
| 1 | AVDD | Supply | VDD | **2.5V or 3.3V Power supply for PLL**[2,3] |
| 11 | VDD | Supply | VDD | **2.5V or 3.3V Power supply for core, inputs, and bank A output clock**[2,3] |
| 7 | AVSS | Supply | Ground | **Analog ground** |
| 13, 17, 21, 25, 29 | VSS | Supply | Ground | **Common ground** |

Note: 1 PU = Internal pull-up, PD = Internal pull-down.

2. A 0.1µF bypass capacitor should be placed as close as possible to each positive power pin (<0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the traces.
3. AVDD and VDD pins must be connected to a power supply level that is at least equal or higher than that of VDDQB, VDDQC, and VDDQD output power supply pins.

PRELIMINARY



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### Table 1: Frequency Table

| Feedback Output Divider | VCO | Input Frequency Range (AVDD = 3.3V) | Input Frequency Range (AVDD = 2.5V) |
|---|---|---|---|
| ÷2 | Input Clock * 2 | 100 MHz to 200 MHz | 100 MHz to 190MHz |
| ÷4 | Input Clock * 4 | 50 MHz to 125 MHz | 50 MHz to 95MHz |
| ÷8 | Input Clock * 8 | 25 MHz to 62.5 MHz | 25 MHz to 47.5MHz |

### Table 2: Function Table

| Control | Default | 0 | 1 |
|---|---|---|---|
| REF_SEL | 0 | PCLK | TCLK |
| PLL_EN | 1 | Bypass mode, PLL disabled. The input clock connects to the output dividers | PLL enabled. The VCO output connects to the output dividers |
| OE# | 0 | Outputs enabled | Outputs disabled (three-state), VCO running at its minimum frequency |
| SELA | 0 | ÷2 (Bank A) | ÷ 4 (Bank A) |
| SELB | 0 | ÷4 (Bank B) | ÷ 8 (Bank B) |
| SELC | 0 | ÷4 (Bank C) | ÷ 8 (Bank C) |
| SELD | 0 | ÷4 (Bank D) | ÷ 8 (Bank D) |

### Absolute Maximum Ratings

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | | –0.3 | 5.5 | V |
| $V_{DD}$ | DC Operating Voltage | Functional | 2.375 | 3.465 | V |
| $V_{IN}$ | DC Input Voltage | Relative to $V_{SS}$ | –0.3 | $V_{DD}$+ 0.3 | V |
| $V_{OUT}$ | DC Output Voltage | Relative to $V_{SS}$ | –0.3 | $V_{DD}$+ 0.3 | V |
| $V_{TT}$ | Output termination Voltage | | | $V_{DD}$ ÷2 | V |
| LU | Latch Up Immunity | Functional | 200 | | mA |
| $R_{PS}$ | Power Supply Ripple | Ripple Frequency < 100 kHz | | 150 | mVp-p |
| $T_S$ | Temperature, Storage | Non-functional | –65 | +150 | °C |
| $T_A$ | Temperature, Operating Ambient | Functional | –40 | +85 | °C |
| $T_J$ | Temperature, Junction | Functional | | +150 | °C |
| $Ø_{JC}$ | Dissipation, Junction to Case | Functional | 42 | | °C/W |
| $Ø_{JA}$ | Dissipation, Junction to Ambient | Functional | 105 | | °C/W |
| $ESD_H$ | ESD Protection (Human Body Model) | | 2000 | | Volts |
| FIT | Failure in Time | Manufacturing test | 10 | | ppm |

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

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## DC Electrical Specifications ($V_{DD}$ = 2.5V ± 5%, $T_A$ = -40°C to +85°C)

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Voltage, Low | LVCMOS | - | - | 0.7 | V |
| $V_{IH}$ | Input Voltage, High | LVCMOS | 1.7 | - | $V_{DD}$+0.3 | V |
| $V_{PP}$ | Peak-Peak Input Voltage | LVPECL | 250 | - | 1000 | mV |
| $V_{CMR}$ | Common Mode Range[1] | LVPECL | 1.0 | - | $V_{DD}$– 0.6 | V |
| $V_{OL}$ | Output Voltage, Low[2] | $I_{OL}$= 15mA | - | - | 0.6 | V |
| $V_{OH}$ | Output Voltage, High[2] | $I_{OH}$= –15mA | 1.8 | - | - | V |
| $I_{IL}$ | Input Current, Low[3] | $V_{IL}$= $V_{SS}$ | - | - | -100 | µA |
| $I_{IH}$ | Input Current, High[3] | $V_{IL}$= $V_{DD}$ | - | - | 100 | µA |
| $I_{DDA}$ | PLL Supply Current | AVDD only | - | 5 | 10 | mA |
| $I_{DDQ}$ | Quiescent Supply Current | All VDD pins except AVDD | - | - | 7 | mA |
| $I_{DD}$ | Dynamic Supply Current | Outputs loaded @ 100 MHz | - | 180 | - | mA |
| | | Outputs loaded @ 200 MHz | - | 210 | - | |
| $C_{IN}$ | Input Pin Capacitance | | - | 4 | - | pF |
| $Z_{OUT}$ | Output Impedance | | 14 | 18 | 22 | Ω |

Note: 1 $V_{CMR}$ (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the $V_{CMR}$ range and the input swing is within the $V_{PP}$ (DC) specification.
2.Driving one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
3.Inputs have pull-up or pull-down resistors that affect the input current.

## DC Electrical Specifications ($V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to +85°C)

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Voltage, Low | LVCMOS | - | - | 0.8 | V |
| $V_{IH}$ | Input Voltage, High | LVCMOS | 2.0 | - | $V_{DD}$+0.3 | V |
| $V_{PP}$ | Peak-Peak Input Voltage | LVPECL | 250 | - | 1000 | mV |
| $V_{CMR}$ | Common Mode Range[1] | LVPECL | 1.0 | - | $V_{DD}$– 0.6 | V |
| $V_{OL}$ | Output Voltage, Low[2] | $I_{OL}$= 24 mA | - | - | 0.55 | V |
| | | $I_{OL}$= 12 mA | - | - | 0.30 | |
| $V_{OH}$ | Output Voltage, High[2] | $I_{OH}$= –24 mA | 2.4 | - | - | V |
| $I_{IL}$ | Input Current, Low[3] | $V_{IL}$= $V_{SS}$ | - | - | –100 | µA |
| $I_{IH}$ | Input Current, High[3] | $V_{IL}$= $V_{DD}$ | - | - | 100 | µA |
| $I_{DDA}$ | PLL Supply Current | AVDD only | - | 5 | 10 | mA |
| $I_{DDQ}$ | Quiescent Supply Current | All VDD pins except AVDD | - | - | 7 | mA |
| $I_{DD}$ | Dynamic Supply Current | Outputs loaded @ 100 MHz | - | 270 | - | mA |
| | | Outputs loaded @ 200 MHz | - | 300 | - | |
| $C_{IN}$ | Input Pin Capacitance | | - | 4 | - | pF |
| $Z_{OUT}$ | Output Impedance | | 12 | 15 | 18 | Ω |

Note: 1 $V_{CMR}$ (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the $V_{CMR}$ range and the input swing is within the $V_{PP}$ (DC) specification.
2.Driving one 50Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, each output drives up to two 50Ω series terminated transmission lines.
3.Inputs have pull-up or pull-down resistors that affect the input current.

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## AC Electrical Specifications ($V_{DD}$ = 2.5V ± 5%, $T_A$ = -40°C to +85°C) [1]

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ | VCO Frequency | | 200 | - | 380 | MHz |
| $f_{in}$ | Input Frequency | ÷2 Feedback | 100 | - | 190 | MHz |
| | | ÷4 Feedback | 50 | - | 95 | |
| | | ÷8 Feedback | 25 | - | 47.5 | |
| | | Bypass mode (PLL_EN = 0) | 0 | - | 200 | |
| $f_{refDC}$ | Input Duty Cycle | | 25 | - | 75 | % |
| $V_{PP}$ | Peak-Peak Input Voltage | LVPECL | 500 | - | 1000 | mV |
| $V_{CMR}$ | Common Mode Range[2] | LVPECL | 1.2 | - | VDD– 0.6 | V |
| $t_r$, $t_f$ | TCLK Input Rise/FallTime | 0.7V to 1.7V | - | - | 1.0 | nS |
| $f_{MAX}$ | Maximum Output Frequency | ÷2 Output | 100 | - | 190 | MHz |
| | | ÷4 Output | 50 | - | 95 | |
| | | ÷8 Output | 25 | - | 47.5 | |
| DC | Output Duty Cycle | $f_{MAX}$ < 100 MHz | 47.5 | - | 52.5 | % |
| | | $f_{MAX}$ > 100 MHz | 45 | - | 55 | |
| $t_r$, $t_f$ | Output Rise/Fall times | 0.6V to 1.8V | 0.1 | - | 1.0 | nS |
| $t_{(\varphi)}$ | Propagation Delay (static phase offset) | TCLK to FB_IN | –100 | - | 100 | pS |
| | | PCLK to FB_IN | –100 | - | 100 | |
| $t_{sk(O)}$ | Output-to-Output Skew | | - | - | 150 | pS |
| $t_{PLZ, HZ}$ | Output Disable Time | | - | - | 10 | nS |
| $t_{PZL, ZH}$ | Output Enable Time | | - | - | 10 | nS |
| BW | PLL Closed Loop Bandwidth (–3dB) | ÷2 Feedback | - | 2.2 | - | MHz |
| | | ÷4 Feedback | - | 0.85 | - | |
| | | ÷8 Feedback | - | 0.6 | - | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | Same frequency | - | - | 150 | pS |
| | | Multiple frequencies | - | - | 250 | |
| $t_{JIT(PER)}$ | Period Jitter | Same frequency | - | - | 100 | pS |
| | | Multiple frequencies | - | - | 175 | |
| $t_{JIT(\varphi)}$ | I/O Phase Jitter | | - | 175 | - | pS |
| $t_{LOCK}$ | Maximum PLL Lock Time | | - | - | 1 | mS |

Note: 1 AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$. Parameters are guaranteed by characterization and are not 100% tested.
2. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset t(φ).

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## AC Electrical Specifications ($V_{DD}$ = 3.3V ± 5%, $T_A$ = -40°C to +85°C)[1]

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{VCO}$ | VCO Frequency | | 200 | - | 500 | MHz |
| $f_{in}$ | Input Frequency | ÷2 Feedback | 100 | - | 200 | MHz |
| | | ÷4 Feedback | 50 | - | 125 | |
| | | ÷8 Feedback | 25 | - | 62.5 | |
| | | Bypass mode (PLL_EN = 0) | 0 | - | 200 | |
| $f_{refDC}$ | Input Duty Cycle | | 25 | - | 75 | % |
| $V_{PP}$ | Peak-Peak Input Voltage | LVPECL | 500 | - | 1000 | mV |
| $V_{CMR}$ | Common Mode Range[2] | LVPECL | 1.2 | - | $V_{DD}$– 0.9 | V |
| $t_r$, $t_f$ | TCLK Input Rise/FallTime | 0.8V to 2.0V | - | - | 1.0 | nS |
| $f_{MAX}$ | Maximum Output Frequency | ÷2 Output | 100 | - | 200 | MHz |
| | | ÷4 Output | 50 | - | 125 | |
| | | ÷8 Output | 25 | - | 62.5 | |
| DC | Output Duty Cycle | $f_{MAX}$ < 100 MHz | 47.5 | - | 52.5 | % |
| | | $f_{MAX}$ > 100 MHz | 45 | - | 55 | |
| $t_r$, $t_f$ | Output Rise/Fall times | 0.8V to 2.4V | 0.1 | - | 1.0 | nS |
| $t_{(\varphi)}$ | Propagation Delay (static phase offset) | TCLK to FB_IN, same VDD | –100 | - | 100 | pS |
| | | PCLK to FB_IN, same VDD | –100 | - | 100 | |
| $t_{sk(O)}$ | Output-to-Output Skew | Banks at same voltage | - | - | 150 | pS |
| $t_{sk(B)}$ | Bank-to-Bank Skew | Banks at different voltages | - | - | 350 | pS |
| $t_{PLZ, HZ}$ | Output Disable Time | | - | - | 10 | nS |
| $t_{PZL, ZH}$ | Output Enable Time | | - | - | 10 | nS |
| BW | PLL Closed Loop Bandwidth (–3dB) | ÷2 Feedback | - | 2.2 | - | MHz |
| | | ÷4 Feedback | - | 0.85 | - | |
| | | ÷8 Feedback | - | 0.6 | - | |
| $t_{JIT(CC)}$ | Cycle-to-Cycle Jitter | Same frequency | - | - | 150 | pS |
| | | Multiple frequencies | - | - | 250 | |
| $t_{JIT(PER)}$ | Period Jitter | Same frequency | - | - | 100 | pS |
| | | Multiple frequencies | - | - | 150 | |
| $t_{JIT(\varphi)}$ | I/O Phase Jitter | I/O same VDD | - | 175 | - | pS |
| $t_{LOCK}$ | Maximum PLL Lock Time | | - | - | 1 | mS |

Note: 1. AC characteristics apply for parallel output termination of 50Ω to $V_{TT}$. Parameters are guaranteed by characterization and are not 100% tested.
2. $V_{CMR}$ (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the $V_{CMR}$ range and the input swing lies within the $V_{PP}$ (AC) specification. Violation of $V_{CMR}$ or $V_{PP}$ impacts static phase offset t(φ).

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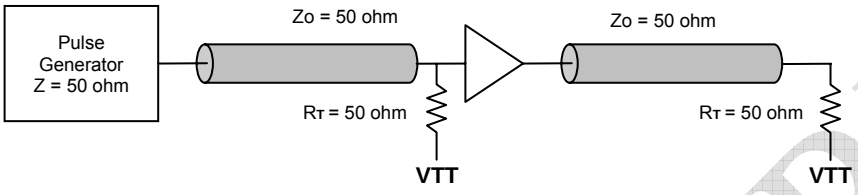


**Figure 1. LVCMOS_CLK AC Test Reference for $V_{DD}$ = 3.3V / 2.5V**

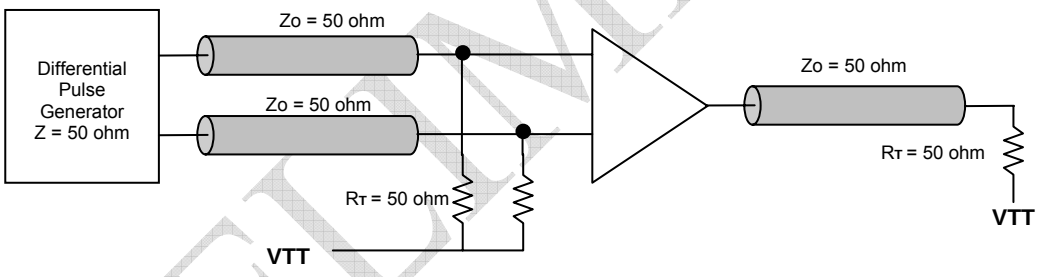


**Figure 2. PECL_CLK AC Test Reference for $V_{DD}$ = 3.3V / 2.5V**

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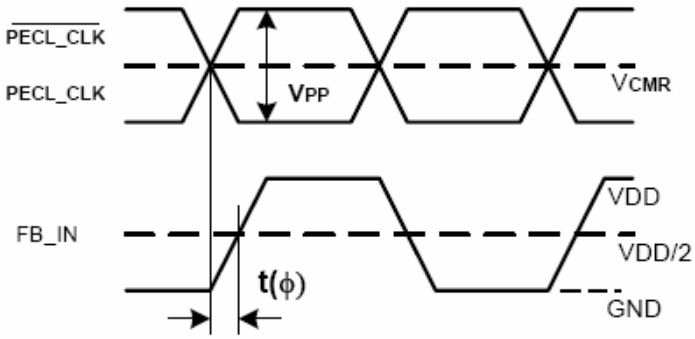



Figure 3. LVPECL Propagation Delay t(f), static phase offset

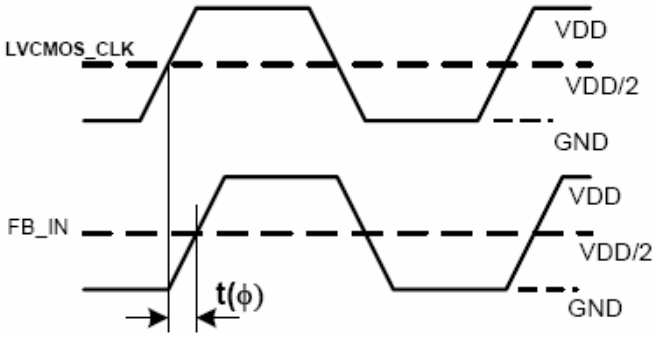
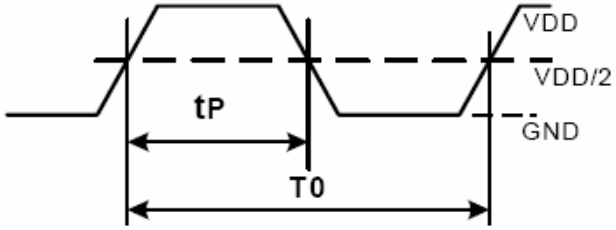



Figure 4. LVCMOS Propagation Delay t(ϕ), static phase offset




DC = tP / T0 x 100%

Figure 5. Output Duty Cycle (DC)

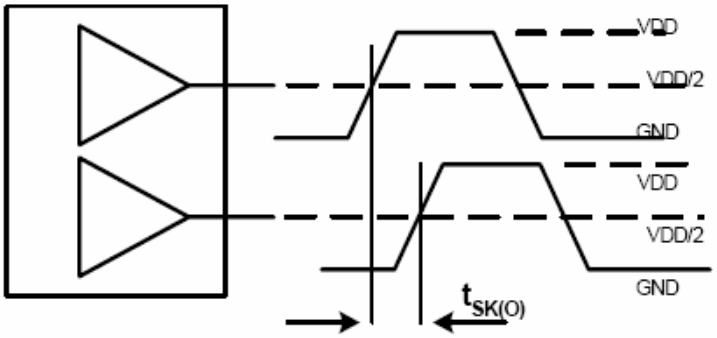



Figure 6. Output-to-Output Skew, $t_{sk(O)}$



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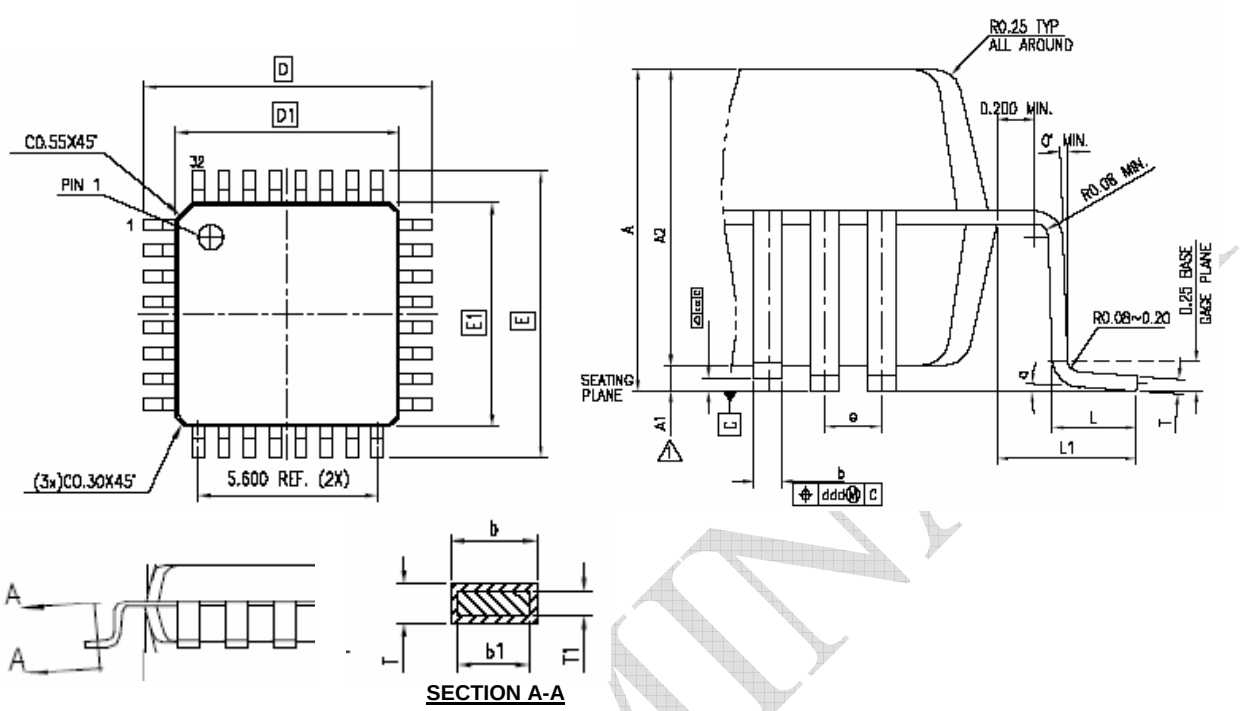
## Package Diagram

**32-lead TQFP Package**




SECTION A-A

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | … | 0.0472 | … | 1.2 |
| A1 | 0.0020 | 0.0059 | 0.05 | 0.15 |
| A2 | 0.0374 | 0.0413 | 0.95 | 1.05 |
| D | 0.3465 | 0.3622 | 8.8 | 9.2 |
| D1 | 0.2717 | 0.2795 | 6.9 | 7.1 |
| E | 0.3465 | 0.3622 | 8.8 | 9.2 |
| E1 | 0.2717 | 0.2795 | 6.9 | 7.1 |
| L | 0.0177 | 0.0295 | 0.45 | 0.75 |
| L1 | 0.03937 REF | | 1.00 REF | |
| T | 0.0035 | 0.0079 | 0.09 | 0.2 |
| T1 | 0.0038 | 0.0062 | 0.097 | 0.157 |
| b | 0.0118 | 0.0177 | 0.30 | 0.45 |
| b1 | 0.0118 | 0.0157 | 0.30 | 0.40 |
| R0 | 0.0031 | 0.0079 | 0.08 | 0.2 |
| a | 0° | 7° | 0° | 7° |
| e | 0.031 BASE | | 0.8 BASE | |

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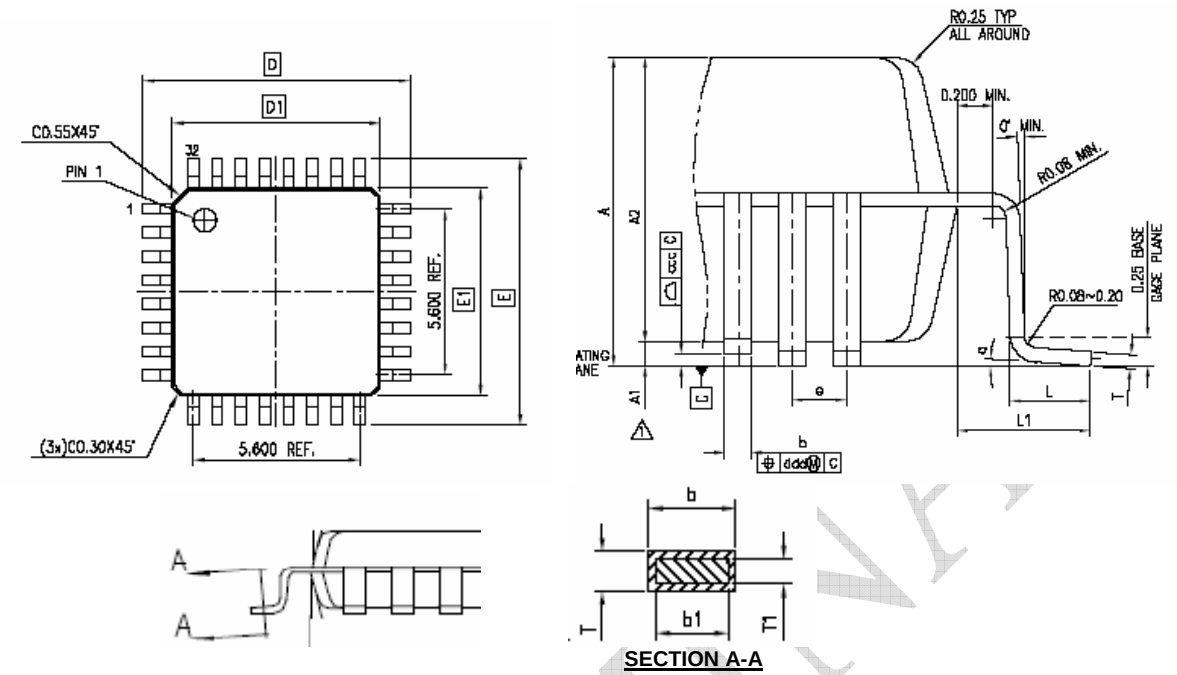
## 32-lead LQFP Package




SECTION A-A

| Symbol | Dimensions | | | |
|---|---|---|---|---|
| | Inches | | Millimeters | |
| | Min | Max | Min | Max |
| A | …. | 0.0630 | … | 1.6 |
| A1 | 0.0020 | 0.0059 | 0.05 | 0.15 |
| A2 | 0.0531 | 0.0571 | 1.35 | 1.45 |
| D | 0.3465 | 0.3622 | 8.8 | 9.2 |
| D1 | 0.2717 | 0.2795 | 6.9 | 7.1 |
| E | 0.3465 | 0.3622 | 8.8 | 9.2 |
| E1 | 0.2717 | 0.2795 | 6.9 | 7.1 |
| L | 0.0177 | 0.0295 | 0.45 | 0.75 |
| L1 | 0.03937 REF | | 1.00 REF | |
| T | 0.0035 | 0.0079 | 0.09 | 0.2 |
| T1 | 0.0038 | 0.0062 | 0.097 | 0.157 |
| b | 0.0118 | 0.0177 | 0.30 | 0.45 |
| b1 | 0.0118 | 0.0157 | 0.30 | 0.40 |
| R0 | 0.0031 | 0.0079 | 0.08 | 0.20 |
| e | 0.031 BASE | | 0.8 BASE | |
| a | 0° | 7° | 0° | 7° |

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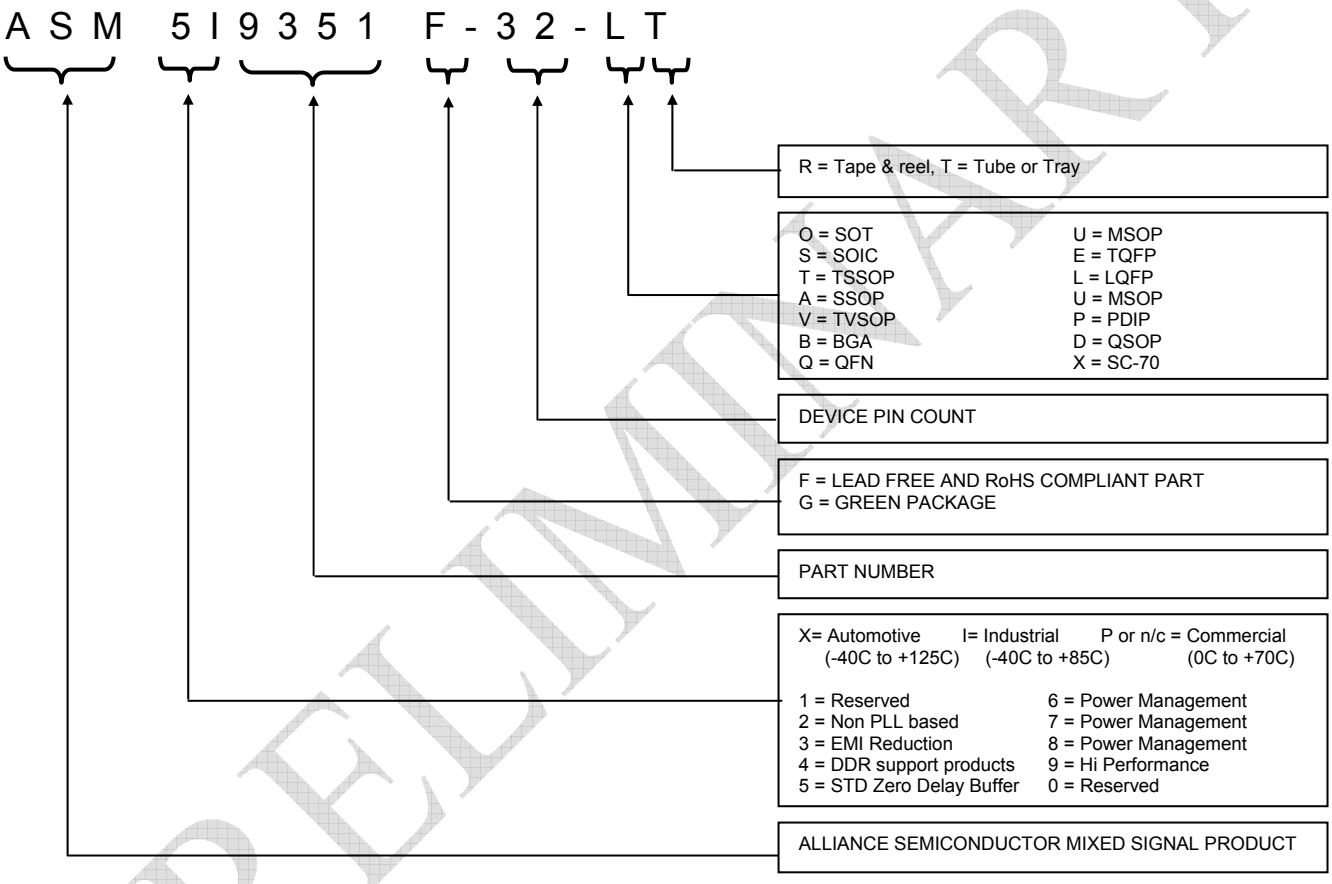
**rev 0.2**

## Ordering Information

| Part Number | Marking | Package Type | Temperature |
|---|---|---|---|
| ASM5I9351-32-ET | ASM5I9351 | 32-pin TQFP | Industrial |
| ASM5I9351-32-LT | ASM5I9351 | 32-pin LQFP –Tape and Reel | Industrial |
| ASM5I9351G-32-ET | ASM5I9351G | 32-pin TQFP, Green | Industrial |
| ASM5I9351G-32-LT | ASM5I9351G | 32-pin LQFP –Tape and Reel, Green | Industrial |

## Device Ordering Information

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