Universal Hexadecimal Counter

AVAILABLE AS MILITARY SPECIFICATIONS

• MIL-STD-883, Paragraph 1.2.2 Compliant

GENERAL DESCRIPTION

The AS10H536 is a high speed synchronous hexadecimal counter. This MECL 10H part which is a functional/pinout duplication of the standarad MECL 10K family part, with 100% improvement in propagation delay, and no increase in powersupply current.

FEATURES

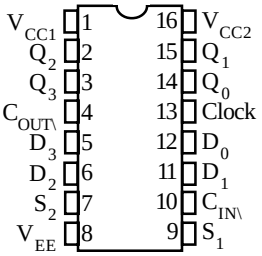
• Counting frequency, 250 MHz minimum
• 900 mW Max/Pkg (No Load)
• Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
• Voltage Compensated
• MECL 10K-Compatible
• Available in a 16-pin DIP package (C designator), CDIP2-T16 per MIL-STD-1835 and in a 16-pin Flatpack (F designator), CDFP4-F16 per MIL-STD-1835.

BURN-IN CONDITIONS:

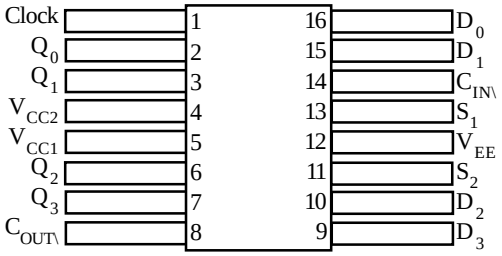
V_{TT} = -2.0V MAX/ -2.2V MIN
V_{EE} = -5.7V MAX/ -5.2V MIN

PIN ASSIGNMENT
(Top View)

16-Pin Side Brazed DIP
(C Designator)



16-Pin Bottom Brazed FP
(F Designator)



Function Select Table			
C_{IN}\	S_1	S_2	Operating Mode
Don't Care	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
Don't Care	H	H	Hold (Stop Count)

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PIN ASSIGNMENTS (Ceramic DIP)

FUNCTION	PIN #	BURN-IN (CONDITION C)
V_{CC1}	1	GND
Q_2	2	51 Ω to V_{TT}
Q_3	3	51 Ω to V_{TT}
C_{OUT}\	4	51 Ω to V_{TT}
D_3	5	GND
D_2	6	GND
S_2	7	OPEN
V_{EE}	8	V_{EE}
S_1	9	OPEN
C_{IN}\	10	OPEN
D_1	11	GND
D_0	12	GND
CLK	13	CP1
Q_0	14	51 Ω to V_{TT}
Q_1	15	51 Ω to V_{TT}
V_{CC2}	16	GND

PIN ASSIGNMENTS (Ceramic FP)

FUNCTION	PIN #	BURN-IN (CONDITION C)
CLK	1	CP1
Q_0	2	51 Ω to V_{TT}
Q_1	3	51 Ω to V_{TT}
V_{CC2}	4	GND
V_{CC1}	5	GND
Q_2	6	51 Ω to V_{TT}
Q_3	7	51 Ω to V_{TT}
C_{OUT}\	8	51 Ω to V_{TT}
D_3	9	GND
D_2	10	GND
S_2	11	OPEN
V_{EE}	12	V_{EE}
S_1	13	OPEN
C_{IN}\	14	OPEN
D_1	15	GND
D_0	16	GND

ORDERING INFORMATION

EXAMPLE: AS10H536C16MIL

Device Number	Package Type	Pin Count	Process*
AS10H536	C	16	MIL
AS10H536	F	16	MIL

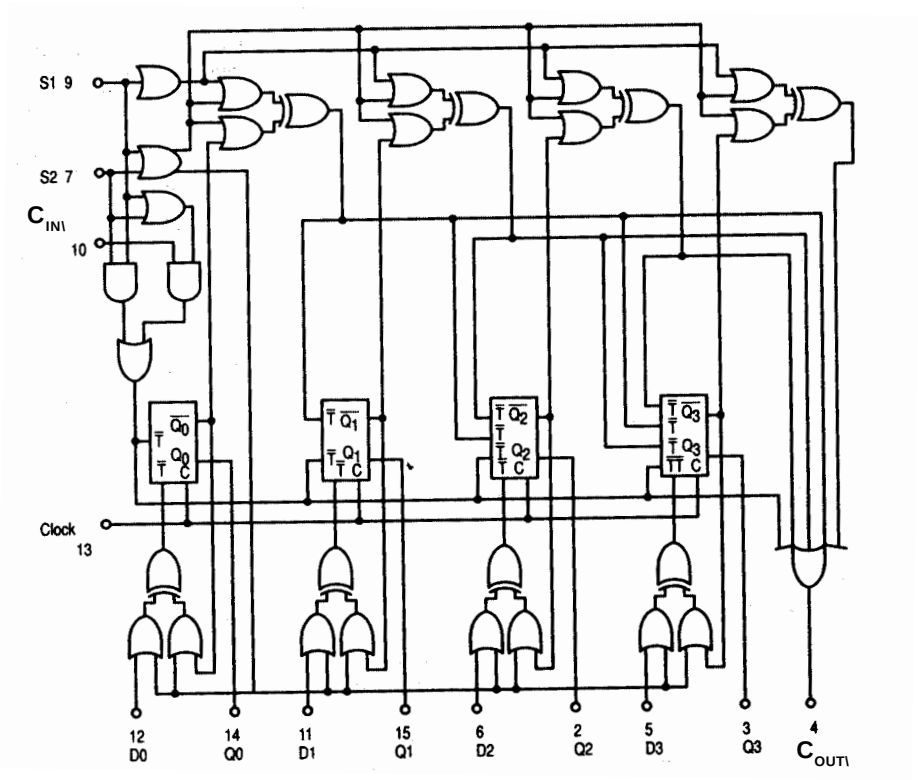
***AVAILABLE PROCESSES**

MIL = Military Processing -55°C to +125°C

SEQUENTIAL TRUTH TABLE •												
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{\text{Carry IN}}$	Clock ••	Q_0	Q_1	Q_2	Q_3	$\overline{\text{Carry OUT}}$
L	L	L	L	H	H	Ø	H	L	L	H	H	L
L	H	Ø	Ø	Ø	Ø	L	H	H	L	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	L	H	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	H	H	H	L
L	H	Ø	Ø	Ø	Ø	H	L	H	H	H	H	H
L	H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	H	H	H	H
L	L	H	H	L	L	Ø	H	H	H	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	H	H	H	H	H

Ø = Don't Care
● Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
●● A clock H is defined as a clock input transition from a low to a high logic level.

FIGURE 1. Logic Diagram



NOTES: Flip flops will toggle when all T\ inputs are LOW.

QUIESCENT LIMIT TABLE*

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

SYM	PARAMETER	LIMITS						UNITS	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Paramters:	+25°C		+125°C		-55°C			Pinouts referenced are for DIP Package, Check Pin Assignments V_{CC}=0V, Output Load=100Ω to -2.0V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		MIN	MAX	MIN	MAX	MIN	MAX		V_{IH1}	V_{IL1}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.046	-1.819	-0.899	-0.692	-1.099	-0.882	V	3-6, 11-14	13		8	1, 16	2, 3, 4, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.592	-1.95	-1.578	-1.95	-1.623	V	13	13		8	1, 16	2, 3, 4, 14, 15
V_{OH1}	High Output Voltage	-1.046	-0.819	-0.899	-0.692	-1.099	-0.882	V			8	8	1, 16	2, 3, 4, 14, 15
V_{OL1}	Low Output Voltage	-1.95	-1.592	-1.95	-1.578	-1.95	-1.623	V			8	8	1, 16	2, 3, 4, 14, 15
I_{EE}	Power Supply Current	-149		-164		-164		mA				8	1, 16	8
I_{IH}	Input Current High		225		365		365	µA	9			8	1, 16	10 C_{IN}\
I_{IH1}	Input Current High		260		415		415	µA	10			8	1, 16	5, 6, 11, 12, 13 CLK, D_0-D_3
I_{IH2}	Input Current High		320		520		520	µA	5, 6, 11-13			8	1, 16	7 S2
I_{IH3}	Input Current High		405		655		655	µA	7			8	1, 16	9 S1
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5-7, 10-13	8		1, 16	5, 6, 11 - 13

QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
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T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay														
	Clk to Q	0.7	3.2	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
	Clk to $\overline{\text{Carry Out}}$	0.7	7.0	0.7	7.7	0.7	7.7	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	0.7	3.0	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
t_{SET}	Setup Time														
	Data (D_0 to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Select (S to C)	3.5		3.5		3.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Carry In ($\overline{C_{IN}}$ to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	(C to $\overline{C_{IN}}$)	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
t_{HOLD}	Hold Time														
	Data (D_0 to C)	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Select (S to C)	-0.5		-0.5		-0.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Carry In ($\overline{C_{IN}}$ to C)	150		150		150		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	(C to $\overline{C_{IN}}$)	2.0		2.2		2.2		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
f_{Count}	Count Frequency	250		250		250		MHz	12	13	9		1, 16	8	3, 14