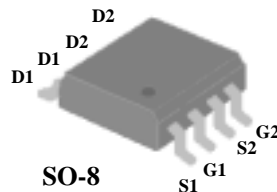


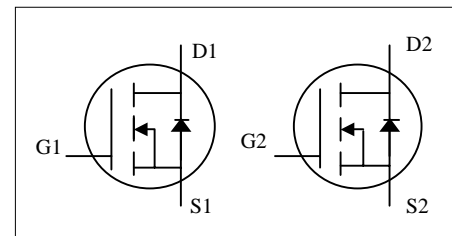
- ▼ Low On-Resistance
- ▼ Simple Drive Requirement
- ▼ Dual N MOSFET Package



$BV_{DSS}$	30V
$R_{DS(ON)}$	22m $\Omega$
$I_D$	7.8A

### Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current <sup>3</sup>	7.8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current <sup>3</sup>	6.2	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	30	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ C$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 62.5	$^\circ C/W$



**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.02	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =7A	-	-	22	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	-	-	32	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =7A	-	12	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =70°C)	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =7A	-	13	21	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =24V	-	3	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	9	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =15V	-	10	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =1A	-	7	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	22	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =15Ω	-	8	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	720	1150	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	230	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	200	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.2	1.8	Ω

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =1.7A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =7A, V <sub>GS</sub> =0V,	-	16	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	8	-	nC

**Notes:**

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤10sec ; 135 °C/W when mounted on Min. copper pad.

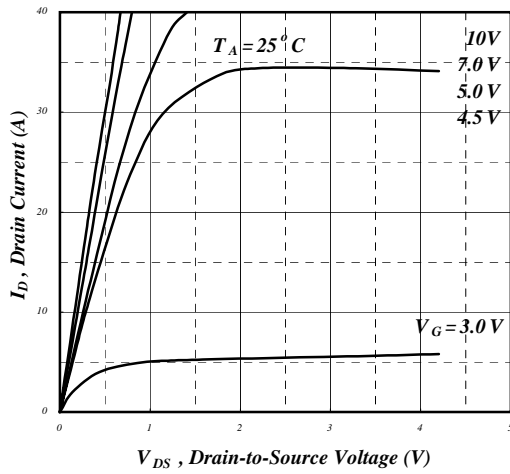


Fig 1. Typical Output Characteristics

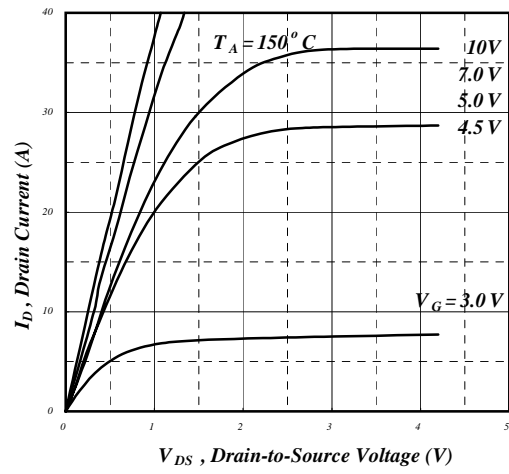


Fig 2. Typical Output Characteristics

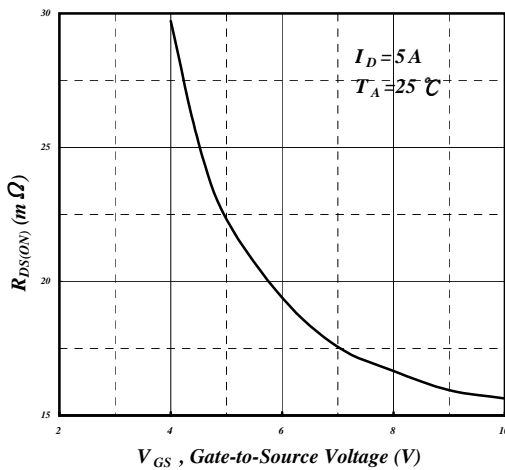


Fig 3. On-Resistance v.s. Gate Voltage

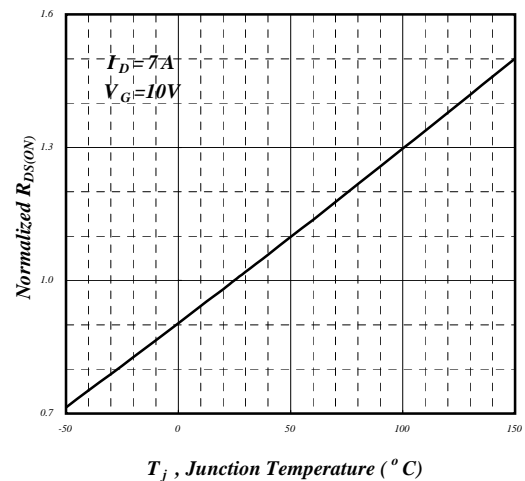


Fig 4. Normalized On-Resistance v.s. Junction Temperature

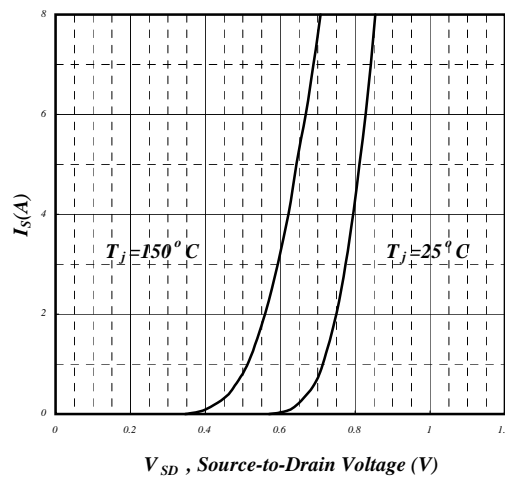


Fig 5. Forward Characteristic of Reverse Diode

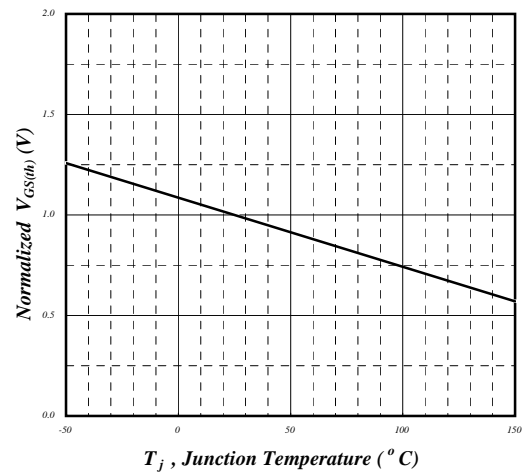


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

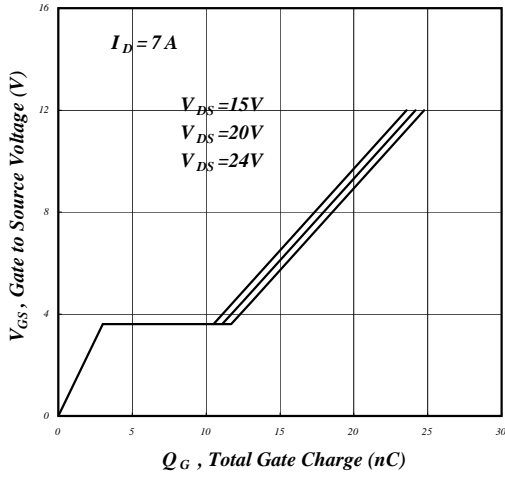


Fig 7. Gate Charge Characteristics

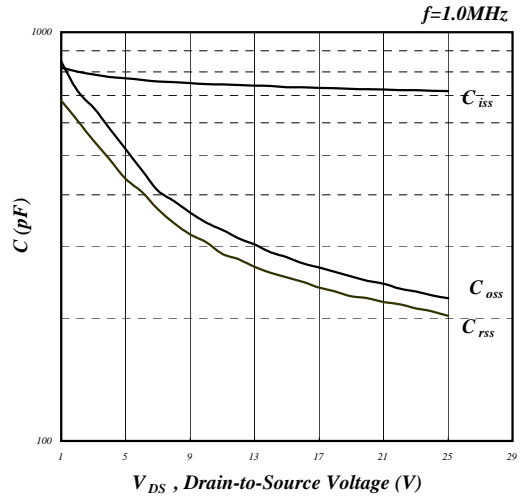


Fig 8. Typical Capacitance Characteristics

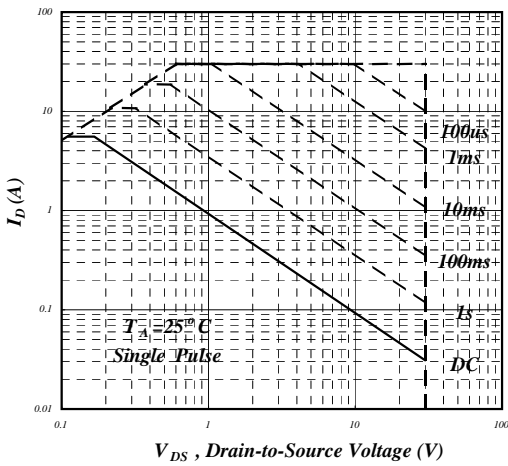


Fig 9. Maximum Safe Operating Area

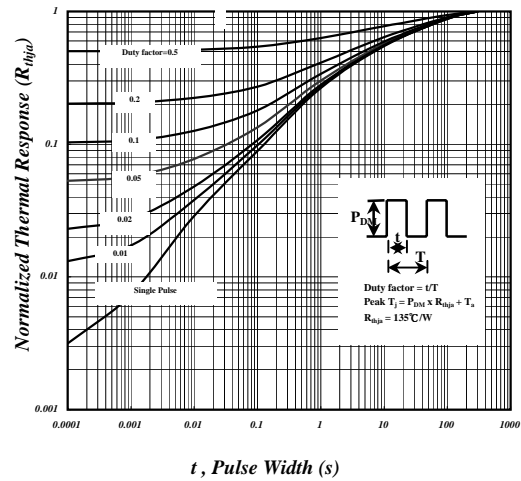


Fig 10. Effective Transient Thermal Impedance

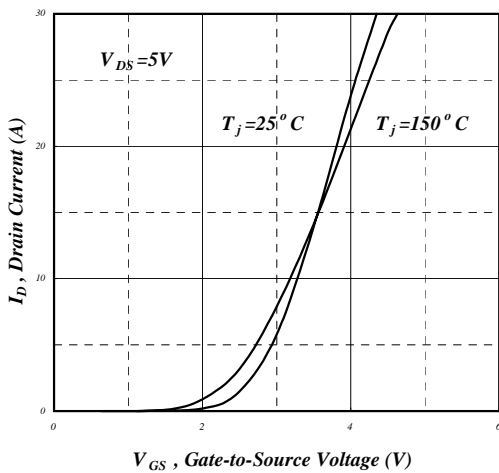


Fig 11. Transfer Characteristics

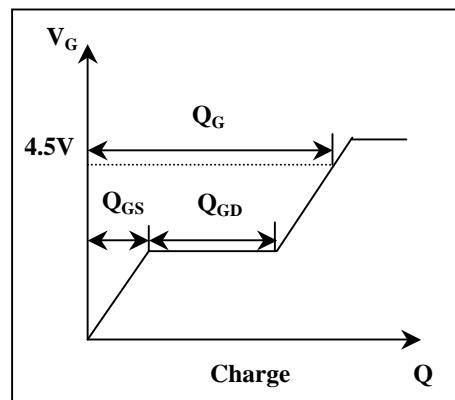


Fig 12. Gate Charge Waveform