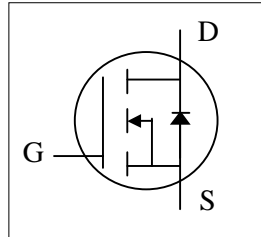




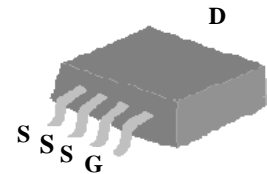
- ▼ SO-8 similar area footprint and pin assignment
- ▼ Low Gate Charge
- ▼ Fast Switching Speed
- ▼ RoHS Compliant



$BV_{DSS}$	30V
$R_{DS(ON)}$	6m $\Omega$
$I_D$	75A

## Description

The APAK-5 package is preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



**APAK-5**

## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	75	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	55	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	300	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation	62.5	W
	Linear Derating Factor	0.5	W/ $^\circ C$
$E_{AS}$	Single Pulse Avalanche Energy <sup>4</sup>	29	mJ
$I_{AR}$	Avalanche Current	24	A
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

## Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 2	$^\circ C/W$
Rthj-a	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 85	$^\circ C/W$



# AP0603GMA

## Electrical Characteristics @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	-	-	V
ΔBV <sub>DSS</sub> /ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.018	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =45A	-	-	6	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =30A	-	-	10	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =30A	-	32	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	uA
	Drain-Source Leakage Current (T <sub>j</sub> =150°C)	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V	-	-	500	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±20V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =30A	-	33	52	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =24V	-	7.5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	24	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =15V	-	11.2	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =30A	-	77	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	35	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =0.5Ω	-	67	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	2700	4200	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	550	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	380	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.9	2.8	Ω

## Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =45A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time <sup>2</sup>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V,	-	28	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI/dt=100A/μs	-	10	-	nC

### Notes:

1. Pulse width limited by safe operating area.
2. Pulse width ≤300us, duty cycle ≤2%.
3. Surface mounted on FR4 board.
4. Starting T<sub>j</sub>=25°C, V<sub>DD</sub>=25V, L=0.1mH, R<sub>G</sub>=25Ω

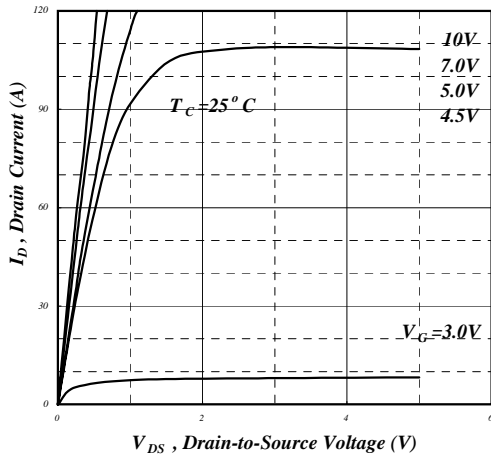


Fig 1. Typical Output Characteristics

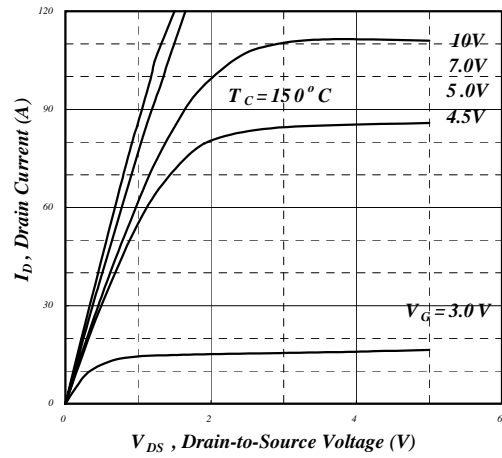


Fig 2. Typical Output Characteristics

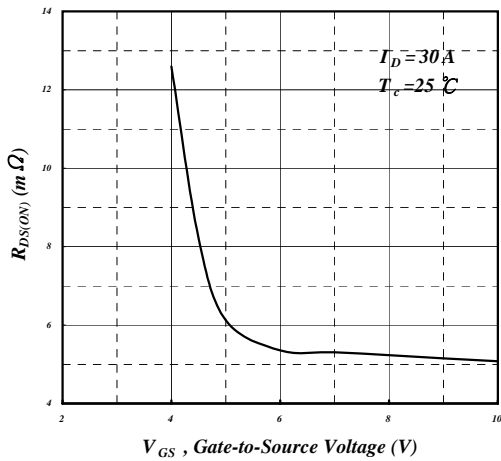


Fig 3. On-Resistance v.s. Gate Voltage

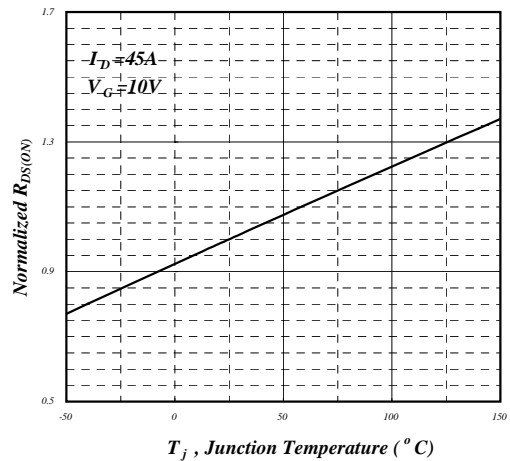


Fig 4. Normalized On-Resistance v.s. Junction Temperature

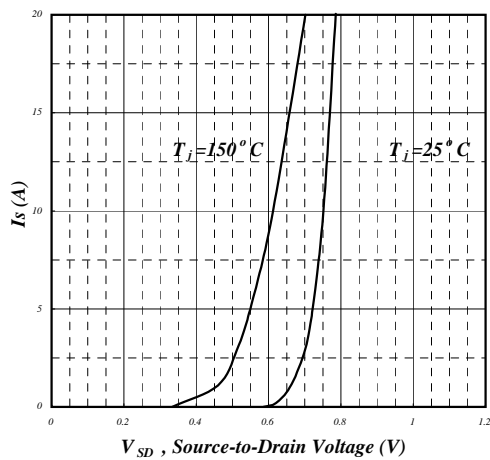


Fig 5. Forward Characteristic of Reverse Diode

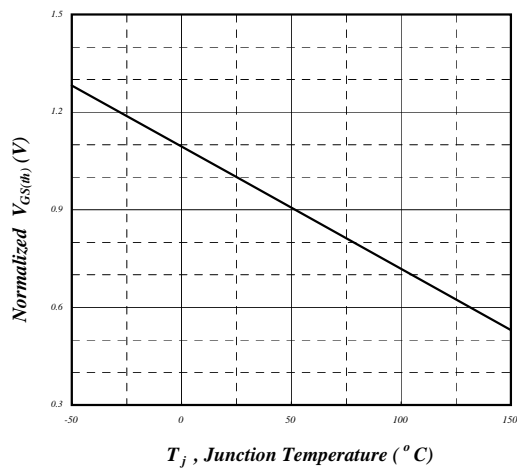


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

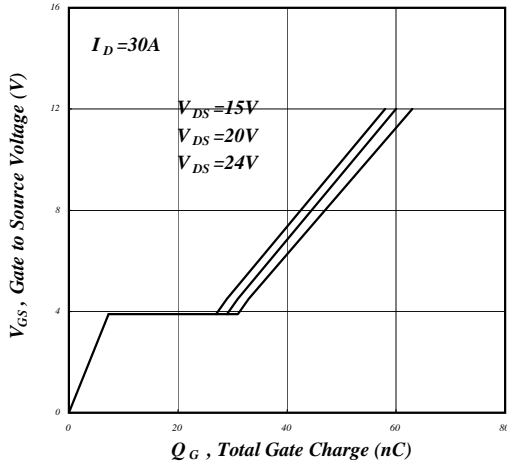


Fig 7. Gate Charge Characteristics

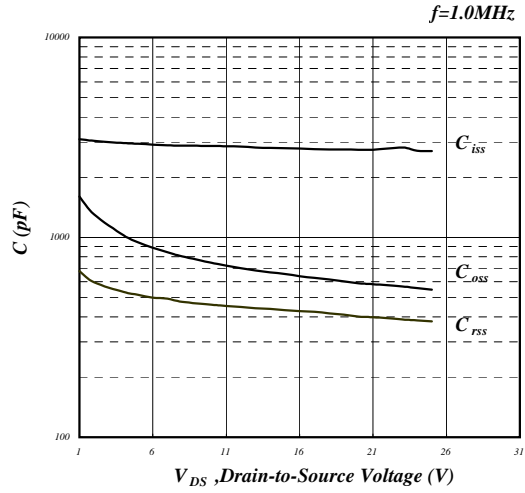


Fig 8. Typical Capacitance Characteristics

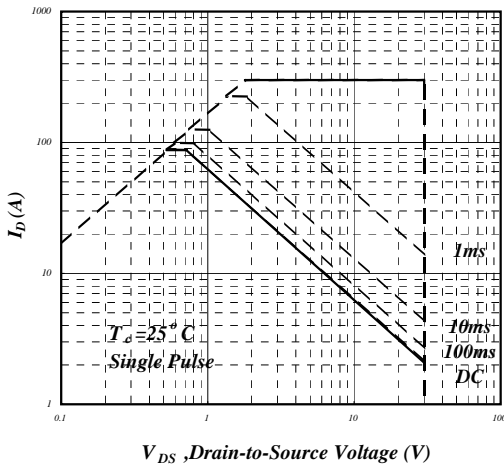


Fig 9. Maximum Safe Operating Area

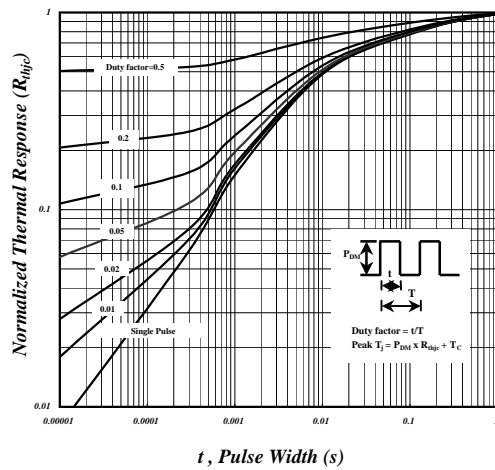


Fig 10. Effective Transient Thermal Impedance

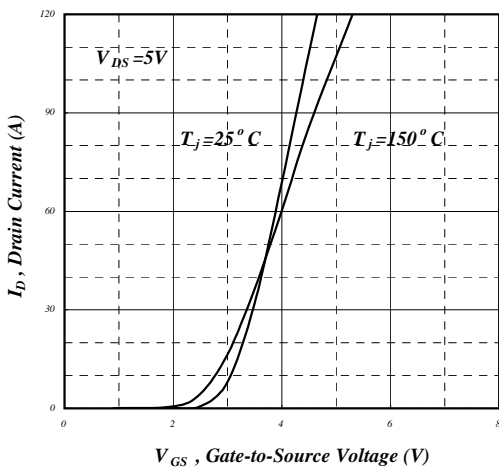


Fig 11. Transfer Characteristics

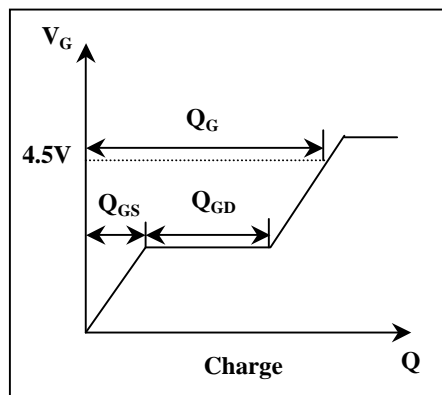


Fig 12. Gate Charge Waveform