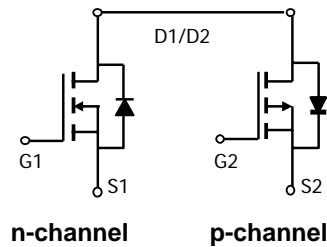
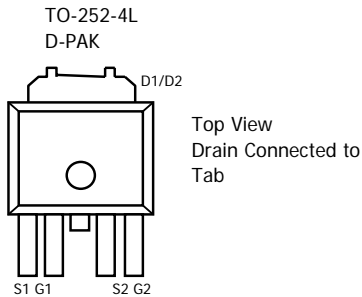



**AOD606**
**Complementary Enhancement Mode Field Effect Transistor**
**General Description**

The AOD606 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard product AOD606 is Pb free (meets ROHS & Sony 259 specifications). AOD606L is a Green Product ordering option. AOD606 and AOD606L are electrically identical.*

**Features**

n-channel	p-channel
$V_{DS} (V) = 40V$	-40V
$I_D = 8A (V_{GS}=10V)$	-8A ( $V_{GS} = -10V$ )
$R_{DS(ON)}$	$R_{DS(ON)}$
< 33 m $\Omega$ ( $V_{GS}=10V$ )	< 50 m $\Omega$ ( $V_{GS} = -10V$ )
< 47 m $\Omega$ ( $V_{GS}=4.5V$ )	< 70 m $\Omega$ ( $V_{GS} = -4.5V$ )


**Absolute Maximum Ratings  $T_A=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	40	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	8	8	A
$T_C=25^\circ C$		8	8	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	-30	
Avalanche Current <sup>C</sup>	$I_{AR}$	8	-8	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	20	30	mJ
Power Dissipation <sup>B</sup>	$P_D$	20	50	W
		$T_C=100^\circ C$	10	
Power Dissipation <sup>A</sup>	$P_{DSM}$	2	2.5	W
		$T_A=70^\circ C$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	-55 to 175	$^\circ C$

**Thermal Characteristics: n-channel and p-channel**

Parameter	Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	n-ch	17.4	30	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>		n-ch	50	60	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	n-ch	4	7.5	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	p-ch	16.7	25	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A</sup>		p-ch	40	50	$^\circ C/W$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	p-ch	2.5	3	$^\circ C/W$

N-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$ , $V_{GS}=0\text{V}$	40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1	2.3	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=8\text{A}$		27	33	m $\Omega$
		$T_J=125^\circ\text{C}$		39	52	
		$V_{GS}=4.5\text{V}$ , $I_D=6\text{A}$		37	47	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=8\text{A}$		25		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.76	1	V
$I_S$	Maximum Body-Diode Continuous Current				8	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=20\text{V}$ , $f=1\text{MHz}$		404		pF
$C_{oss}$	Output Capacitance			95		pF
$C_{rss}$	Reverse Transfer Capacitance			37		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		2.7		$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=20\text{V}$ , $I_D=8\text{A}$		9.2		nC
$Q_g(4.5\text{V})$	Total Gate Charge			4.5		nC
$Q_{gs}$	Gate Source Charge			1.6		nC
$Q_{gd}$	Gate Drain Charge			2.6		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=10\text{V}$ , $V_{DS}=20\text{V}$ , $R_L=2.5\Omega$ , $R_{GEN}=3\Omega$		3.5		ns
$t_r$	Turn-On Rise Time			6		ns
$t_{D(off)}$	Turn-Off DelayTime			13.2		ns
$t_f$	Turn-Off Fall Time			3.5		ns
$t_{rr}$	Body Diode Reverse Recovery Time		$I_F=8\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		22.9	
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=8\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		18.3		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300 \mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

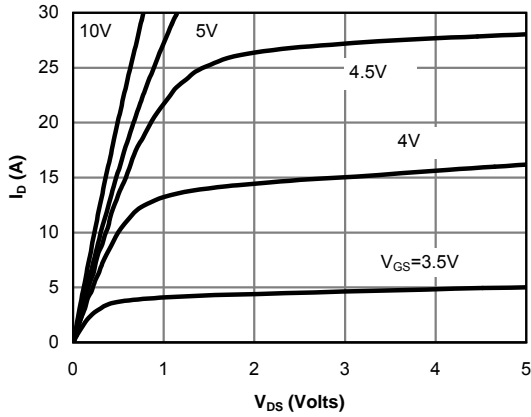
G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

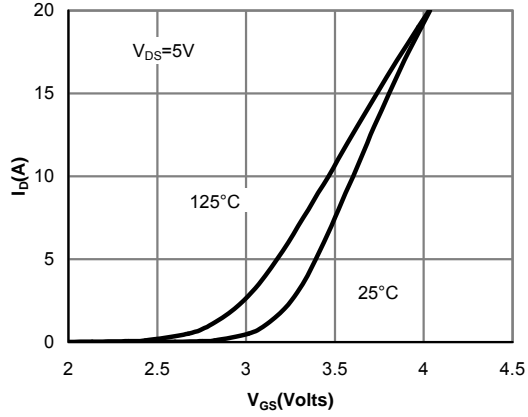
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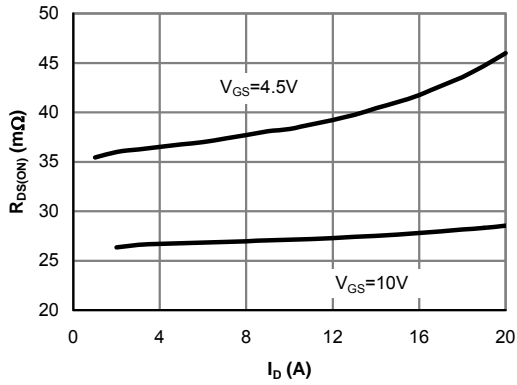
**N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



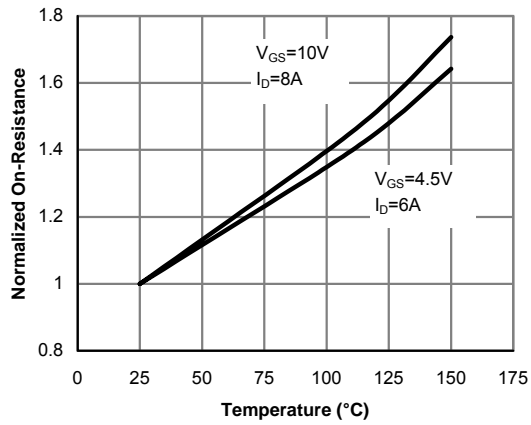
**Fig 1: On-Region Characteristics**



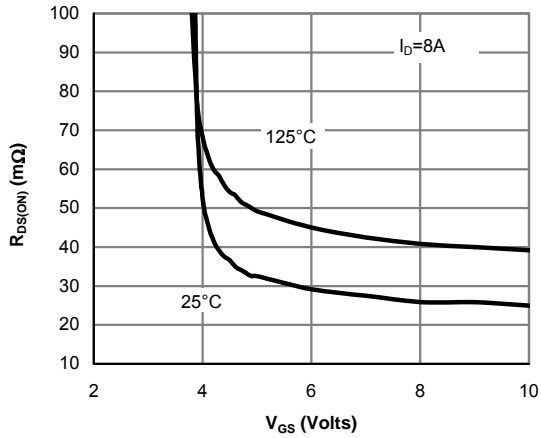
**Figure 2: Transfer Characteristics**



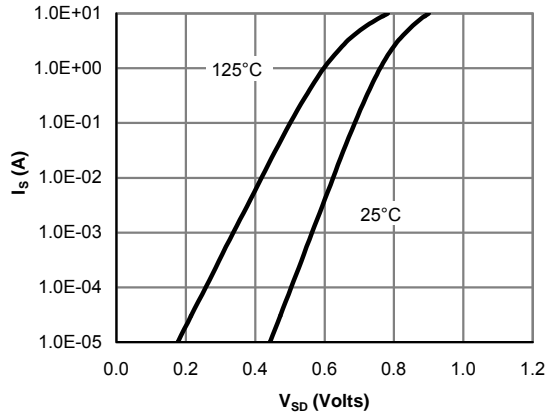
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

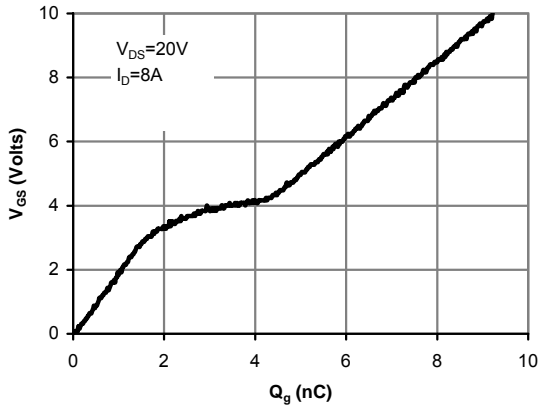


Figure 7: Gate-Charge Characteristics

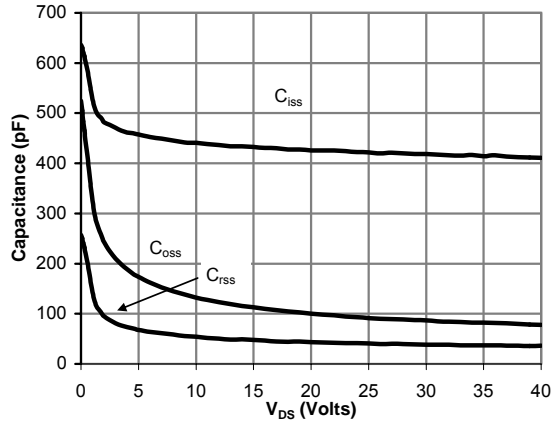


Figure 8: Capacitance Characteristics

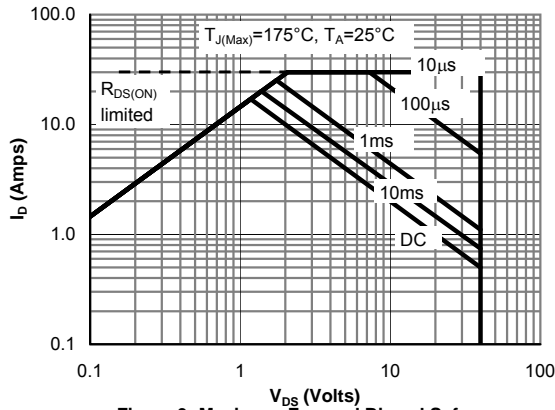


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

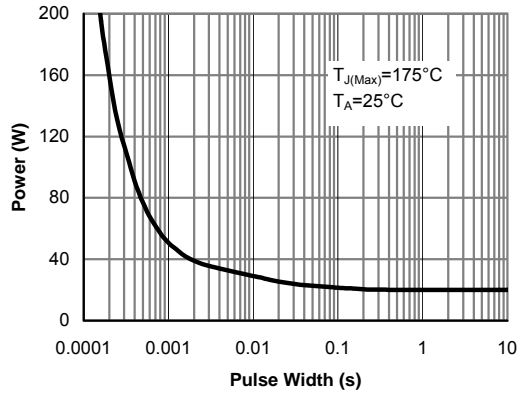


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

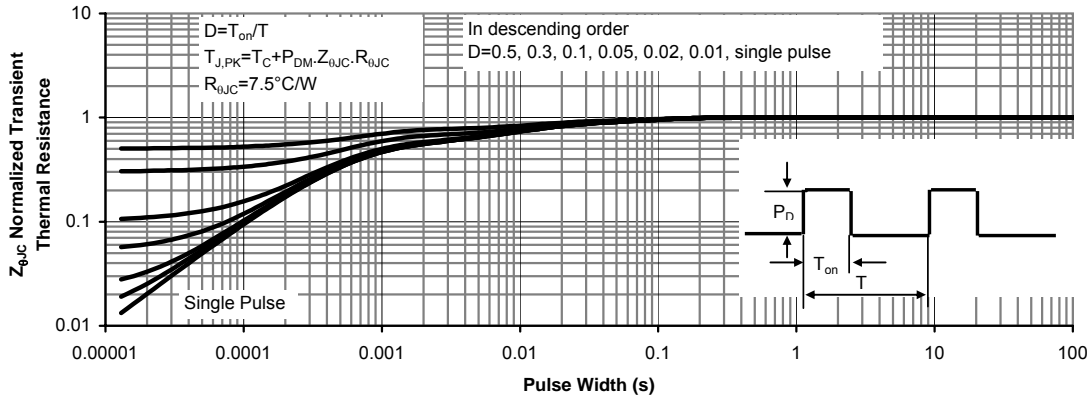


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

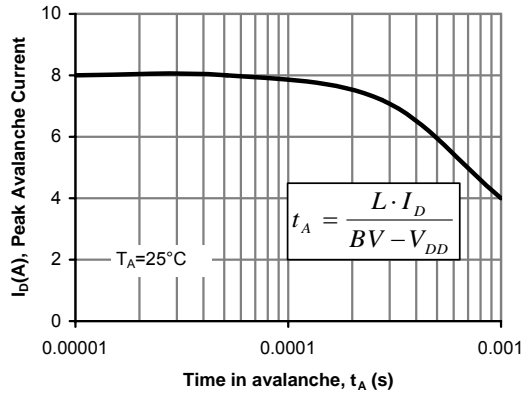


Figure 12: Single Pulse Avalanche capability

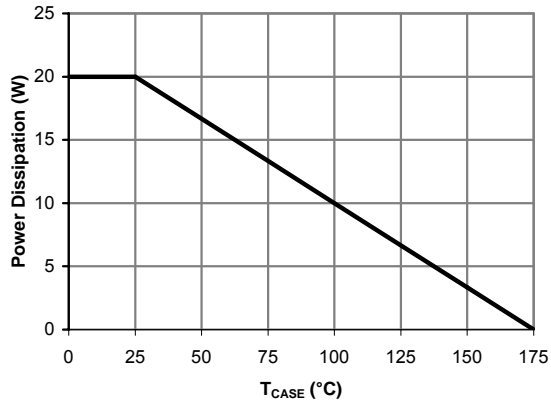


Figure 13: Power De-rating (Note B)

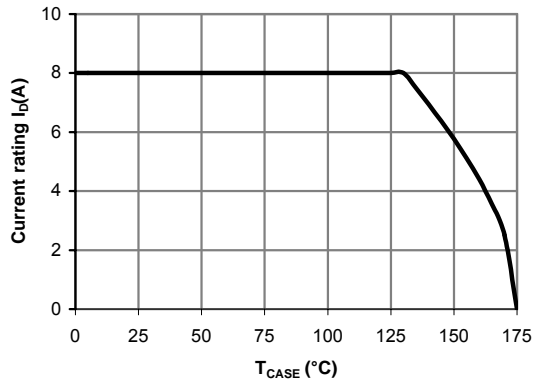


Figure 14: Current De-rating (Note B)

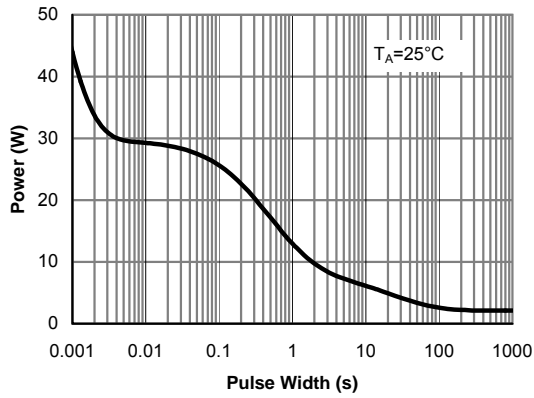


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

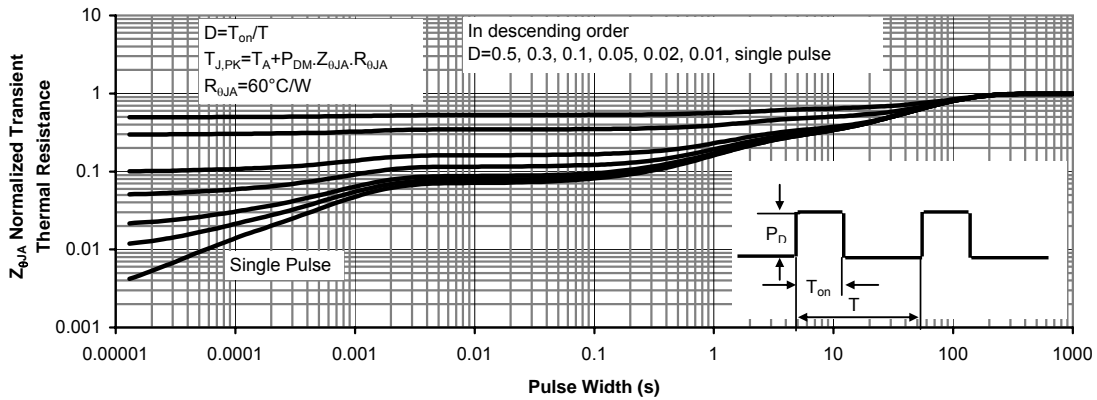


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-32V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.8	-3	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-30			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-8A T <sub>J</sub> =125°C		35 62	50	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4A		55	70	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-8A		16		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.75	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				-8	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-20V, f=1MHz		657		pF
C <sub>oss</sub>	Output Capacitance			143		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			63		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		6.5		Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge (10V)	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-8A		14.1		nC
Q <sub>g</sub> (4.5V)	Total Gate Charge (4.5V)			7		nC
Q <sub>gs</sub>	Gate Source Charge			2.2		nC
Q <sub>gd</sub>	Gate Drain Charge			4.1		nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =2.5Ω, R <sub>GEN</sub> =3Ω		8		ns
t <sub>r</sub>	Turn-On Rise Time			12.2		ns
t <sub>D(off)</sub>	Turn-Off Delay Time			24		ns
t <sub>f</sub>	Turn-Off Fall Time			12.5		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time		I <sub>F</sub> =-8A, dI/dt=100A/μs		23.2	
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-8A, dI/dt=100A/μs		18.2		nC

A: The value of R<sub>qJA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation PDSM is based on R<sub>qJA</sub> and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on T<sub>J</sub>(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J</sub>(MAX)=175°C.

D: The R<sub>qJA</sub> is the sum of the thermal impedance from junction to case R<sub>qJC</sub> and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J</sub>(MAX)=175°C.

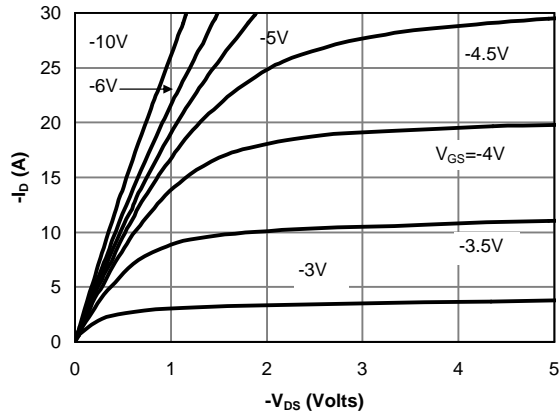
G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

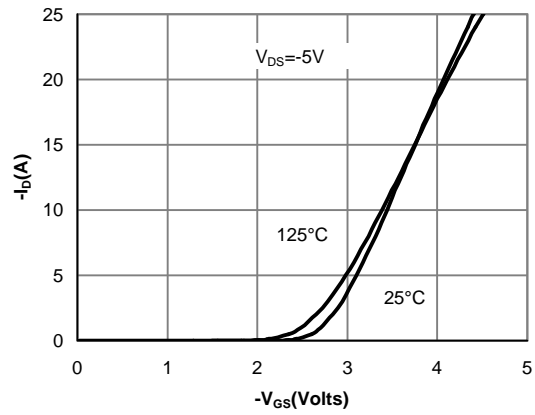
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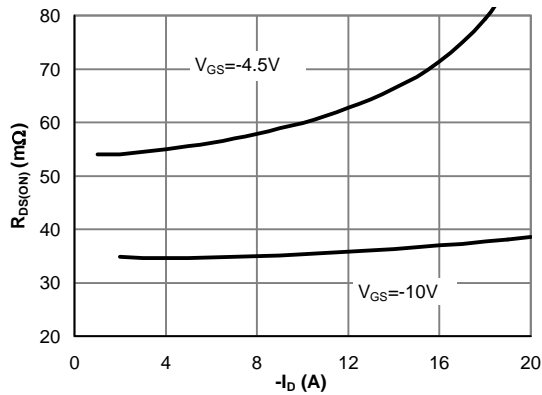
**P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)**



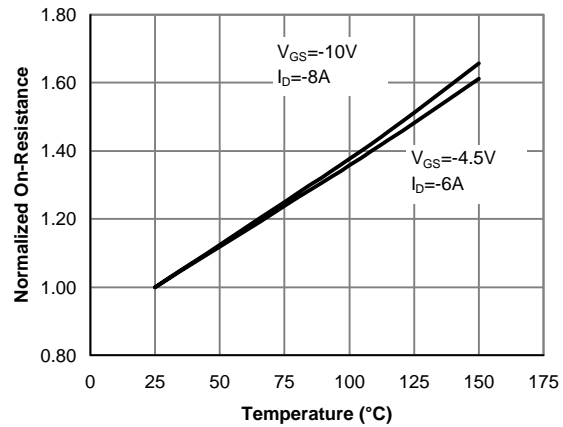
**Fig 1: On-Region Characteristics**



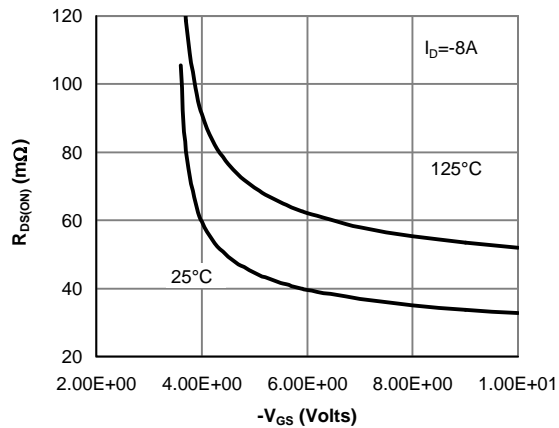
**Figure 2: Transfer Characteristics**



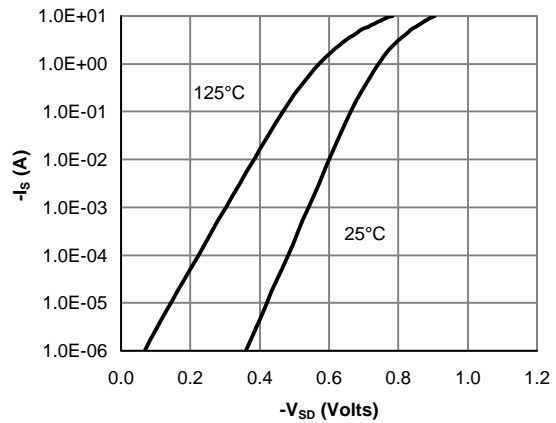
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**



**Figure 4: On-Resistance vs. Junction Temperature**



**Figure 5: On-Resistance vs. Gate-Source Voltage**



**Figure 6: Body-Diode Characteristics**

P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

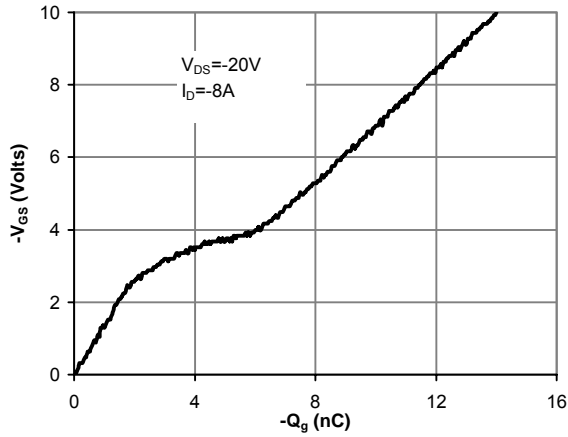


Figure 7: Gate-Charge Characteristics

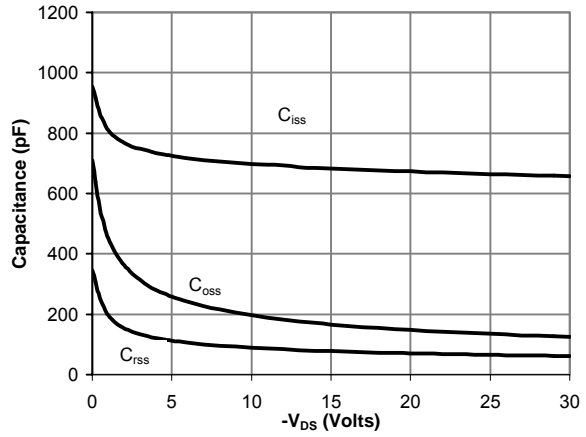


Figure 8: Capacitance Characteristics

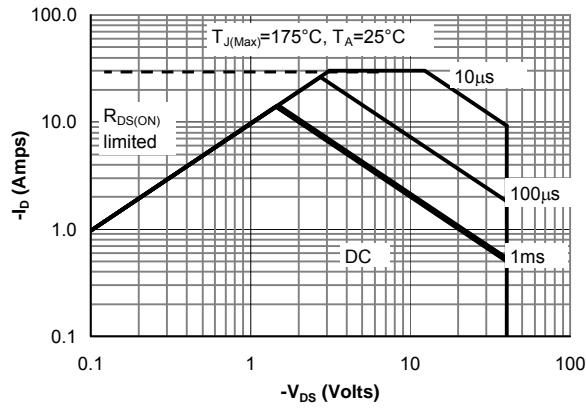


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

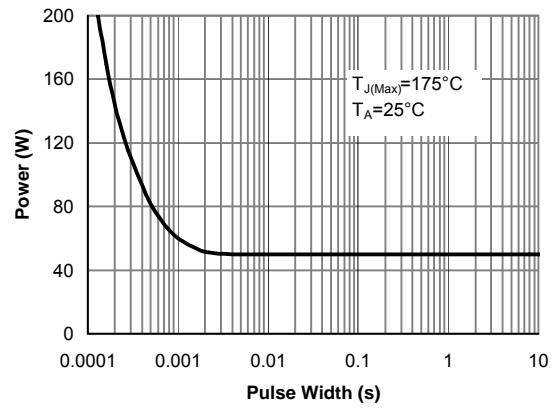


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

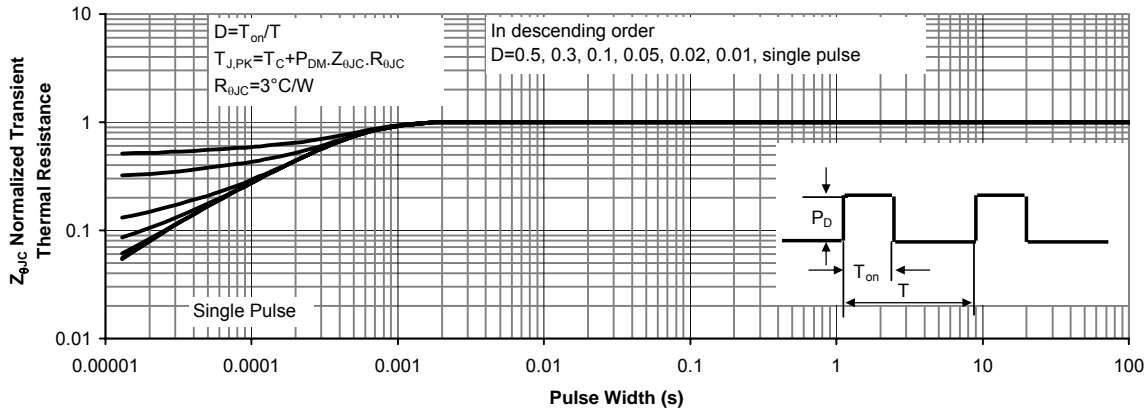


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

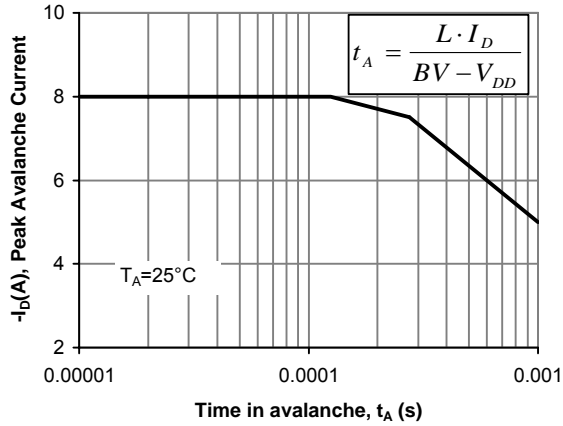


Figure 12: Single Pulse Avalanche capability

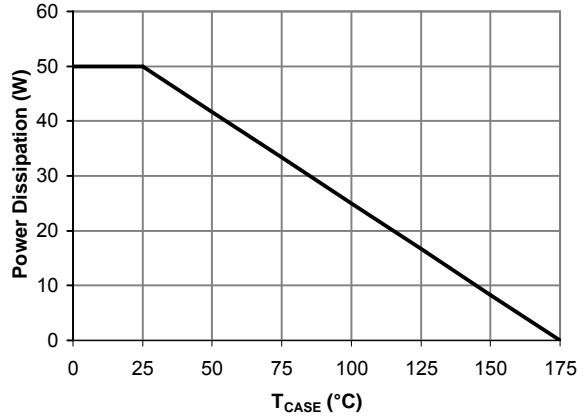


Figure 13: Power De-rating (Note B)

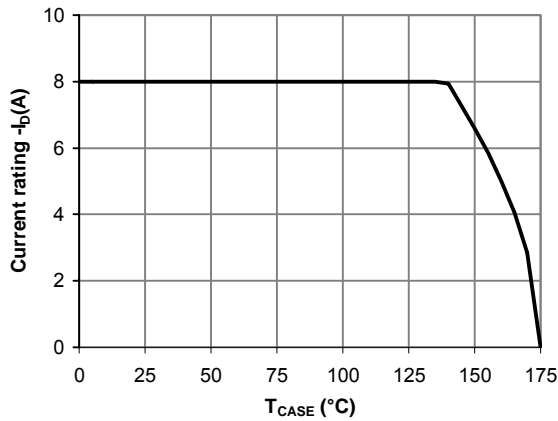


Figure 14: Current De-rating (Note B)

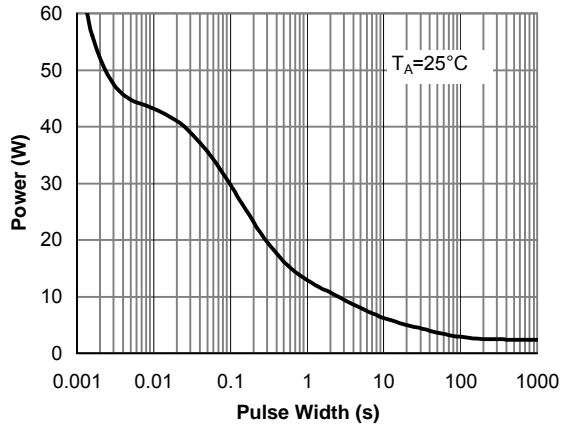


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

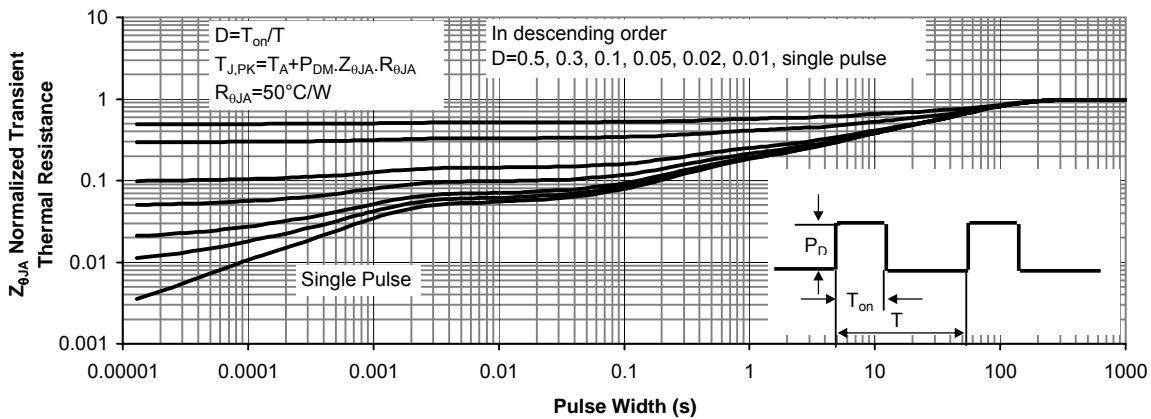


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)