1.0 Description

AMI Semiconductor's AMIS-720639 (PI3039) contact image sensor (CIS) sensor chip is a linear array image sensor chip with a 600 elements per inch resolution. The sensor chip is fabricated with AMI Semiconductor's proprietary CMOS image sensing technology. Since this image sensor chip is intended for CIS module applications, multiple numbers of these sensors will be serially cascaded to form a linear scanning image array of arbitrary length. These sensors are butted end-to-end on a printed circuit board (PCB). The sensors are mounted using the chip-on-board technology to form scanning arrays with various lengths.

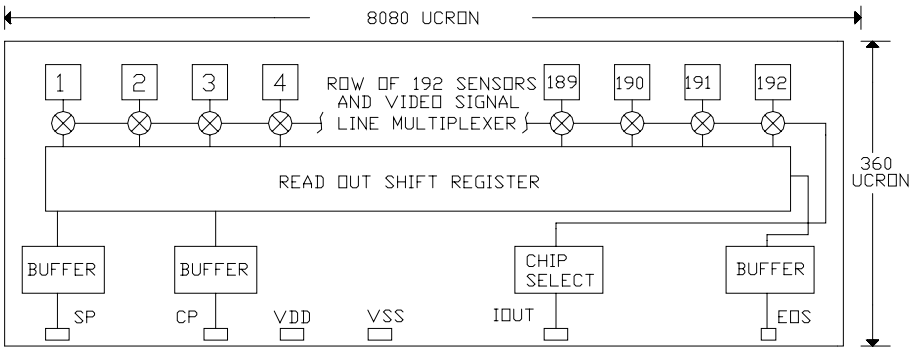
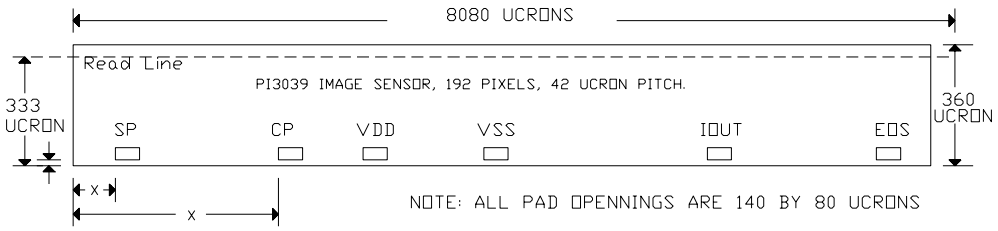


Figure 1: AMIS-720639 Sensor Block Diagram

Figure 1 is a block diagram of the sensor chip. Each sensor chip consists of 192 detector elements, their associated multiplexing switches, buffer amplifiers and a chip selector. The detector's element-to-element spacing is approximately 42µm. The size of each chip without the scribe lines is 8080µm by 360µm and each sensor chip has six bonding pads. The pad symbols and functions are described in Table 1.

Table 1: Pad Symbols and Functions

Symbol	Function
SP	Start pulse: input to start the line scan
CP	Clock pulse: input to clock the shift register
VDD	Positive supply: +5V supply connected to substrate
VSS	VSS is tied to ground: connection topside common
IOUT	Video signal current output from a source follower
EOS	End-of-scan pulse: output from the shift register at end-of-scan



PAD	FUNCTION	Y	X
SP	START INPUT	30	575
CP	CLOCK INPUT	30	2195
VDD	+5 SUPPLY	30	3295
VSS	TIED TO GROUND	30	4373
IOUT	VIDEO SIGNAL OUT	30	5495
EOS	SCAN OUTPUT	30	7272

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATION ARE GIVEN IN THE TABLE
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENNING
5. ALL DIMENSIONS ARE IN UCRON

Figure 2: Bonding Pad Layout Diagram:

Figure 2 shows the bonding pad locations for the AMIS-720639 sensor chip. The locations are referenced to the lower left corner of the die.

2.0 Electro-Optical Characteristics (25°C)

Table 2 lists the electro-optical characteristics of the AMIS-720639 sensor chip at 25°C.

Table 2: Electro-Optical Characteristics

Parameters	Symbols	Typical	Units	Notes
Number of photo-elements		192	Elements	
Pixel-to-pixel spacing		42	µm	
Chip scanning rate	Tint (1)	38.4	µsec	@ typical 5MHz pixel rate See Note 2
Clock frequency	fclk (2)	5.0	MHz	See Note 2
IOUT (saturation charge output for a given sample time) At 5.0MHz clock frequency	Qsat (3)	170 to 200	pC	With 570nm light source. At saturation exposure of 5.7Joules/cm^2
Video voltage output from an A4 size CIS module, AMIS-710620-A4 (PI620MC-A4) (four tapped outputs, for high speed application)	Vpavg (4)	1.0 0.300	V V	Using a red LED source Using a Yellow-Green LED source, at minimum integration time ≅ 277µsec @ 5MHz clock rate
Output voltage non-uniformity	Up (5)	± 7.5	%	Test circuit used only the amplifier of Note 4
Chip-to-chip non-uniformity	Ucc	± 7.5	%	Test circuit used only the amplifier in Note 4
Dark output voltage	Vd (6)	<50	mV	Test circuit see Note 4
Dark output non-uniformity	Ud (6)	<20	mV	Test circuit see Note 4

Notes:

(1) Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two SPs at the maximum clock rate of 6.5MHz, Tint = 29.5µsec.

(2) fclk stands for the input clock frequency; maximum operating frequency is 6.5MHz.

(3) There are three types of signal outputs that are called out in the table (see Section 7.0). The referenced section discusses each of the video output circuits. Two are defined for pulsed current, or charge processing, (see Figure 5 or Figure 7). The third is voltage output circuit, specified for most CIS applications because of its lower cost and simpler implementation advantages (see Figure 6).

(4) Specified for CIS application is a circuit with a buffer amplifier that interfaces the video output (see Figure 6).This typical video output line is terminated with a commonly used standard op-amp circuit. It is located in Section 7.0. The AMIS-710227 (PI227MC-A4) CIS module, employing this type of output circuit, was used in the measurements.
Note: A LED light source is an integral part of the module.

(5) Up is the uniformity specification. It is measure with the image sensor exposed under a uniform light source.
Up = [(Vpmax-Vpavg)/Vpavg]x100%
Or [(Vpavg-Vpmin)/Vpavg]x100%, which ever is greater.
Where Vpavg = ∑Vpn/Npixels
   a. Vpn is the nth pixels of sensor chip.
   b. Npixels is the total number of pixels in sensor chip.
   c. Vpmax is the maximum pixel output voltage in the light.
   d. Vpmin is the minimum pixel output voltage in the light.
Note: In the light means the sensor is exposed to the light.

(6) Video output in dark: Vd = ∑Vdn/Npixels
Note: In the dark means that sensor are placed on dark target and measured with the light off.

(7) Uniformity in the dark: Ud = (Vdmax-Vdmin)
   a. Vdmax is the maximum pixel output voltage in the dark.
   b. Vdmin is the minimum pixel output voltage in the dark.

3.0 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameters	Symbol	Maximum Rating	Units
Power supply voltage	VDD	7.0	V
Power supply current	IDD	<3.0	ma
Input clock pulse (high level)	Vih	Vdd + 0.5	V
Input clock pulse (low level)	Vil	-0.25	V

4.0 Environmental Ratings

Table 4: Environmental Ratings

Parameters	Symbol	Maximum Rating	Units
Operating Temperature	Top	0 to 50	°C
Operating humidity	Hop	10 to 85	RH %
Storage temperature	Tstg	-25 to 75	°C
Storage humidity	Hstg	10 to 90	RH %

5.0 Operating Range at Room Temperature

Table 5: Recommended Operating Conditions at Room Temperature

Parameters	Symbols	Min.	Typical	Max.	Units
Power supply	VDD	4.5	5.0	5.5	V
Input clock pulses high level	Vih (1)	4.0	5.0	VDD	V
Input clock pulse low level	Vil (1)	0	0	0.8	V
Video signal current (charge for given sample time)	Iout (2)		See Note 2		
Clock frequency	fclk (3)(4)	0.1	5.0	6.5	MHz
Clock pulse duty cycle	Dty (5)		50		%
Clock pulse high durations	Tw		100		nsec
Integration time	Tint (6)	29.54			µsec
Operating temperature	Top		25	50	°C

Notes:

(1) Applies to both CP and SP.

(2) See Note 3 under Table 2.

(3) Although the clock frequency will operate the device at less than 100kHz, it is recommended that the device be operated above 500kHz. This recommendation is for long module length, such as the A4 size with 27 sequentially cascaded sensors. The long module at low clock rates has a long scan time. This results in a long photo integration time that generates leakage currents. The leakage currents randomly store arbitrary amounts of charges in the photo-site, contributing to the FPN in the dark.

(4) For fclk < 5.0MHz, the clock duty cycle is typically 25 percent. But at fclk = 5.0MHz or higher a typical of 50 percent is recommended. This is to keep the die-to-die, fixed pattern noise (FPN), to a minimum between die transitions in CIS operation.

(5) Duty cycle is the ratio of clock pulse width over the clock period.

(6) Tint at the minimum integration time is specified with a maximum clock frequency of 6.5MHz. This specification is for a single sensor. When multiple sensors are cascaded in series, this minimum integration time increases with each additional number of sensors.

6.0 Switching Characteristics at 25°C

Since these image sensors are applied in a multiple-length line array with a wide range in scanning speeds, two types of output video amplifiers are used. Three video output circuits are discussed in Section 7.0. There are only two basic types of video output circuits. One is a current sensing amplifier and the other is a charge storing buffer amplifier. Simplified block diagrams show their interface connections with the image sensors. They were also used to measure the specifications given in this data sheet. The timing relationships among these two different video signals and the image sensor's two input clocks, its SP, its shift register clock (CP) and its shift register output (EOS), are shown in two diagrams, Figure 3 and its supplement, Figure 4. The two timing diagrams are accompanied with two tables of timing symbol's specification. These symbols graphically define the timing relationships among the waveforms in the timing diagrams; see Figure 3. The switching specifications are given in Table 6. Except for the analog video output, the rest are digital clock waveforms. Their levels are +5V CMOS compatible. The video signal, Iout, timing is specified in Table 6. Its amplitude was specified in Table 2.

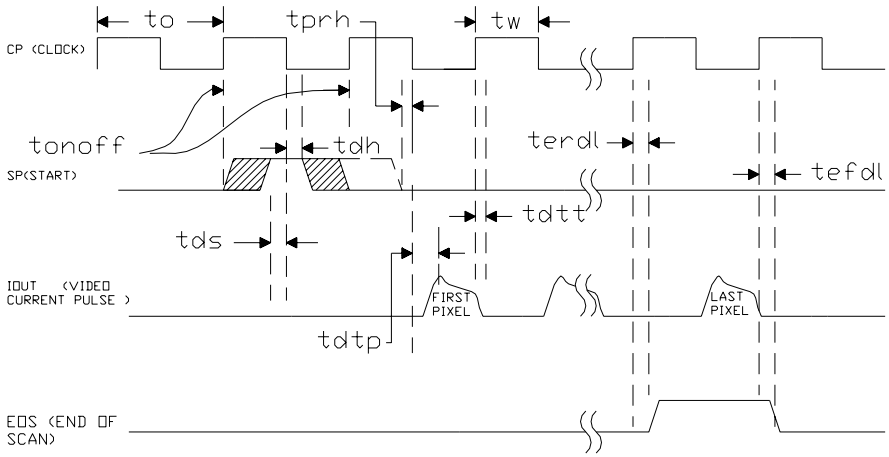


Figure 3: Timing Diagram of the AMIS-720639 Sensor

Table 6: Timing Symbol's Definition

Item	Symbol	Min.	Mean	Max.	Units
Clock cycle time	to (1)	154		10000	ns
Clock pulse width	tw (2)	77			ns
Clock duty cycle	Dty (3)	25	50	75	%
Data setup time	tds	20			ns
Data hold time	tdh	20			ns
Prohibit crossing time	Tprh (4)		20		ns
SP turn on and off	Tonoff(5)				Note 5
EOS rise delay	terdl		80		ns
EOS fall delay	tefdl		75		ns
Signal delay time to peak	tdtp(6)		20		ns
Signal fall time delay	tftd(6)		80		ns

Notes:

(1) Minimum is specified at the maximum clock frequency of 6.5MHz.

(2) Since the clock pulse width varies with frequency, tw will vary according to duty cycle. This minimum is specified at 6.5MHz and 50 percent duty cycle.

(3) The clock duty cycle typically is 25 percent. At 5.0MHz or higher 50 percent is recommended. This recommendation is to keep the die-to-die FPN to a minimum between die transitions in CIS operation.

(4) Tprh is the time where the SP high is prohibited. No consecutive falling clock edges are allowed during one cycle of SP. Otherwise, two SPs or more will load into the shift register for each negative going clock edge. Multiple SPs loaded into the shift register will access proportional numbers of multiple pixels simultaneously at each clock cycle.

(5) The recommended time to start and stop the SP is between two consecutive rising clock edges, indicated by the tonoff arrows.

(6) These values, tdtp and tftd, are measurements from the circuit in Figure 6, which is essentially the pulse voltage across the 50Ω resistor. This is one of the circuits employed to convert the video signal current to voltage. See the discussion on the two amplifier configurations in Section 7.0.

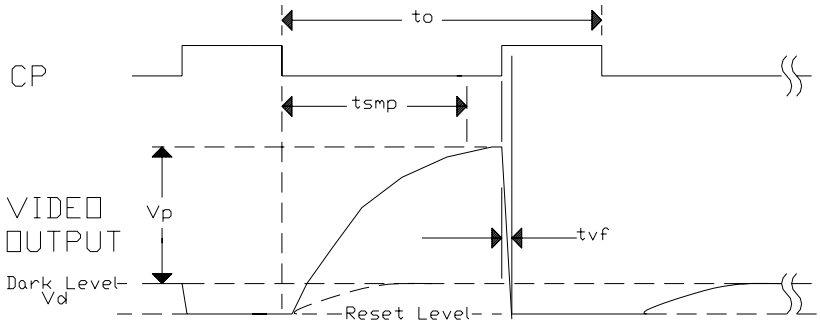


Figure 4: Supplement Timing Diagram

This supplementary timing diagram, Figure 4, graphically defines the symbols used to describe the timing relationship between the waveforms at the output of the voltage buffer amplifier. The accompanying Table 7 is shown below.

Cp is the same clock that is shown in Figure 3. As in the Figure 3, it is the reference for defining the video signal pulse times. Vp is the peak amplitude of the pixel when the image sensor is under light exposure. Vd is the dark level of the pixel when the image sensor has no light exposure. The reset level is used during the time when image sensor is reset to ground with an external shunting switch, SW. Refer to any of the simplified block diagrams in Section 7.0. The video line reset is active while Cp is high. The video signal charges the video line with the falling edge of Cp.

The shape of the video is a typical characteristic that is exhibited when the sensor current charges the video line capacitance. It continues to rise until it becomes asymptotic to a horizontal line. However, for a clock frequency >2.0MHz, the slope does not reach the asymptotic condition. Because of this ever-charging slope, the output voltage changes with the clock frequency and its duty cycle. Hence, there is no optimum point for the video pixel sampling position. Using an edge-triggered sampling A/D with a very narrow aperture, the users of these CIS devices sample the signal as close to top of the waveform as possible. Although the optimum way is to adjust the sampling position in the application, the following sampling time given in terms of clock-time ratio will provide a rule-of-thumb in setting the sampling time. By using the relationship below, the user can place the sampling clock within an acceptable range.

$Tsmp \approx [to \times (1.0 - Dty) + Damp]$
where Dty is the clock duty cycle defined in Table 6.

Table 7: Supplement Timing Symbol's Definition

Item	Symbol	Min.	Mean	Max.	Units
Clock pulse period	to[1]	166	200	10000	ns
Video sample time	tsmp [2]	107	120		ns
Amplifier group delay	Damp [3]	15	20		%
Video fall time	tvf	20	30		ns

Notes:
(1) to is the clock cycle period with minimum set with 6.0MHz.
(2) tsmp has been previously defined above, with Dty=0.5.
(3) Damp is group delay time associated with the amplifier design in Figure 7, Video Buffer Amplifier, EL2044 by Elantec.

7.0 Output Circuits for Converting the Video Signals

This section discusses the test methods employed to measure the video performance characteristics of the AMIS-720639 image sensors and serves as a reference for Table 2, Notes 3 and 4. It also serves as an application note for implementing the AMIS-720639 image sensors. The output of each sensor element in the AMIS-720639 image sensor is an emitter of a source. Accordingly, when its video output line is terminated into a low impedance line, such as the current amplifier in Figure 5, the pulsed video signal currents proportional to photon integration time are produced. At a high sampling frequency rate, these video current pulse widths are limited to the pixel sampling time. Hence, the output signal voltage is limited to the signal current pulse time and amplitude. Accordingly, the usual practice is to integrate this small signal charge instead of using a sensing resistor, RFB, (see Figure 5). In this case, RFB can be changed to a capacitor with a reset switch, thus converting the circuit to a Miller Integrator. The integrator will convert the charges to proportional signal voltages. However, the disadvantage to this low-cost application is that the cost is higher than just using a single amplifier and the implementation is more complex. Another disadvantage to this application is that it will require a signal-inverting amplifier if a positive-going signal is desired. But, if kept in this simple resistor feedback form and, if the application can accept an inverted output voltage, this current-to-voltage amplifier can also implement a relatively low cost, simple circuit. Accordingly, it is introduced and discussed as one of the three amplifier structures that can be used for the video output of the AMIS-720639 device. The other amplifiers that will be discussed are configured as simple buffer amplifiers.

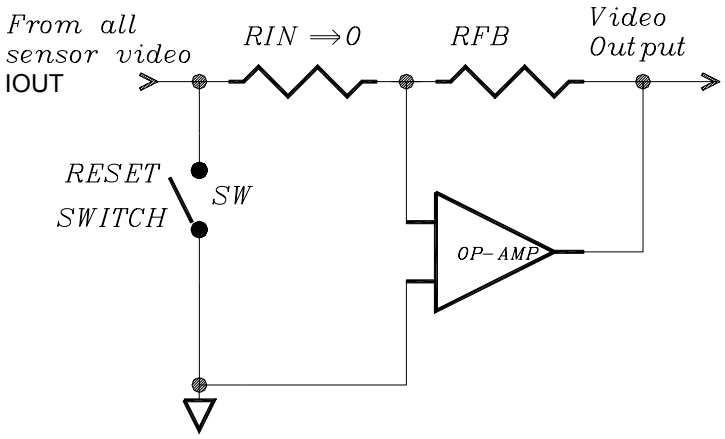


Figure 5: Virtual Ground Amplifier

The first circuit is shown in Figure 5. The signal currents from the photo-site are converted into a voltage signal through its feedback resistor, while the photo-site output sees a very close approximation to a ground because the input resistor value can be small enough to render the video line capacitance negligible, hence providing a fast responding video samples. The first method is to use the video line capacitance as a charge storing capacitance. When the selected sensor's photo-site outputs its video signal current, the video line reset switch, SW, is open. After the video is sampled by the host system, SW closes and resets the video line and the photo-site which are presently under interrogation. Then it opens just prior to the next pixel readout. This reset is active during CP's high state. The disadvantage of this circuit is that it has negative-going output and will have pulse shape of the current impulse that decays over a long period. Hence, it may not be desirable at low clock sample frequencies.

To get around this decaying type of sampling pixels, the second circuit may be more desirable (see Figure 6). This method uses the video line as a storage medium. It uses a buffer amplifier and buffers the video line with its high input impedance. Hence, the video line effectively approaches the condition of an open circuit and becomes a capacitance that is proportional to video line length and geometry. When the photo site produces the signal current, it charges the video line capacitance and converts the output into a voltage signal. The switch, SW, is a video line reset switch. It resets the video line and the photo-site presently under interrogation, just prior to the next pixel readout. This reset is active during CP's high state.

Figure 6, shows the buffer amplifier configuration. The general video wave shape and timing characteristics of this circuit are discussed in Section 6.0. Figure 4 shows the general signal wave shape and its timing relationship to the clock. Table 6 defines the symbols used in Figure 4. This circuit is generally employed in CIS applications where the clock speeds are under 5.0MHz.

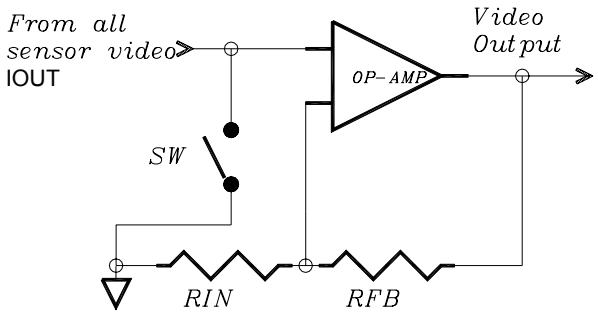


Figure 6: Voltage Buffer Amplifier

This video line charging implementation is extensively used because of its simplicity and low cost, however, speed is limited because of the video line capacitance. For any given video line capacitance, the rate of signal charge remains the same, creating the charging slope. As the sampling frequency is increased, the pixel's signal window decreases, reducing the amplitude and at very high frequency the video sample becomes triangular in shape. This effect is especially prevalent when longer line arrays are implemented. However, the CIS modules are cascaded structures of N Image sensors in series, forming various lengths of line arrays. It is easy to see that as N increases, the length of the video line on the PCB increases, thus increasing the video line capacitance and making it difficult to extract the signal, especially at high speeds.

The third circuit is desirable for high-speed application, specifically, above 5.0MHz. Again, a buffer amplifier is employed. It uses the same buffer stage as in the second circuit. It has a positive-going output buffer amplifier, but instead of applying the video directly to the input of the amplifier, it uses a small shunt-sensing resistor to ground (see Figure 7). In this case, a small 50Ω resistor load, low enough in impedance to allow the image sensor to effectively see a virtual ground, is employed. This low impedance minimizes the effect of video line capacitance. The signal is pulsed out as an impulse current. This signal current produces a fast rising signal voltage across the resistor, then the signal decays at a slightly slower rate. At high clock rates, the time duration is short enough for the impulse current to develop an approximated square wave voltage across the resistor (see Figure 3). Iout, the signal current across the 50Ω is exemplified as a very fast rising and falling signal voltage pulse. The advantage of this circuit is that it is a positive going output signal, which eliminates the need for the second inverter stage. In addition, although it is not recommended for low frequency operation, its low impedance video line lends to high-speed operation, above 5.0MHz. Accordingly, this circuit offers the advantages of high-speed performance in addition to its cost and implementation advantages. The disadvantage to this circuit is that since it senses the output on a 50Ω resistor, the signal-to-noise is slightly less than the circuit that stores the signal charges on the video line.

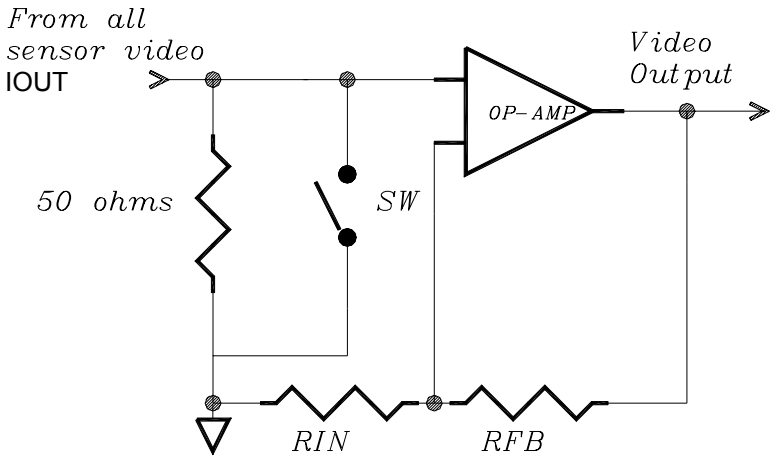


Figure 7: Signal Current to Voltage Converter

8.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our Web site at: http://www.amis.com

North America
Tel: +1.208.233.4690
Fax: +1.208.234.6795

Europe
Tel: +32 (0) 55.33.22.11
Fax: +32 (0) 55.31.81.12