

1.0 General Description

The AMIS-710600-A8 (PI600MC-A8) is a contact image sensor (CIS) module. It is a short version within a family of contact image sensor modules. It consists of image sensor chips, AMIS-720639 (PI3039), which are also a product of AMIS. This AMIS-720639 sensor chip is a linear array image sensor chip with a 600 elements per inch resolution. Fabricated with AMI Semiconductor's proprietary CMOS image sensing technology, these sensors are bonded on a printed circuit board (PCB) to produce the AMIS-710600-A8 CIS modules. Using the chip-on-board technology, seven sensor chips are bonded to the PCB, forming a linear array module of 57mm, with a total of 1344 pixel elements. This 57mm active read length lends itself to scanning A8 size documents with 23.62 dots per millimeter (dpm) resolution. This short array length module was especially designed for applications in card scanners but it is not limited to this specific application. It can be used in various mark readers and other automation equipment requiring narrow scanning modules.

2.0 Key Features

- Light source, lens and sensor are integrated into a single module
- 23.62dpm resolution, 57mm scanning length
- Up to 390 μ sec/line scanning speed, with 3.5MHz pixel rate
- Wide dynamic range
- Analog output
- Yellow-Green LED light source
- Compact size \cong 12mm x 15mm x 70mm
- Low power
- Light weight

3.0 Functional Description

As described in the previous section, the AMIS-710600-A8 imaging array consists of seven image sensors. Each solid-state sensor contains an integrated array of photo-detectors with their associated multiplex switches and a digital shift register, to sequentially readout each video pixel from its photo-detector. Seven of these integrated array sensors are bonded on the PCB and sequentially cascaded to form a CIS line array of 1344 pixel elements. Since each sensor has I/O pads for the shift register start pulse (SP) and the end-of-scan pulse (EOS); each preceding sensor's EOS in the sequence loads into the following sensor's SP, providing for a continuously scanning array each time the first sensor's SP in the sequence is loaded. These sequential video pixels from each sensor are summed on to a common video line, which terminates into a common buffer amplifier. The output of the amplifier produces the output video pixels from the module (see Figure 1).

The PCB is enclosed in the module housing along with its associated electro-optical components, to form a self-contained imaging system. Its array sensors are optically aligned and mounted along with a one-to-one graded indexed micro lens array, which focuses the image from the scanned documents onto the sensing plane of its array. Its light source is specially fabricated and aligned with the micro lens and its document to form a completely integral CIS imaging system.

The enclosed module has a cover glass with its surface near or on the focal point for the object being scanned, while it serves to protect the imaging sensors, the micro lens assembly and the LED light source from contaminants in the environment, such as dust. The I/O to the module is a 10-pin connector located on one end of the module. Figure 2 shows a cross section of the AMIS-710600-A8.

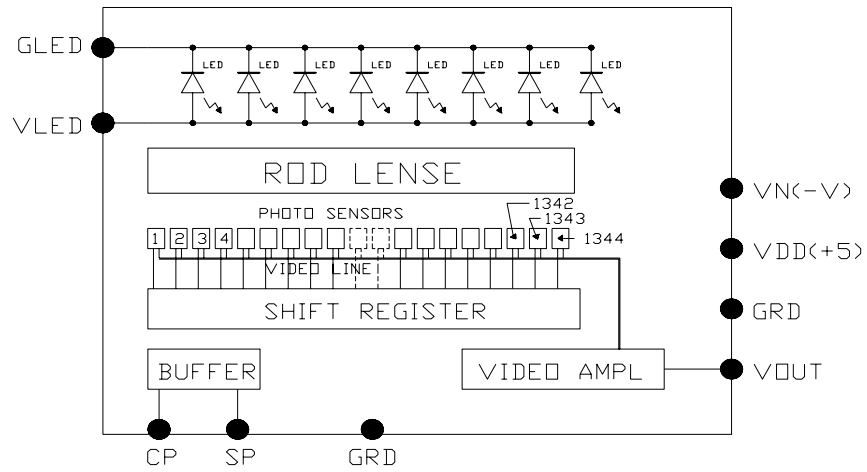


Figure 1: Block Diagram of the AMIS-710600-A8 Module

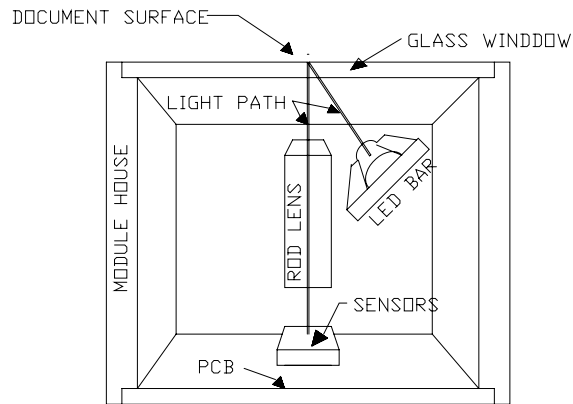


Figure 2: AMIS-710600-A8 Cross Section

Although the connector location is not seen in the cross section sketch (Figure 2), it is shown in the mechanical drawing (Figure 4). Table 1 shows the pin outs and their definitions.

Table 1: Pin Configuration

Pin Number	Symbol	Names and Functions
1	VOUT	Analog video output
2	GRD	Ground; 0V
3	Vdd (+5V)	Positive power supply
4	VN (-5V)	Negative power supply
5	GND	Ground; 0V
6	CP	Clock pulse
7	GND	Ground; 0V
8	SP	Shift register start pulse
9	GLED	Ground for the light source; 0V
10	VLED	Supply for the light source

4.0 Operational Environment

Conceptually, the overview of the module operation can be understood from the functional description (Section 3.0) and the module pin out description. All that the module requires are the power supplies, VDD, VGLED and VSS, with two control clock pulses, CP and SP. The timing diagram (Figure 3) provides the clock timing and its relationship to the output video pixels. When the power supplies and the clocks are connected, the module will start its line scanning process, hence the module is ready to produce video signal as soon as it is placed on the image document.

4.1 Absolute Maximum Rating

Table 2 shows the absolute maximum rating of inputs to the module.

Table 2: Absolute Maximum Rating

Parameter	Symbols	Maximum Rating	Units
Power supply inputs	VDD	10	V
	IDD	50	mA
	VLED	5.5	V
	ILED	150	mA
Input clocks high	Vih	Vdd – 0.5V	V
Input clocks low	Vil	-0.6	V

4.2 Operating Environment

Table 3 shows the environmental specification for the module.

Table 3: Environmental Specifications

Parameter	Symbols	Maximum Rating	Units
Operating temperature	Top	0 to 50	°C
Operating humidity	Hop	10 to 85	%
Storage temperature	Tstg	-25 to +75	°C
Storage humidity	Hstg	5 to 95	%

4.3 Electro-Optical Characteristics (25°C)

Table 4 lists the typical operational parameters at 25 °C, which characterizes the module's operations.

Table 4: Electro-Optical Characteristics at 25°C

Parameter	Symbol	Parameter	Units	Note
Number of photo detectors		1344	Elements	
Pixel-to-pixel spacing		42.3	µm	
Line scanning rate	Tint ⁽¹⁾	680	µsec	@ 2.0MHz clock frequency (see Note 1)
Clock frequency ⁽²⁾	f	2.0	MHz	
Bright output voltage ⁽³⁾	Vpavg	1.0	V	
Bright output non-uniformity ⁽⁴⁾	Up	<+/-30	%	
Adjacent pixel non-uniformity ⁽⁵⁾	Uadj	<15	%	
Dark non-uniformity ⁽⁶⁾	Ud	<200	mV	
Dark output voltage ⁽⁷⁾	Vd	<0.1	V	See Note 7
Modulation transfer function ⁽⁸⁾	MTF	>30	%	

- Notes:**
- (1) Tint: line scanning rate or the integration time. Tint is determined by the interval of two SPs. The minimum tint of 390µs is available with a 3.5MHz clock. However, the Vpavg is directly proportional to the integration time. For example, if tint is increased two times, Vpavg increases by two. Alternately, if tint is decreased by two then Vpavg decreases by two. The Vpavg of this module is adjusted to 1.0V with an integration time of 680µsec with a CP = 2.0MHz, hence if the SP is increased or decreased, the output will also increase or decrease. Note that changing the clock frequency will also change the tint if the SP rate is divided down from the CP.
 - (2) f: main clock frequency
 - (3) The video output is 1.0V with an integration time of 680µs. The video output is calculated based on $Vpavg = \sum Vp(n)/1344$
 - (4) $Up = [(Vpmax - Vpavg) / Vpavg] \times 100\%$ or $[(Vpavg - Vpmin) / Vpavg] \times 100\%$
Where Vpmax = the maximum video pixel value and Vpmin = the minimum video pixel value in the line scan.
 - (5) $Uadj = MAX[| (Vp(n) - Vp(n+1)) | / Vp(n)] \times 100\%$
Where Vp(n) is the nth pixel in the scan.
Uadj is the non-uniformity percentage pixel to pixel
 - (6) $Ud = Vdmax - Vdmin$
Vdmin is the minimum output on a black document(O.D.=0.8)⁽⁹⁾
Vdmax: maximum output voltage of a black document (O.D.= 0.8)
 - (7) Vd is adjustable, it can be set to ground, (0V). The factory adjust is close to 0V.
 - (8) $MTF = [(Vmax - Vmin) / (Vmax + Vmin)] \times 100 [\%]$
Vmax: maximum output voltage on a 11.8lp/mm⁽¹⁰⁾ bar target (300dpi)⁽¹¹⁾
Vmin: minimum output voltage on a 11.8lp/mm (300dpi) bar target.
 - (9) O.D. = optical density
 - (10) lp / mm: line pair per mm
 - (11) DPI = dots per inch

4.4 Recommended Operating Conditions (25°C)

Table 5 lists the recommended operating conditions of the module.

Table 5: Recommended Operating Conditions (25°C)

Item	Symbol	Min.	Mean	Max.	Units
Power supply	VDD	4.5	5.0	5.5	V
	VLED	4.5	5	5.5	V
	IDD	20	25	30	ma
	ILED	85	115	150	ma
Input voltage at digital high	Vih	Vdd-1.0	Vdd-.5	Vdd	V
Input voltage at digital low	Vil	0		0.8	V
Clock frequency	f			3.5	MHz
Clock pulse high duty cycle		25	50	75	%
Clock pulse high duration		71 ⁽¹⁾			ns
Integration time	Tint	390 ⁽²⁾		10000	µs
Operating temperature	Top		25	50	C

- Notes:**
- (1) This is with a maximum clock frequency of 3.5MHz and a duty cycle of 25 percent.
 - (2) The integration time is the minimum allowable time at a 3.5MHz clock rate.

5.0 Timing Characteristics of the Module (25°C)

The input control clocks and video pixel output relationships are depicted in Figure 3. As indicated, the internal shift register is loaded on the falling edges of the module's clock, CP and during this time the SP is high or true. To ensure that only one shift register pulse is loaded into the shift register during any one line scan, only one SP is allowed to go high for one CP cycle going low. After loading the shift register, the SP is to remain low throughout the remainder of the line scan; otherwise multiple start pulses will load into the shift register. To prevent this phenomenon, as the timing diagram shows, SP should occur only once in one CP cycle. When only one pulse is loaded in the register, a single pulse shifts down the register, accessing a single photo-site with each shift and sequentially reading it out onto the common video line where the video pixel is amplified and produced at the output I/O.

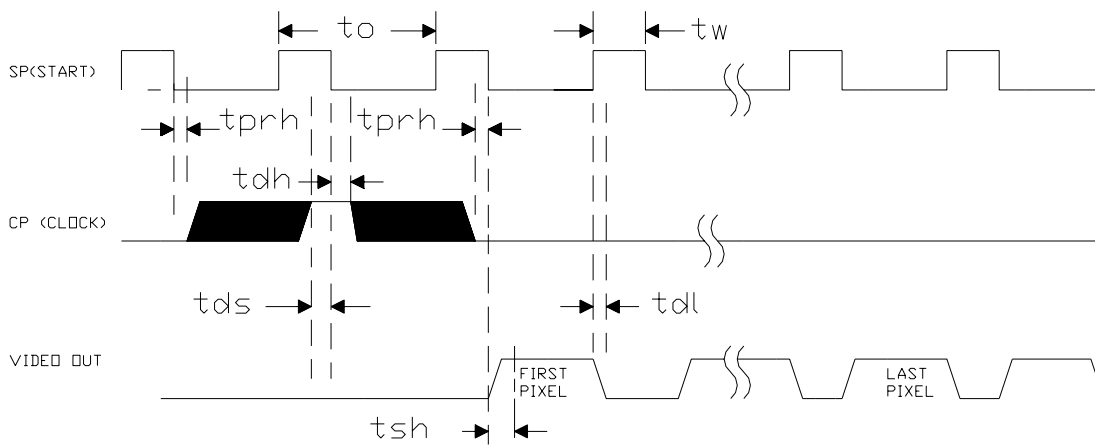


Figure 3: Timing Diagram of SP Relative to First Pixel

The call outs for the switching characteristics in Figure 3 are given in Table 6. This table defines the symbols used in the timing diagram and calls out their time durations.

Table 6: Timing Definition and Specifications

Item	Symbol	Min.	Typ.	Max.	Units
Clock cycle time	to	290		7440	ns
Clock pulse width	tw	71			ns
Clock duty cycle		25		75	%
Prohibit crossing time of SP	tprh	30			ns
Data setup time	tds	30			ns
Data hold time	tdh	30			ns
Signal delay time	tdl	50			ns
Signal sample and hold time	tsh	120			ns

6.0 AMIS-710600-A8 Module and its Mechanical Dimensions

The pictorial sketch depicted in Figure 4 illustrates the approximate dimensions of the AMIS-710600-A8 housing. It is not intended to be a reference for a detailed system design but provides the overall dimensions for estimating possible uses for this module in a given system. A detailed drawing can be made available upon request.

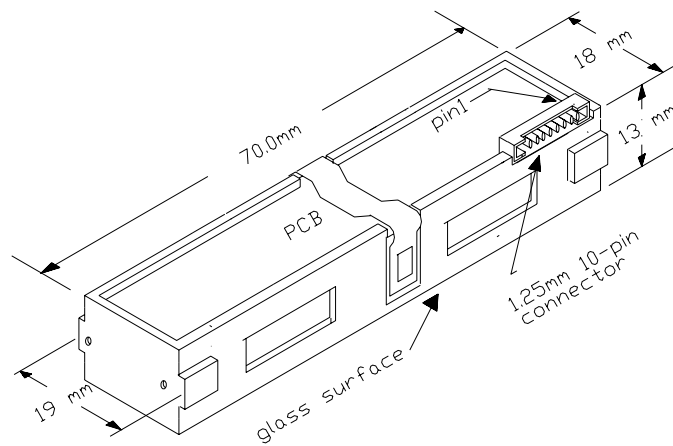


Figure 4: AMIS-710600-A8 Module and its Mechanical Dimensions

7.0 Company or Product Inquiries

For more information about AMI Semiconductor, our technology and our product, visit our Web site at: <http://www.amis.com>

North America

Tel: +1.208.233.4690

Fax: +1.208.234.6795

Europe

Tel: +32 (0) 55.33.22.11

Fax: +32 (0) 55.31.81.12

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