

## FEATURES

### Four Operational Modes Including:

- Constant Laser Current
- Constant Optical Output Power
- Constant EDFA Gain
- Constant Laser Power

### High Power Efficiency: >90%

### Three Built-In Photodiode TIAs

### Adjustable Laser Diode and EDFA Protection Limits

### Free-run or Synchronous Switching Frequency Modes

### Adjustable Phase Delay for Synchronous Clock Mode

### Optional Dithering Built-In

### Programmable Dither Frequency and Amplitude

## APPLICATIONS

### EDFA Pump Laser Diode Control

### CW Laser Bias Control

### Raman Amplifiers

## GENERAL DESCRIPTION

The ADN8820 is a versatile Continuous Wave (CW) and EDFA laser diode driver and controller. It provides a low noise and precise current control for driving a source or pump laser diode.

It can be set to operate in one of four controller modes: Constant Current (CC), Constant Laser Power (CLP), Constant

Output Power (COP), or Constant EDFA Gain (CG). Multiple pump laser applications are easily supported by the ADN8820. Common-cathode-to-ground and common-anode-to-VDD configurations are also supported.

The ADN8820 has a high speed closed-loop control, making it suitable for add/drop applications in telecommunication systems. It has a low-current shutdown mode and a soft-start feature to minimize power supply bounce on start-up.

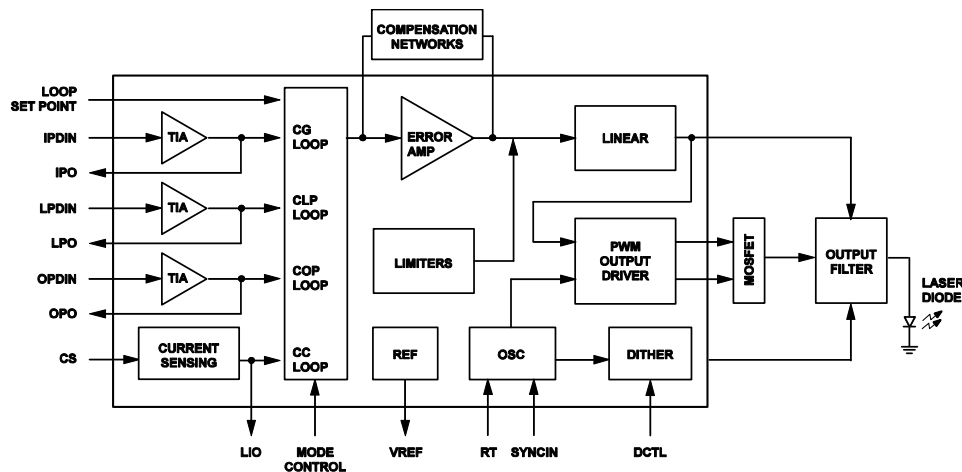
Protection circuitry is built into the device. The protection limits are easily adjustable and are used to set maximum output current and voltage, optical output power, EDFA gain, and pump or CW laser power.

The output stage consists of a high-efficiency PWM amplifier in parallel with a high-speed linear amplifier. This provides the fastest settling time response along with the lowest power and heat dissipation. A pair of external MOSFETs on the PWM amplifier provide output currents of up to 5A.

Three low-bias current TIAs are built-in. These allow amplification for the laser back-facet photodiode and EDFA input and output photodiodes. For CW laser applications, the two unused TIAs can be used for etalon photodiode amplification, allowing continuous wavelength monitoring.

The ADN8820 is available in a 7 x 7 mm lead-frame chip scale package (LFCSP) with a package height of less than 1 mm.

## FUNCTIONAL BLOCK DIAGRAM



\* U.S. Patent Pending

### Rev. PrB

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# ADN8820 - SPECIFICATIONS<sup>1</sup>

## Preliminary Technical Data

**Table 1. ADN8820—Electrical Characteristics (AVDD = PVDD = 5V, AGND = PGND = 0V, T<sub>A</sub> = 25°C, using typical circuit in Figure 1, unless otherwise noted.)<sup>2</sup>**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>TRANSIMPEDANCE AMPLIFIERS</b>						
Detection Range	I <sub>IP</sub>	From IPDIN Photodiode	0.005		5,000	μA
	I <sub>OP</sub>	From OPDIN Photodiode	0.005		5,000	μA
	I <sub>LP</sub>	From LPDIN Photodiode	5		5,000	μA
Input Bias Current	I <sub>BIPDIN</sub>	IPDIN, OPDIN, LPDIN Amplifier		100		pA
	I <sub>BOPDIN</sub>	Inputs		100		pA
	I <sub>BLPDIN</sub>			100		pA
Input Voltage Range	V <sub>BLP</sub> , V <sub>B</sub>		0		VDD	V
Monitor Output Range	V <sub>IPO</sub>	IPO, LPO, OPO Outputs	0		VDD	V
	V <sub>LPO</sub>		0		VDD	V
	V <sub>OPO</sub>		0		VDD	V
Input Offset Voltage	V <sub>OSIP</sub>	IPDIN, OPDIN, LPDIN Amplifiers		10		μV
	V <sub>OSOP</sub>			10		μV
	V <sub>OSLP</sub>			2		mV
Maximum Output Current	I <sub>OUTIPO</sub>	IPO, LPO, OPO Outputs		±10		mA
	I <sub>OUTLPO</sub>			±10		mA
	I <sub>OUTOPO</sub>			±10		mA
Gain-Bandwidth Product	GBW <sub>IP</sub>	IPDIN, OPDIN, LPDIN Amplifiers		10		MHz
	GBW <sub>OP</sub>			10		MHz
	GBW <sub>LP</sub>			1		MHz
<b>LIMIT CONTROLS</b>						
Input Voltage Range	V <sub>INLIM</sub>	IPMIN, OPLIM, LPLIM, ILIM, and VLIM	0		2.6	V
Limiter Accuracy	V <sub>OSLIM</sub>	OPLIM, LPLIM, ILIM, IPMIN			±10	mV
Open Circuit Voltage	V <sub>LIMNC</sub>	Voltage for OPLIM, LPLIM, and ILIM with no connection	2.5	2.6	2.7	V
Pull-up Current	I <sub>B LIM</sub>	Flowing out of OPLIM, LPLIM, and ILIM with LIM Voltage <2.0V		500		nA
IPMIN Disable Threshold	V <sub>IPMINLO</sub>	V <sub>IPO</sub> = 0V		200		mV
VLIM Input Bias Current	I <sub>VLIM</sub>	Flowing into VLIM pin			1	μA
VLIM Voltage Control Accuracy		V <sub>LINOUT</sub> - VLIM			50	mV
<b>ERROR AMPLIFIER</b>						
Input Offset Voltage	V <sub>OSEA</sub>			10	25	μV
Input Common-Mode Voltage Range	V <sub>CMEA</sub>		0		VDD	V
Output Voltage Swing	V <sub>OUTEA</sub>		0		VDD	V
Maximum Output Current	I <sub>MAXEA</sub>			±10		mA
Gain-Bandwidth	GBW <sub>EA</sub>			10		MHz
<b>SET INPUT</b>						
Input Voltage Range	V <sub>SET</sub>		0		VDD	V
Input Bias Current	I <sub>B SET</sub>			±1		μA
<b>MULTIPLEXERS</b>						
Output Impedance				100		Ω
Output Voltage Range			0		VDD	V

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>LINEAR OUTPUT</b>						
Short-Circuit Output Current	I <sub>OUTLIN</sub>	I <sub>OUTLIN</sub> = 300mA (sourcing) I <sub>OUTLIN</sub> = -160mA (sinking)	300			mA
Output Voltage Compliance	V <sub>LINMAX</sub>		4.5			V
	V <sub>LINMIN</sub>				0.5	V
Power Supply Rejection Ratio	PSRR <sub>LIN</sub>			68		dB
Gain-Bandwidth Product	GBW <sub>LIN</sub>			10		MHz
<b>PWM OUTPUT</b>						
Offset Voltage	V <sub>OSPWM</sub>	V <sub>OSPWM</sub> = L <sub>INOUT</sub> - FB			±10	mV
Non-Overlap Delay						
Output Transition Time	t <sub>r</sub> , t <sub>f</sub>	FET C <sub>ISS</sub> ≤ 3nF		40		ns
Output Driver Resistance	R <sub>NGATE</sub> R <sub>PGATE</sub>			6 6		Ω Ω
Output Current Ripple		I <sub>OUT</sub> = 300mA, V <sub>OUT</sub> = 2V		1		%
Soft-Start Time		C <sub>SS</sub> = 0.1 μF		15		ms
Standby Mode Threshold	V <sub>SSSB</sub>	PWM and L <sub>INOUT</sub> disabled			0.4	V
<b>OSCILLATOR</b>						
Free-Run Oscillation Frequency	f <sub>CLK</sub>	CMPOSC = VDD; SYNCIN = 0V	100		1,000	kHz
Synchronization Capture Range		SYNCIN driven with external clock	100		1,000	kHz
Phase Adjustment	φ <sub>CLK</sub>		45		315	degrees
<b>CURRENT SENSE AMPLIFIER</b>						
Input Common-Mode Voltage Range	V <sub>CMCS</sub>		0		VDD	V
Input Resistance	R <sub>INCS</sub>			10.5		kΩ
Output Offset Voltage	V <sub>OSLIO</sub>	V <sub>CSP</sub> = V <sub>CSN</sub> = 2.5V		1		mV
Gain	A <sub>VCS</sub>	V <sub>LIO</sub> / (V <sub>CSP</sub> - V <sub>CSN</sub> )		20		V/V
Output Voltage Range	V <sub>LIO</sub>		0		VDD	V
<b>DITHER GENERATOR</b>						
Frequency Range	f <sub>DITHER</sub>	xx kΩ ≤ RT ≤ xx kΩ	0.2		2	MHz
Frequency Multiplier Programming Voltage		See Table II				
Dither Current Control Voltage	V <sub>DCTL</sub>	V <sub>LIO</sub> = 2.5 V	1.2	1.25	1.3	V
Programming Current Range	I <sub>DCTL</sub>	V <sub>LIO</sub> = 2.5 V	0		100	μA
Maximum DO Output Current	I <sub>MAXDO</sub>		±19	±20	±21	mA
DO Output Voltage	V <sub>DO</sub>			1.5		V
<b>POWER SUPPLY</b>						
Power Supply Range	V <sub>DD</sub>		3.0		5.5	V
Supply Current	I <sub>SY</sub>	DSEL/ $\overline{SD}$ ≥ 0.8V; I <sub>OUT</sub> = 0A -40°C ≤ T <sub>A</sub> ≤ +85°C		25	30	mA
Shutdown Current	I <sub>SD</sub>	DSEL/ $\overline{SD}$ ≤ 0.2V		10		μA
Standby Current	I <sub>SB</sub>	SS/ $\overline{SB}$ ≤ 0.2V		2.5		mA
Undervoltage Lockout	V <sub>UVLO</sub>			2.4	2.5	V
<b>REFERENCE OUTPUT</b>						
Reference Voltage	V <sub>REF</sub>	I <sub>REF</sub> ≤ 2 mA	2.4	2.5	2.6	V
Power Supply Rejection Ratio	PSRR <sub>REF</sub>	With respect to AVDD		68		V

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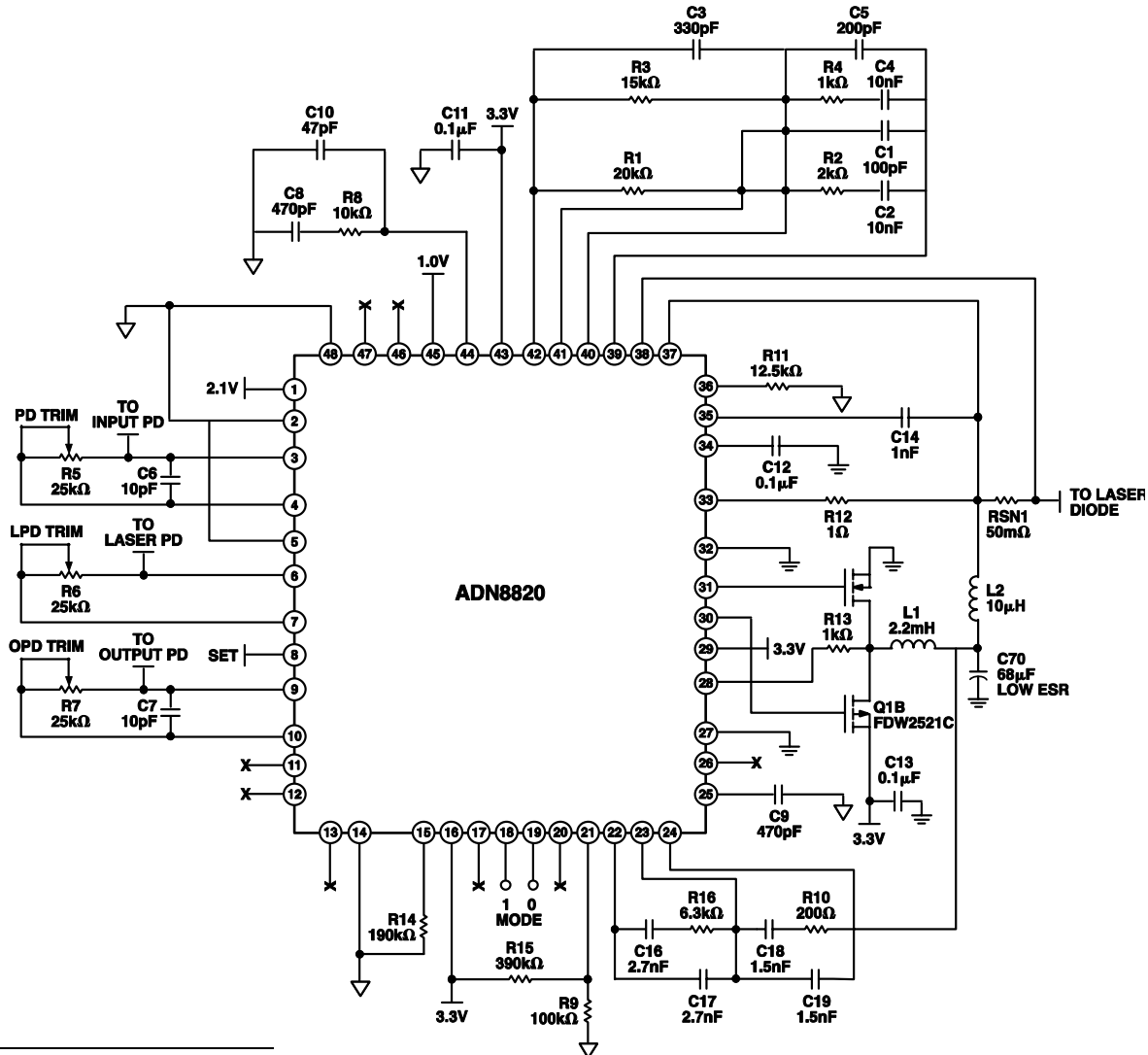
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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DUAL OUTPUT						
Output Voltage Range	V <sub>DUAL</sub>	I <sub>DUAL</sub> ≤ 500 μA	0.4		VDD-0.4	V
Voltage Gain	A <sub>V DUAL</sub>	A <sub>V DUAL</sub> = DUAL / LIO; V <sub>LIM</sub> = 2.25V with 1.9V ≤ V <sub>LIO</sub> ≤ 2.1V		20		V/V
CONTROL LOOP STATUS OUTPUT						
CLGD High	V <sub>CLGDHI</sub>	0.05 x VDD ≤ V <sub>EAOUT</sub> ≤ 0.95 x VDD	4.8			V
CLGD Low	V <sub>CLGDLO</sub>	Otherwise			0.2	V
LOGIC CONTROL						
Logic Low Input Threshold	V <sub>IL</sub>	MODE0, MODE1, SYNCIN			0.2	V
Logic High Input Threshold	V <sub>IH</sub>	MODE0, MODE1, SYNCIN	VDD-0.2			V
Logic Low Output Level	V <sub>OL</sub>				0.2	V
Logic High Output Level	V <sub>OH</sub>		VDD-0.2			V
Input Current					±1	μA



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Figure 1. Typical Application Circuit

## ABSOLUTE MAXIMUM RATINGS

**Table 2. Absolute Maximum Ratings (at 25°C, unless otherwise noted)**

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range: CP Packages	-65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

**Table 3. Thermal Resistance**

Package Type	$\theta_{JA}^1$	$\theta_{JC}$	Unit
LFSCP-48 (CP-48)	32	12	°C/W

<sup>1</sup>  $\theta_{JA}$  is specified for the worst-case conditions, i.e.,  $\theta_{JA}$  is specified for device soldered in circuit board for surface mount packages.

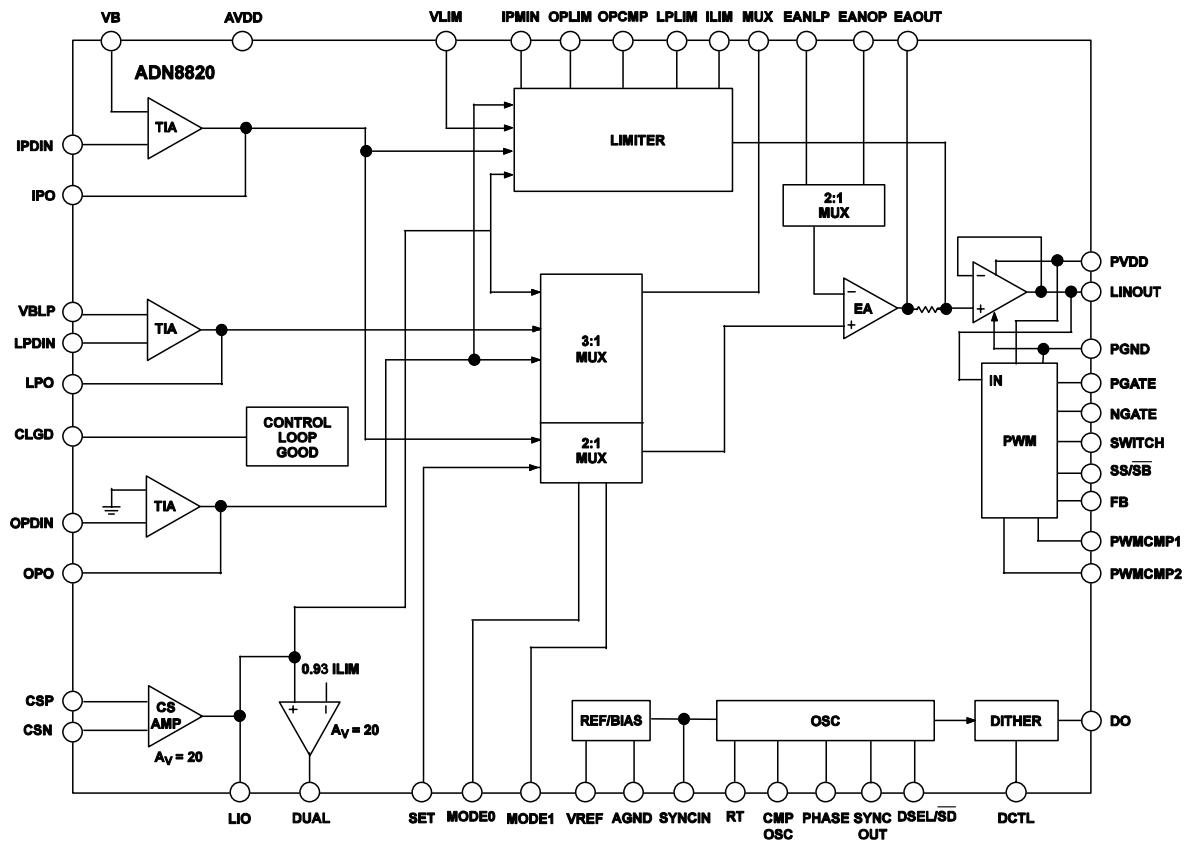
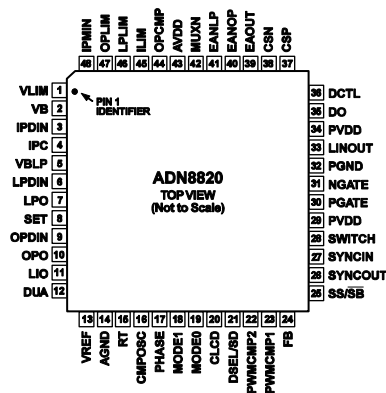


Figure 2. System Block Diagram

## PIN CONFIGURATION



## PIN FUNCTIONS

Name	Pin	Function	Connections
<b>AMPLIFIER INPUTS</b>			
IPDIN	3	Input to TIA for EDFA input photodiode	EDFA input photodiode and feedback resistor
LPDIN	6	Input to TIA for laser photodiode	Laser photodiode and feedback resistor
OPDIN	9	Input to TIA for EDFA output photodiode	EDFA output photodiode and feedback resistor
VB	2	Bias voltage for EDFA input and output photodiodes	External bias voltage required
VBLP	5	Bias voltage for laser photodiode	External bias voltage required
CSP	37	Non-inverting input of current sense amplifier	High-side of laser current sense resistor (50 mΩ typ.)
CSN	38	Inverting input of current sense amplifier	Low-side of laser current sense resistor (50 mΩ typ.)
<b>LIMIT INPUTS</b>			
VLIM	1	Laser diode voltage will not exceed VLIM	External voltage required
ILIM	45	Limits output voltage if LIO > ILIM	External voltage or no connection (defaults to 2.5 V)
OPLIM	47	Limits output voltage if OPO > OPLIM	External voltage or no connection (defaults to 2.5 V)
LPLIM	46	Limits output voltage if LPO > LPLIM	External voltage or no connection (defaults to 2.5 V)
IPMIN	48	Limits output voltage if IPO is lower than IPMIN	External voltage required
<b>ERROR (COMPENSATION) AMPLIFIER (EA)</b>			
EANLP	41	Compensation network for laser diode loop	Internally connects inverting input of EA to laser diode compensation network
EANOP	40	Compensation network for EDFA loop	Internally connects inverting input of EA to EDFA compensation network
EAOUT	39	Output of compensation amplifier	Internal connection to linear output amplifier
MUX	42	Allows separate compensation for EDFA and laser diode	Connects to two external compensation networks: one for EDFA loop, one for laser diode loop
OPCMP	44	Compensation for limiter section	R-C network to ground
SET	8	Sets output power or current based on MODE settings	External voltage or DAC
<b>POWER OUTPUT AMPLIFIERS</b>			
LINOUT	33	Linear amplifier output	Laser diode through 1 Ω series resistor
PGATE	30	PWM switching for PMOS	Gate of external PMOS for PWM output
NGATE	31	PWM switching for NMOS	Gate of external NMOS for PWM output
SWITCH	28	PWM amplifier output	Drains of external NMOS, PMOS, and input of L-C filter
FB	24	Feedback input for PWM amplifier	Output of L-C filter and laser diode
PWMCMP1	23	Compensation for PWM amplifier	Series R-C networks to FB and PWMCMP2
PWMCMP2	22	Compensation for PWM amplifier	Series R-C to PWMCMP1
SS/SB	25	Constant current charges external capacitor to soft-start PWM output from 0% duty cycle	Optional external FET can pull down and to engage standby mode
<b>OUTPUT MONITOR VOLTAGES</b>			
IPO	4	Output of EDFA input photodiode TIA	Feedback resistor to IPDIN
OPO	10	Output of EDFA output photodiode TIA	Feedback resistor to OPDIN
LPO	7	Output of laser diode photodiode TIA	Feedback resistor to LPDIN
LIO	11	Output of current sense amplifier	
DUAL	12	Compares LIO to 90% of ILIM	To SET pin of additional ADN8820 device in multi-pump optical amplifier applications
EAOUT	39	Output of compensation amplifier	Internal connection to linear output amplifier
<b>OSCILLATOR SECTION</b>			
SYNCIN	27	Optional clock input signal for PLL	Ground or external clock
SYNCOUT	26	Follows rising edge of SYNCIN plus phase shift	Optional connection to SYNCIN of additional ADN8820 device
CMPOSC	16	Compensation for synchronizing PLL	R-C network to ground
PHASE	17	Sets rising edge phase shift of SYNCOUT	External voltage or no connection (default is 0.7V)
RT	15	Sets PWM clock frequency	Resistor (R <sub>T</sub> ) to ground

Name	Pin	Function	Connections
<b>DITHER GENERATOR</b>			
DSEL/ $\overline{SD}$	21	4-level logic input to set dither frequency or engage shutdown	External voltage
DCTL	36	Sets dither current as a percentage of the laser diode current	Resistor ( $R_{DCTL}$ ) to ground
DO	35	Optional dither AC current to laser diode	To laser diode through 1 nF series capacitor
<b>LOGIC INPUTS</b>			
MODE1	18	Sets control loop mode (see Table I)	External logic voltage
MODE0	19	Sets control loop mode (see Table I)	External logic voltage
DSEL/ $\overline{SD}$	21	Pulling voltage low engages shutdown	External voltage
SS/ $\overline{SB}$	25	Pulling voltage low engages standby	470 pF soft-start capacitor to ground; optional external FET can pull down to engage standby
<b>LOGIC OUTPUTS</b>			
CLGD	20	Logic high if EAOUT is within 5% to 95% of AVDD; Logic low otherwise	
<b>POWER</b>			
PVDD	29, 34	Power for output amplifiers and digital sections	3.0 V to 5.5 V
AVDD	43	Low noise power for TIAs, limiter section, and EA	3.0 V to 5.5 V
PGND	32	Current return for output amplifiers	0 V
AGND	14	Low noise ground	0 V
VREF	13	2.5 V reference voltage	Can be used as reference for VB, VBLP, SET, and limiter inputs

**TABLE 4. MODE CONTROL LOGIC**

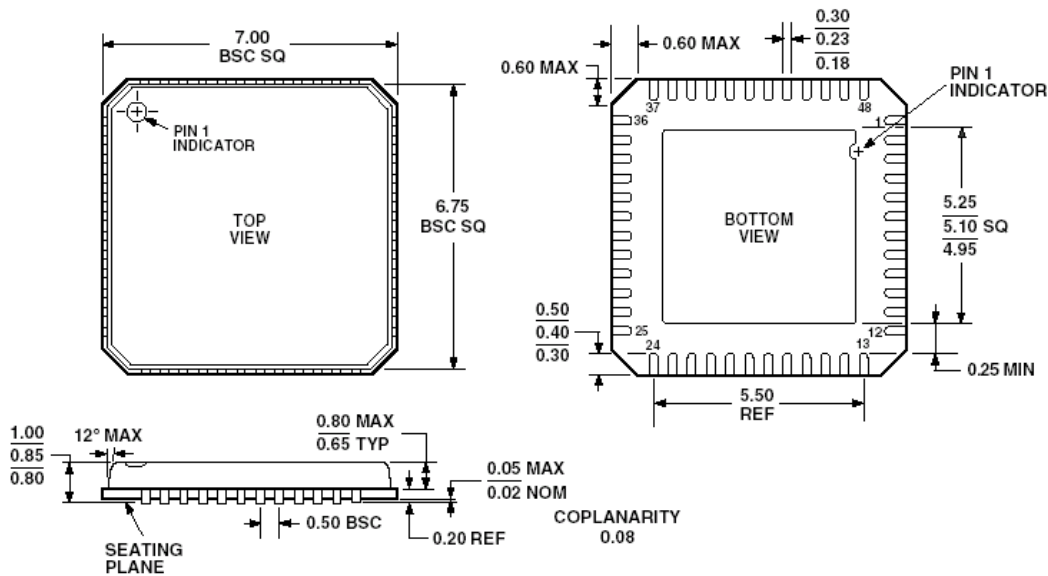
MODE Inputs		Mode Setting	Error Amplifier		MUX Output	Description
MODE1	MODE0		-Input	+Input		
0	0	Constant Current	EANLP	SET	LIO	Maintains a fixed current through laser diode; generally used for calibration.
0	1	Constant Laser Power	EANLP	SET	LPO	Maintains a constant optical output power from laser diode.
1	0	Constant Ouptut Power	EANOP	SET	OPO	Maintains a constant optical power at output of EDFA.
1	1	Constant Gain	EANOP	IPO	OPO	Monitors both input and output optical power to maintain constant gain from optical amplifier.

**TABLE 5. PWM CLOCK FREQUENCY SELECTION LEVELS**

DSEL/ $\overline{SD}$ (V)		Mode	PWM Clock Frequency Division
Min	Max		
0	0.5	Shutdown	N/A
0.7	1.2	Active	$f_{DITHER} \div 2$
1.3	1.8	Active	$f_{DITHER} \div 4$
2.0	VDD	Active	$f_{DITHER} \div 8$

Note:  $f_{DITHER}$  is the ADN8820 dither frequency and is set by a resistor connected from RT to ground.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKGD-2

Figure 3. 48-Lead Frame (LFCSP-48) Chip Scale Package

7 x 7 mm Body  
(CP-48)  
Dimensions Shown in Millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## ORDERING GUIDE

**Table 6. ADN8820 Ordering Guide**

Product	Package Description	Package Option	Top Mark	No. of Parts per Reel	Temperature Range (°C)
ADN8820	48-Lead LFCSP	CP-48	TBD	N/A	-40 to +125
ADN8820-REEL7	48-Lead LFCSP	CP-48	TBD	TBD	-40 to +125
ADN8820-EVAL	Eval board	N/A	N/A	N/A	-40 to +125