Ultrafast SiGe Voltage Comparator

Preliminary Technical Data

ADCMP580/ADCMP581/ADCMP582

FEATURES

150 ps propagation delay
25 ps overdrive and slew rate dispersion
8 GHz equivalent input rise time bandwidth
100 ps minimum pulse width
35 ps typical output rise/fall
10 ps deterministic jitter(DJ)
200 fs random jitter (RJ)
−2 V to +3 V input range with +5 V/−5.2 V supplies
On-chip terminations at both input pinsl
Resistor-programmable hysteresis
Differential latch control
Power supply rejection > 70 dB

APPLICATIONS

Automatic test equipment (ATE)
High speed instrumentation
Pulse spectroscopy
Medical imaging and diagnostics
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Clock and data signal restoration

GENERAL DESCRIPTION

The ADCMP580/ADCMP581/ADCMP582 are ultrafast voltage comparators fabricated on Analog Devices, Inc.'s proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP580 features CML output drivers; the ADCMP581 features reduced swing ECL (negative ECL) output drivers; and the ADCMP582 features reduced-swing PECL (positive ECL) output drivers.

The three comparators offer 150 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs random jitter (RJ). Overdrive and slew rate dispersion is typically less than 25 ps.

FUNCTIONAL BLOCK DIAGRAM

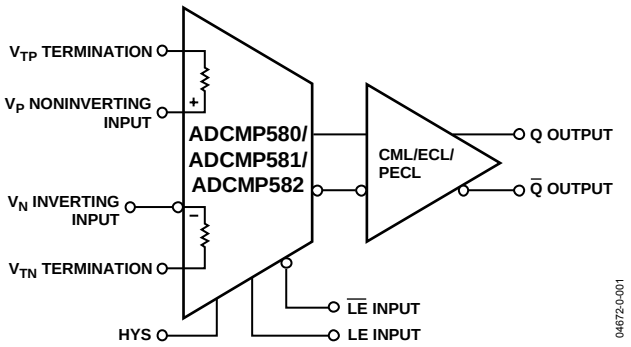

Figure 1.

The ±5 V power supplies enable a wide −2 V to +3 V input range with logic levels referenced to the CML/NECL/PECL outputs. The three inputs have 50 Ω on-chip termination resistors with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance input.

The CML output stage is designed to directly drive 400 mV into 50 Ω transmission lines terminated to ground. The NECL output stages are designed to directly drive 400 mV into 50 Ω terminated to −2 V. The PECL output stages are designed to directly drive 400 mV into 50 Ω terminated to V_{CCO} − 2 V. High speed latch and programmable hysteresis are also provided. The differential latch input controls are also 50 Ω terminated to an independent V_{TT} pin to interface to either CML or ECL or to PECL logic.

The ADCMP580/ADCMP581/ADCMP582 are available in a 16-lead LFCSP package.

Rev. PrA

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REVISION HISTORY

6/04—Revision PrA

ELECTRICAL CHARACTERISTICS

V_{CCI} = +5.0 V, V_{EE} = −5.0 V, V_{CCO} = +3.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Input Voltage Range	V_P, V_N		−2.0		+3.0	V
Input Differential Range			−2.0		+2.0	V
Input Offset Voltage	V_{OS}		−5.0	±2.0	+5.0	mV
Offset Voltage Tempco	$\Delta V_{OS}/d_T$			10.0		µV/°C
Input Bias Current	I_P, I_N	Open termination		15.0	30.0	µA
Input Bias Current Tempco				50.0		nA/°C
Input Offset Current				2.0	5.0	µA
Input Capacitance	C_P, C_N			TBD		pF
Input Resistance			47.5	50	52.5	Ω
Input Resistance, Differential Mode		Open termination		50		kΩ
Input Resistance, Common Mode		Open termination		500		kΩ
Active Gain	A_V			48		dB
Common-Mode Rejection	CMRR	V_{CM} = −2.0 V to +3.0 V		50		dB
Hysteresis		R_{HYS} = ∞		±1		mV
LATCH ENABLE CHARACTERISTICS						
ADCMP580 (CML)						
Latch Enable Input Range			−0.8		0	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 100 mV		60		ps
Latch Hold Time	t_H	V_{OD} = 100 mV		0		ps
ADCMP581 (NECL)						
Latch Enable Input Range			−1.8		+0.8	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 100 mV		25		ps
Latch Hold Time	t_H	V_{OD} = 100 mV		0		ps
ADCMP582 (PECL)						
Latch Enable Input Range			V_{CCO} − 1.8		V_{CCO} − 0.8	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	V_{OD} = 100 mV		5		ps
Latch Hold Time	t_H	V_{OD} = 100 mV		0		ps
Latch Enable Input Impedance			47.5	50.0	52.5	ps
Latch to Output Delay	t_{PLOH}, t_{PLOL}	V_{OD} = 100 mV		150		ps
Latch Minimum Pulse Width	t_{PL}	V_{OD} = 100 mV		100		ps
DC OUTPUT CHARACTERISTICS						
ADCMP580 (CML)						
Output Impedance	Z_{OUT}		47.5	50	52.5	Ω
Output Voltage High Level	V_{OH}	50 Ω to GND	−0.10	−0.05	0.00	V
Output Voltage Low Level	V_{OL}	50 Ω to GND	V_{OH} − 0.45	V_{OH} − 0.40	V_{OH} − 0.35	V
Output Voltage Differential		50 Ω to GND	350	400	450	mV
Temperature Coefficient, V_{OH}	$\Delta V_{OH}/d_T$	50 Ω to GND		TBD		mV/°C
Temperature Coefficient, V_{OL}	$\Delta V_{OL}/d_T$	50 Ω GND		TBD		mV/°C
ADCMP581 (NECL)						
Output Voltage High Level	V_{OH}	50 Ω to −2.0 V	−0.90	−0.80	−0.70	V
Output Voltage Low Level	V_{OL}	50 Ω to −2.0 V	V_{OH} − 0.45	V_{OH} − 0.40	V_{OH} − 0.35	V
Output Voltage Differential		50 Ω to −2.0 V	350	400	450	mV

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADCMP582 (PECL)						
Output Voltage High Level	V_{OH}	50 Ω to V_{CCO} − 2.0 V	V_{CCO} − 0.9	V_{CCO} − 0.80	V_{CCO}− 0.70	V
Output Voltage Low Level	V_{OL}	50 Ω to V_{CCO} − 2.0 V	V_{OH} − 0.45	V_{OH} − 0.40	V_{OH} − 0.35	V
Output Voltage Differential		50 Ω to V_{CCO} − 2.0 V	350	400	450	mV
AC PERFORMANCE						
Propagation Delay	t_{PD}	V_{OD} = 200 mV		150		ps
Propagation Delay		V_{OD} = 20 mV		165		ps
Propagation Delay Tempco	$\Delta t_{PD}/d_T$			0.5		ps/°C
Prop Delay Skew—Rising Transition to Falling Transition		V_{OD} = 200 mV, 5 V/ns		10		ps
Overdrive Dispersion		50 mV < V_{OD} < 1.0 V		10		ps
		5 mV < V_{OD} < 1.0 V		15		ps
Slew Rate Dispersion		2 V/ns to 10 V/ns		25		ps
Pulse Width Dispersion		100 ps to 5 ns		5		ps
Duty Cycle Dispersion		1.0 V/ns, V_{CM} = 0.0 V		10		ps
		1.0 V/ns, V_{CM} = 2.0 V		5		ps
Common-Mode Dispersion		V_{OD} = 0.4V , −2 V < V_{CM} < 3 V		5		ps/V
Equivalent Input Bandwidth[1]	BW_{EQ}	0.0 V to 400 mV input t_R = t_F = 25 ps, 20/80		8.0		GHz
Toggle Rate		>50% Output Swing		12.5		Gbps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns PRBS^{31} − 1 NRZ, 4 Gbps		10		ps
Deterministic Jitter	DJ	V_{OD} = 200 mV, 5 V/ns PRBS^{31} − 1 NRZ, 10 Gbps		TBD		ps
RMS Random Jitter	RJ	V_{OD} = 200 mV, 5 V/ns, 1.25 GHz		0.2		ps
Minimum Pulse Width	PW_{MIN}	t_{PD}/P_W < 5 ps		100		ps
Minimum Pulse Width	PW_{MIN}	t_{PD}/P_W < 10 ps		80		ps
Rise Time	t_R	20/80		35		ps
Fall Time	t_F	20/80		35		ps
POWER SUPPLY						
Positive Supply Voltage	V_{CCI}		+4.5	+5.0	+5.5	V
Negative Supply Voltage	V_{EE}		−5.5	−5.0	−4.5	V
Logic Supply Voltage	V_{CCO}		+4.5/+2.0	+5.0/+2.5	+5.5/+3.0	V
ADCMP580 (CML)						
Positive Supply Current	I_{VCCI}	V_{CCI} = +5.0 V, 50 Ω to Ground		6	8	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to Ground		43	50	mA
Power Dissipation	P_D	50 Ω to Ground		244	260	mW
ADCMP581 (NECL)						
Positive Supply Current	I_{VCCI}	V_{CCI} = +5.0 V, 50 Ω to −2 V		6	8	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to −2 V		28	35	mA
Power Dissipation	P_D	50 Ω to −2 V		218	240	mW
ADCMP582 (PECL)						
Positive Supply Current	I_{VCCI} + I_{VCCO}	V_{CCI} = +5.0 V, V_{CCO} = +5.0 V 50 Ω to V_{CCO} − 2 V		47	55	mA
Negative Supply Current	I_{VEE}	V_{EE} = −5.0 V, 50 Ω to V_{CCO} − 2 V		28	35	mA
Power Dissipation	P_D	50 Ω to V_{CCO} − 2 V		253	275	mW
Power Supply Rejection (V_{CCI})	PSR_{VCCI}	V_{CCI}=5.0 V + 5%		70		dB
Power Supply Rejection (V_{EE})	PSR_{VEE}	V_{EE}=-5.0 V + 5%		75		dB
Power Supply Rejection (V_{CCO})	PSR_{VCCO}	V_{CCO}=3.3 V + 5%		70		dB

[1] Equivalent Input Bandwidth assumes a simple first-order input response and is calculated with the following formula: $BW_{EQ} = 0.22/\sqrt{(tr_{COMP}^2 - tr_{IN}^2)}$, where tr_{IN} is the 20/80 transition time of a quasi-Gaussian input edge applied to the comparator input and tr_{COMP} is the effective transition time digitized by the comparator.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
SUPPLY VOLTAGES	
Positive Supply Voltage (V_{CCI} to GND)	−0.5 V to +6.0 V
Negative Supply Voltage (V_{EE} to GND)	−6.0 V to +0.5 V
Logic Supply Voltage (V_{CCO} to GND)	−0.5 V to +6.0 V
INPUT VOLTAGES	
Input Voltage	−3.0 V to +4.0 V
Differential Input Voltage	−2.5 V to +2.5 V
Input Voltage, Latch Enable	−2.5 V to +5.5 V
HYSTERESIS CONTROL PIN	
Applied Voltage (HYS to V_{EE})	−5.5 V to +0.5 V
Maximum Input/Output Current	1 mA
OUTPUT CURRENT	
ADCMP580 (CML)	−25 mA
ADCMP581 (NECL)	−40 mA
ADCMP582 (PECL)	−40 mA
TEMPERATURE	
Operating Temperature, Ambient	−40°C to +85°C
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

THERMAL CONSIDERATIONS

The ADCMP580/ADCMP581/ADCMP582 LFCSP 16-lead package option has a θ_{JA} (junction to ambient thermal resistance) of 70°C/W in still air.

Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

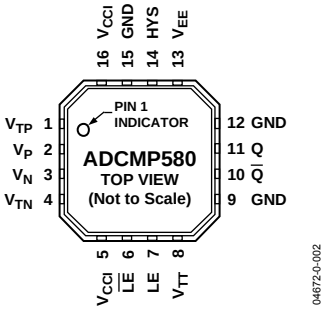

Figure 2. ADCMP580 Pin Configuration

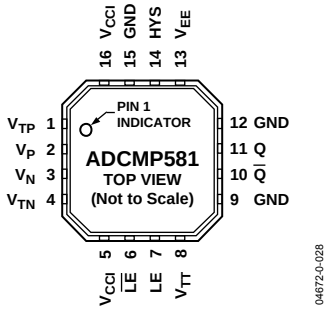

Figure 3. ADCMP581 Pin Configuration

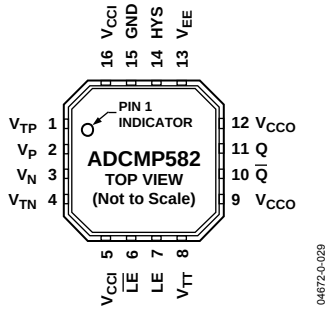

Figure 4. ADCMP582 Pin Configuration

Table 3. Pin Descriptions

Pin No.	Mnemonic	Description
1	V_{TP}	Termination Resistor Return Pin for VP Input.
2	V_P	Noninverting Analog Input.
3	V_N	Inverting Analog Input.
4	V_{TN}	Termination Resistor Return Pin for VN Input.
5, 16	V_{CCI}	Positive Supply Voltage.
6	$\overline{LE}$	Latch Enable Input Pin, Inverting Side. In compare mode ($\overline{LE}$ = low), the output tracks changes at the input of the comparator. In latch mode ($\overline{LE}$ = high), the output reflects the input state just prior to the comparator's being placed into latch mode. $\overline{LE}$ must be driven in compliment with LE.
7	LE	Latch Enable Input Pin, Noninverting Side. In compare mode (LE = high), the output tracks changes at the input of the comparator. In latch mode (LE = low), the output reflects the input state just prior to the comparator's being placed into latch mode. LE must be driven in compliment with $\overline{LE}$.
8	V_{TT}	Termination Return Pin for the LE/$\overline{LE}$ Input Pins. For the ADCMP580 (CML output stage), this pin should be connected to the GND ground. For the ADCMP581 (ECL output stage), this pin should be connected to the −2 V termination potential. For the ADCMP582 (PECL output stage), this pin should be connected to the V_{CCO} − 2 V termination potential.
9, 12	GND/V_{CCO}	Digital Ground Pin/Positive Logic Power Supply Terminal. For the ADCMP580/ADCMP581, this pin should be connected to the GND pin. For the ADCMP582, this pin should be connected to the positive logic power V_{CCO} supply.
10	$\overline{Q}$	Inverting Output. $\overline{Q}$ is logic low if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, V_N, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pins 6 to 7) for more information.
11	Q	Noninverting Output. Q is logic high if the analog voltage at the noninverting input, V_P, is greater than the analog voltage at the inverting input, VN, provided that the comparator is in compare mode. See the LE/$\overline{LE}$ descriptions (Pins 6 to 7) for more information.
13	V_{EE}	Negative Power Supply.
14	HYS	Hysteresis Control. Leave this pin disconnected for zero hysteresis. Connect this pin to the VEE supply with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 9 for proper sizing of the HYS hysteresis control resistor.
15	GND	Analog Ground.
Heatsink	N/C	The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CCI} = +5.0 V, V_{EE} = −5.0 V, V_{CCO} = +3.3 V, T_A = 25°C, unless otherwise noted.

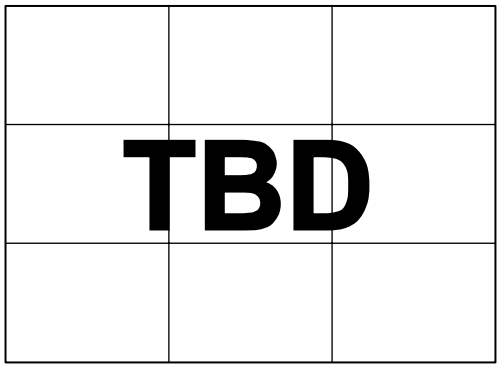

Figure 5. Propagation Delay vs. Input Overdrive

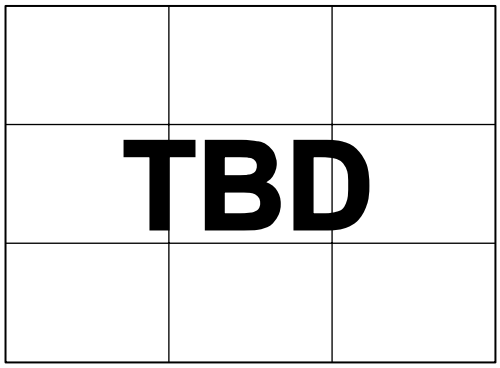

Figure 8. Rise/Fall Time vs. Temperature

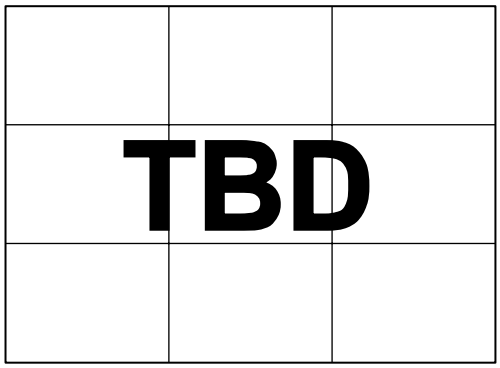

Figure 6. Propagation Delay vs. Input Common Mode

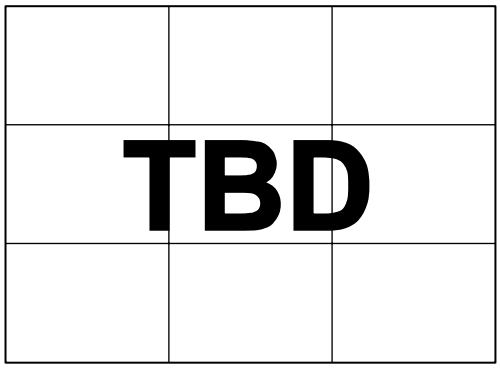

Figure 9. Hysteresis vs. R_{HYS} Control Resistor

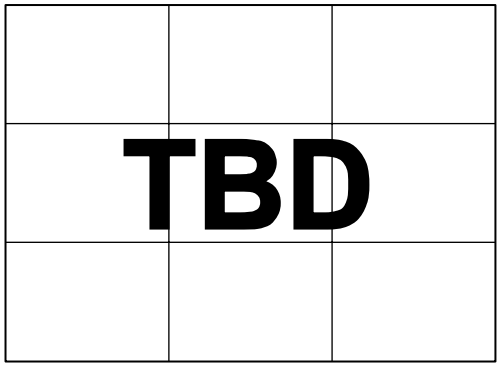

Figure 7. Propagation Delay vs. Temperature

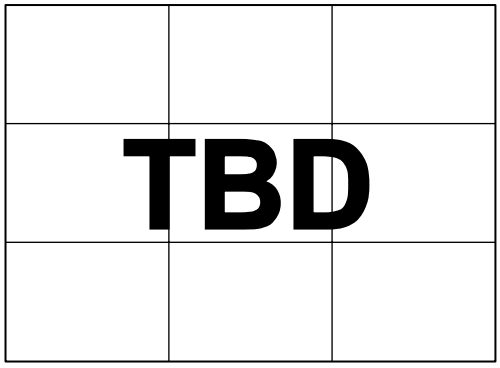

Figure 10. Input Bias Current vs. Input Differential

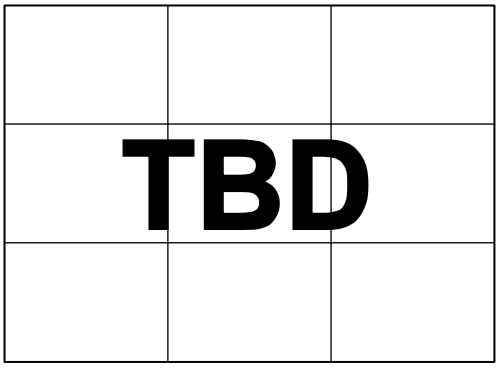

Figure 11. Input Bias Current vs. Temperature

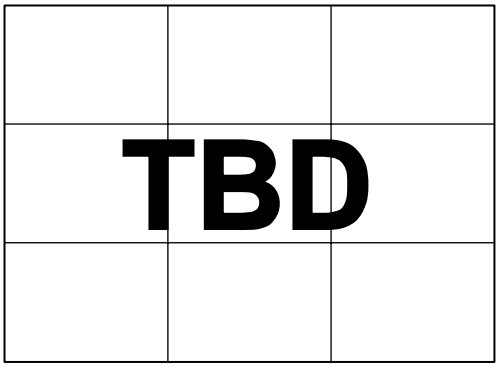

Figure 13. Output Levels vs. Temperature

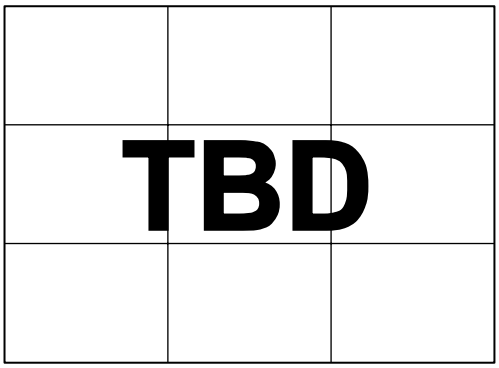

Figure 12. Input Offset Voltages vs. Temperature

APPLICATION INFORMATION

POWER/GROUND LAYOUT AND BYPASSING

The ADCMP58x family of comparators is designed for very high speed applications. Consequently, high speed design techniques must be used to achieve the specified performance. It is critically important to use low impedance supply planes, particularly for the negative supply (V_{EE}), the output supply plane (V_{CCO}) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for the switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. A 1 µF electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, multiple high quality 0.1µF bypass capacitors should be placed as close as possible to each of the V_{EE}, V_{CCI}, and V_{CCO} supply pins and should be connected to the GND plane with redundant vias. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should be strictly avoided to maximize the effectiveness of the bypass at high frequencies.

ADCMP58x FAMILY OF OUTPUT STAGES

Specified propagation delay dispersion performance can be achieved by using proper transmission line terminations. The outputs of the ADCMP580 comparators are designed to directly drive 400 mV into 50 Ω cable or microstrip/stripline transmission lines terminated with 50 Ω referenced to the GND return. The CML output stage is shown in the simplified schematic diagram in Figure 14. The outputs are each back-terminated with 50 Ω for best transmission line matching. The outputs of the ADCMP581/ADCMP582 are illustrated in Figure 15 and should be terminated to −2 V for ECL outputs of ADCMP581 and VCCO − 2 V for PECL outputs of ADCMP582. As an alternative, Thevenin equivalent termination networks may also be used. If high speed CML signals must be routed more than a centimeter, then either microstrip or stripline techniques is required to ensure proper transition times and to prevent excessive output ringing and pulse-width-dependant propagation delay dispersion.

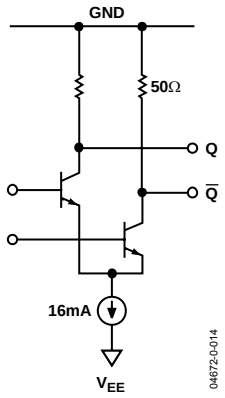

Figure 14. Simplified Schematic Diagram of ADCMP580 CML Output Stage

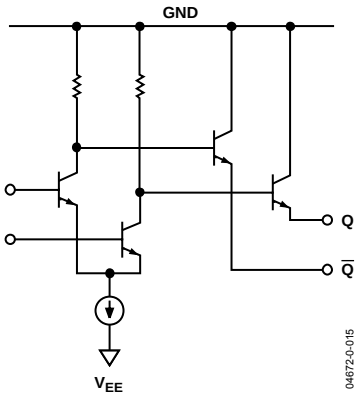

Figure 15. Simplified Schematic Diagram of the ADCMP581/ADCMP582 ECL Output Stage

USING/DISABLING THE LATCH FEATURE

The latch inputs (LE/$\overline{\text{LE}}$) are active low for latch mode, and are internally terminated with 50 Ω resistors to the V_{TT} pin. When using the ADCMP580, V_{TT} should be connected to ground. When using the ADCMP581, V_{TT} should be connected to −2 V. When using the ADCMP582, V_{TT} should be connected externally to V_{CCO} − 2 V, preferably to its own low inductance plane.

When using the ADCMP580/ADCMP582, the latch function can be disabled by connecting the $\overline{\text{LE}}$ pin to V_{EE} with an external pull-down resistor and leaving the LE pin unconnected. To prevent excessive power dissipation, the resistor should be 1.5 kΩ. When using the ADCMP581 comparators, the latch can be disabled by connecting the LE pin to GND with an external 450 Ω resistor, and leaving the $\overline{\text{LE}}$ pin disconnected.

OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and can cause oscillation. Discontinuities along input and output transmission lines can also severely limit the specified pulse width dispersion performance.

For applications working in a 50 Ω environment, input and output matching have a significant impact on data-dependant (or deterministic) jitter (DJ) and pulse width dispersion performance. The ADCMP58x family of comparators provides internal 50 Ω termination resistors for both V_P and V_N inputs. The return side for each termination is pinned out separately with the V_{TP} and V_{TN} pins, respectively. If the a 50 Ω termination is desired at one or both of the V_P/V_N inputs, the V_{TP} and V_{TN} pins can be connected (or disconnected) to (from) the desired termination potential as appropriate. The termination potential should be carefully bypassed using ceramic capacitors as discussed previously to prevent undesired aberrations on the input signal due to parasitic inductance in the termination return path. If a 50 Ω termination is not desired, either one or both of the V_{TP}/V_{TN} termination pins can be left disconnected. In this case, the open pins should be left floating with no external pull downs or bypassing capacitors.

For applications that require high speed operation, but do not have on-chip 50 Ω termination resistors, some reflections should be expected because the comparator inputs can no longer provide matched impedance to the input trace leading up to the device. It then becomes important to back-match the drive source impedance to the input transmission path leading to the input to minimize multiple reflections. For applications in which the comparator is very close to the driving signal source, the source impedance should be minimized. High source impedance in combination with parasitic input capacitance of the comparator could cause undesirable degradation in bandwidth at the input, thus degrading the overall response. Although the ADCMP58x family of comparators has been designed to minimize input capacitance, some parasitic capacitance is inevitable. It is therefore recommended that the drive source impedance should be no more than 50 Ω for best high speed performance.

COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP58x family of comparators has been specifically designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to 500 mV. Propagation delay dispersion is a change in propagation delays, which results from a change in the degree of overdrive or slew rate (how far or fast the input signal exceeds the switching threshold). The overall result is a higher degree of timing accuracy.

Propagation delay dispersion is a specification which becomes important in critical timing applications such as data communication, automatic test and measurement, instrumentation, and event driven applications such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in the overall propagation delay as the input overdrive conditions are changed (Figure 16 and Figure 17). For the ADCMP58x family of comparators, dispersion is typically < 25 ps since the overdrive varies from 5 mV to 500 mV, and the input slew rate varies from 1 V/ns to 10 V/ns. This specification applies for both positive and negative signals since the ADCMP58x family of comparators has almost equal delays for positive- and negative-going inputs.

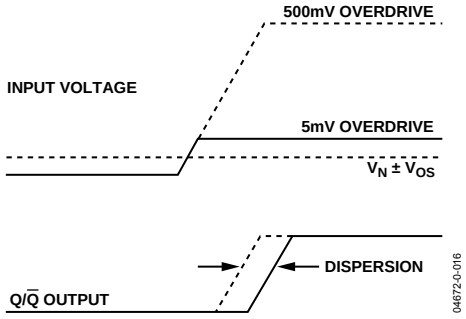

Figure 16. Propagation Delay—Overdrive Dispersion

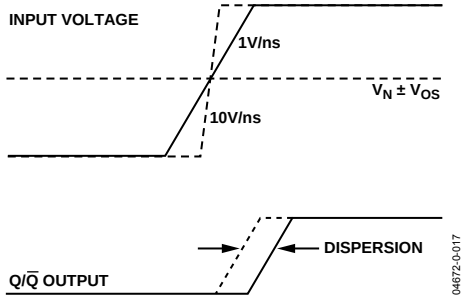

Figure 17. Propagation Delay—Slew Rate Dispersion

COMPARATOR HYSTERESIS

Adding hysteresis to a comparator is often desirable in a noisy environment or when the differential inputs are very small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 18. If the input voltage approaches the threshold from the negative direction, the comparator switches from a low to a high when the input crosses $+V_H/2$. The new switching threshold becomes $-V_H/2$. The comparator remains in the high state until the threshold $-V_H/2$ is crossed coming from the positive direction. In this manner, noise centered on 0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. A limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that will reduce high speed performance, and can even reduce overall stability in some cases.

The ADCMP58x family of comparators offers a programmable hysteresis feature that can significantly improve the accuracy and stability of the desired hysteresis. By connecting an external pull-down resistor from the HYS pin to V_{EE}, a variable amount of hysteresis can be applied. Leaving the HYS pin disconnected disables the feature and hysteresis is then less than 1 mV as specified. The maximum range of hysteresis that can be applied by using this method is approximately ±25 mV.

Figure 19 illustrates the amount of applied hysteresis as a function of external resistor value. The advantage of applying hysteresis in this manner is improved accuracy, stability, and reduced component count. An external bypass capacitor is not required on the HYS pin because it would likely degrade the jitter performance of the device.

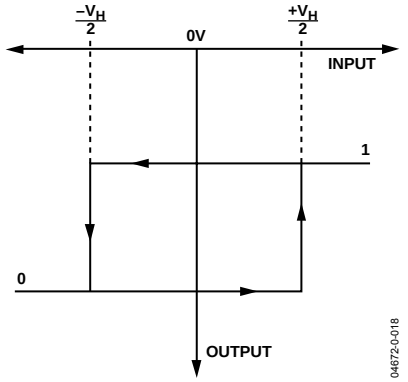

Figure 18. Comparator Hysteresis Transfer Function of the ADCMP580/ADCMP581

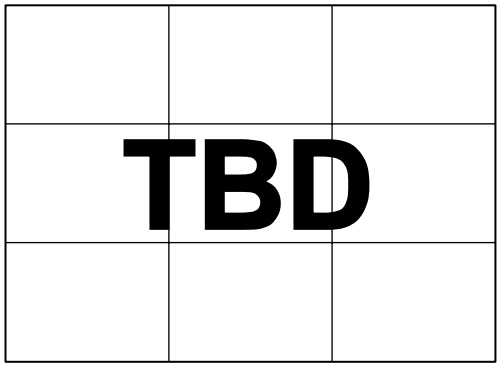

Figure 19. Comparator Hysteresis vs. R_{HYS} Control Resistor

MINIMUM INPUT SLEW RATE REQUIREMENT

As with all high speed comparators, a minimum slew rate must be met to ensure that the device does not oscillate when the input signal crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the feedback parasitics inherent in the package. Analog Devices recommends a minimum slew rate of 50 V/µs to ensure a clean output transition from the ADCMP58x family of comparators unless hysteresis is programmed as discussed previously.

TYPICAL APPLICATION CIRCUITS

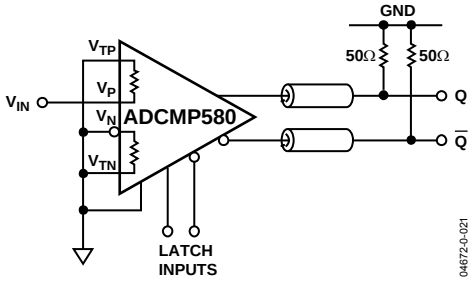

Figure 20. Zero-Crossing Detector with CML Outputs

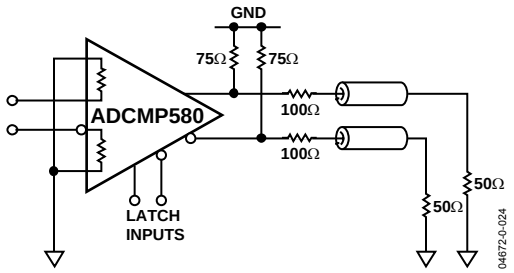

Figure 21. Interfacing CML to a 50 Ω Ground-Terminated Instrument

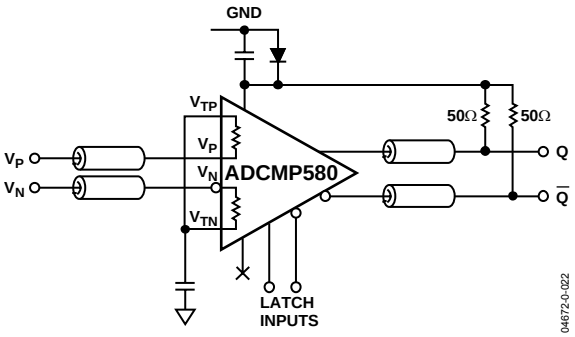

Figure 22. LVDS to a 50 Ω Back-Terminated (RS)ECL Receiver

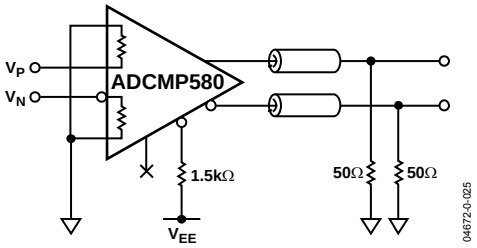

Figure 23. Disabling the Latch Feature

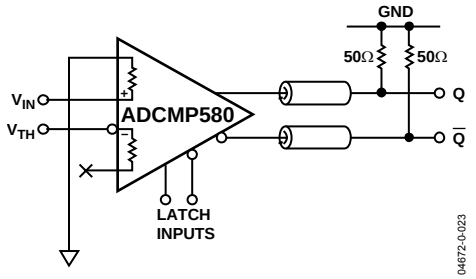

Figure 24. Comparator with –2 V to +3 V Input Range

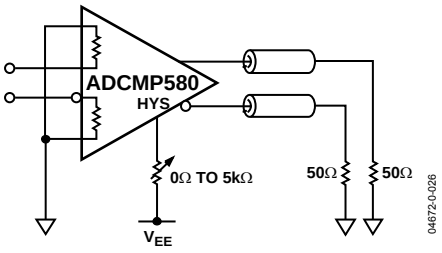

Figure 25. Adding Hysteresis Using the HYS Control

TIMING INFORMATION

Figure 26 shows the ADCMP580/ADCMP581/ADCMP582 compare and latch timing relationships. Table 4 provides a definition of the terms shown in the figure.

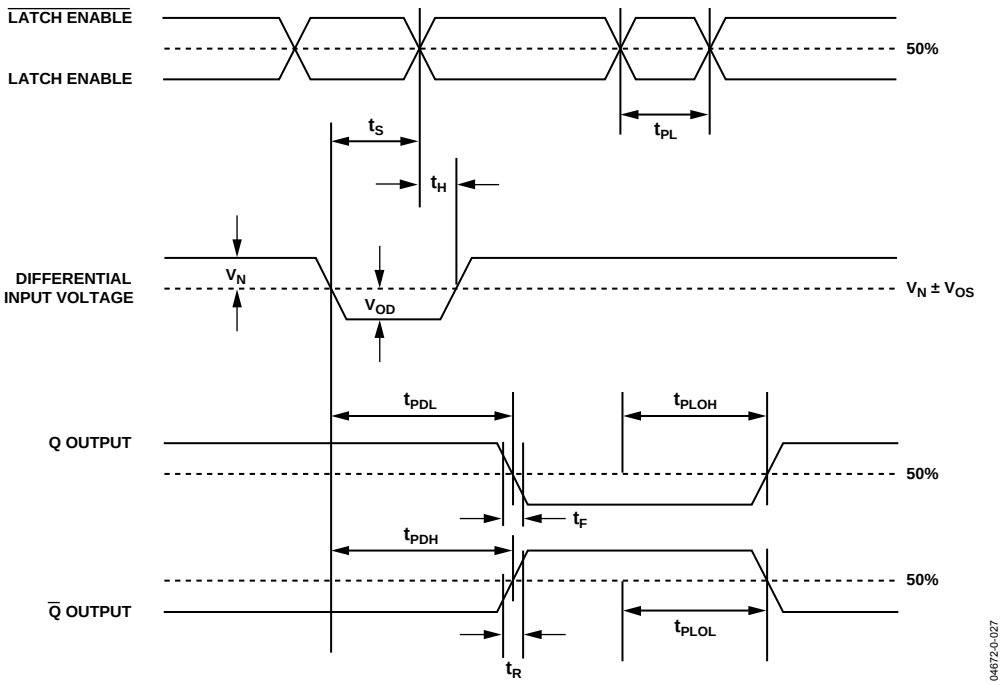

Figure 26. Comparator Timing Diagram

Table 4. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the Latch Enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the Latch Enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the Latch Enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the negative transition of the Latch Enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_P and V_N.

OUTLINE DIMENSIONS

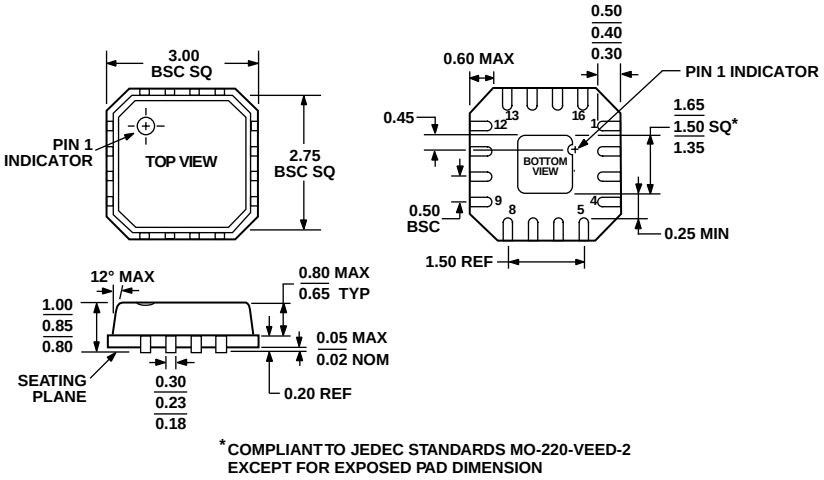

Figure 27. 16-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADCMP580BCP	–40°C to +85°C	LFCSP-16	CP-16
ADCMP581BCP	–40°C to +85°C	LFCSP-16	CP-16
ADCMP582BCP	–40°C to +85°C	LFCSP-16	CP-16

NOTES

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