Quad I/Q Demodulator And Phase Shifter

Preliminary Technical Data

AD8339

FEATURES

Quad Integrated I/Q Demodulator
16 Phase Select on each Output (22.5° per step)
Quadrature Demodulation Accuracy
Phase Accuracy ±1°
Amplitude Balance ±0.25 dB
Bandwidth
4LO: LF – 100 MHz; RF: LF - 25 MHz
Baseband: determined by external filtering
Output Dynamic Range 158 dB (1 Hz Bandwidth)
LO Drive > –10 dBm (50 Ω); 200 mVpp
Supply: ±5 V
Power Consumption 73 mW/channel (290 mW total)
Power Down via SPI (Each Channel and Complete Chip)

APPLICATIONS

Medical Imaging (CW Ultrasound Beamforming)
Phased Array Systems
Radar
Adaptive Antennas
Communication Receivers

FUNCTIONAL BLOCK DIAGRAM

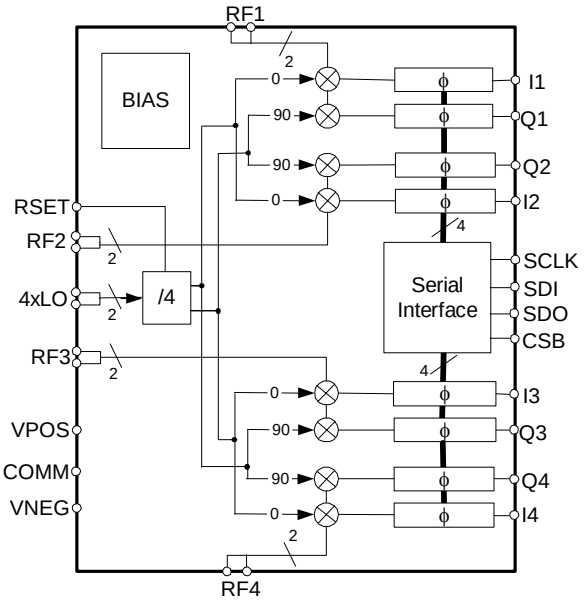

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The AD8339 is a Quad I/Q demodulator intended to be driven by a low noise preamplifier with differential outputs; it is optimized for the LNA in the AD8332/4/5 family of VGAs. The part consists of four identical I/Q demodulators with a 4x local oscillator (LO) input that divides this signal and generates the necessary 0° and 90° phases of the internal LO that drive the mixers. The four I/Q demodulators can be used independently of each other (assuming that a common LO is acceptable) since each has a separate RF input.

The major application is continuous wave (CW) analog beamforming in ultrasound. Since in a beamforming application the outputs of many channels are summed coherently, the signals need to be phase aligned. A reset pin for the LO divider that synchronizes multiple ICs to start in the same quadrant is provided. Sixteen discrete phase rotations in 22.5° increments can be selected independently for each channel. For example, if CH1 is used as a reference and CH2 has an I/Q phase lead of 45°, then by choosing the correct code one can phase align CH2 with CH1.

The mixer outputs are provided in current form so that they can be easily summed. The summed current outputs, one each for the I and Q signals, will need to be converted to a voltage by a high dynamic range current-to-voltage (I-V) converter. A good choice for this transimpedance amplifier is the AD8021 because of its low noise. Following the current summation the combined signal is presented to a high resolution AD converter (ADC) like the AD7665 (16b/570 ksps).

An SPI compatible serial interface is provided for ease of programming the phase of each channel; the interface allows daisy-chaining by shifting the data through each chip from SDI to SDO. The SPI also allows for power down of each individual channel and the complete chip. During power down the serial interface remains active so that the device can be programmed again.

The dynamic range is >158 dB (1 Hz BW) at the I and Q outputs. Note that the following transimpedance amplifier is an important element in maintaining this dynamic range and attention needs to be paid to component selection.

The AD8339 will be available in a 6x6 mm 40 pin LFCSP for the industrial temperature range of -40°C to +85°C.

Rev. PrA - 12/19/06

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REVISION HISTORY

12/19/06 – Rev. Prelim A1

AD8339 SPECIFICATIONS

Table 1. V_S = ±5 V, T_A = 25°C, 4 f_{LO} = 20 MHz, f_{RF} = 5.01 MHz, f_{BB} = 10 kHz, P_{LO} ≥ 0 dBm, per channel performance, dBm (50 Ω) unless otherwise noted. Single channel AD8021 LPF values R_{FILT} = 1.58 kΩ and C_{FILT} = 1 nF (see Figure 2).

Parameter	Conditions	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	4x internal LO at pins **4LOP** and **4LON**				
	Square Wave	LF		100	MHz
	Sine Wave	TBD		100	MHz
RF Frequency Range	Mixing	LF		25	MHz
Baseband Bandwidth	Limited by external filtering	LF		25	MHz
LO Input Level			0	13	dBm
V_{SUPPLY} (V_S)		±4.5	±5	±5.5	V
Temperature Range		-40		+85	°C
DEMODULATOR PERFORMANCE					
Input Impedance	RF - Differential		7||7		kΩ||pF
	LO – Differential		100||1		kΩ||pF
Transconductance	Demodulated I_{OUT}/V_{IN}; Each Ix or Qx output after low pass filtering measured from RF inputs				
	All Phases		1.1		mS
Dynamic Range	IP1dB minus Input referred noise (dBm)		158		dB (1Hz BW)
Max Input Swing	Differential; Inputs biased at 2.5V; Pins **RFxP**, **RFxN**		2.7		Vpp
Peak Output Current (No Filtering)	0° Phase Shift		±2.4		mA
	45° Phase Shift		±3.3		mA
Input P1dB	Ref = 50 Ω		14.5		dBm
	Ref = $1V_{RMS}$		1.5		dBV
Third Order Intermodulation (IM3)	f_{RF1} = 5.010 MHz, f_{RF2} = 5.015 MHz, f_{LO} = 5.023 MHz				
Equal Input Levels	Baseband tones: -7 dBm @ 8 kHz and 13 kHz		-75		dBc
Unequal Input Levels	Baseband tones: -1 dBm @ 8 kHz and -31 dBm @13 kHz		TBD		dBc
Third Order Input Intercept (IIP3)	Same conditions as IM3		30		dBm
LO Leakage	Measured at RF inputs, worst phase, measured into 50 Ω		TBD		dBm
	Measured at baseband outputs, worst phase, AD8021 disabled, measured into 50 Ω		TBD		dBm
Conversion Gain	All codes, see Figure XX		4.7		dB
Input Referred Noise	Output Noise ÷ Conversion Gain (see Figure XX)		TBD		nV/√Hz
Output Current Noise	Output noise ÷ 1.58 kΩ		TBD		pA/√Hz
Noise Figure	With AD8332 LNA				
	R_S = 50 Ω, R_{FB} = ∞		TBD		dB
	R_S = 50 Ω, R_{FB} = 1.1k Ω		TBD		dB
	R_S = 50 Ω, R_{FB} = 274 Ω		TBD		dB
Bias Current	Pins 4**LOP** and 4**LON**		-2		µA
	Pins **RFxP** and **RFxN**		-35		µA
LO Common Mode Range Range	Pins 4**LOP** and 4**LON** (each pin)	0.2		3.8	V
RF Common Mode Voltage	For maximum differential swing; Pins **RFxP** and **RFxN** (DC-coupled to AD8332 output)		2.5		V
Output Compliance Range	Pins **IxOP** and **QxOP**	-1.5		0.7	V

PHASE ROTATION PERFORMANCE	One CH is reference, others are stepped				
Phase Increment	16 Phase Steps per Channel		22.5		°
Quadrature Phase Error	Ix to Qx; all phases, 1σ		±1		°
I/Q Amplitude Imbalance	Ix to Qx; all phases, 1σ		0.25		dB
Channel-to-Channel Matching	Phase Match I-to-I and Q-to-Q; -40°C < T_A < 85°C		±1		°
	Ampl. Match I-to-I and Q-to-Q; -40°C < T_A < 85°C		±0.5		dB
LOGIC INTERFACES	Pins **SDI, CSB, SCLK, RSTS, RSET**				
Logic Level High		1.5			V
Logic Level Low				0.9	V
Bias Current	Logic High (pulled to +5V)		0.5		µA
	Logic Low (pulled to GND)		0		µA
Input Resistance			4		MΩ
LO Divider RSET Setup Time	RSET rising edge to 4LOP-4LON (Differential) rising edge	5			ns
LO Divider RSET High Pulse Width		20			ns
LO Divider RSET Setup Time	RSET falling edge prior to 4LOP-4LON (Differential) rising edge	5			ns
Phase Response Time	Measured from **CSB** going high		TBD		µs
Enable Response Time	Measured from **CSB** going high (with 0.1 µF cap on pin LODC)	15			µs
Output	Pin **SDO**				
Logic Level High	Loaded with 5 pF and next SDI input	1.7	1.9		V
Logic Level Low	Loaded with 5 pF and next SDI input		0.2	0.5	V
SPI TIMING CHARACTERISTICS	Pins **SDI, SDO, CSB, SCLK, RSTS**				
SCLK Frequency	f_{CLK}			10	MHz
CSB to SCLK Setup Time	T_1	TBD			ns
SCLK High Pulse Width	T_2	TBD			ns
SCLK Low Pulse Width	T_3	TBD			ns
Data Access Time after SCLK Falling Edge	T_4			TBD	ns
Data Setup Time Prior to SCLK Rising Edge	T_5	TBD			ns
Data Hold Time after SCLK Rising Edge	T_6	TBD			ns
CSB High Pulse Width	T_7	TBD			ns
SCLK Fall to CSB Fall Hold Time	T_8	TBD			ns
SCLK Fall to CSB Rise Hold Time	T_9	TBD			
POWER SUPPLY	Pins **VPOS, VNEG**				
Supply Voltage		±4.5	±5	±5.5	V
Quiescent Current	VPOS, all phase bits = 0		37.5		mA
	VNEG, all phase bits = 0		-21		mA
Over Temperature	-40°C < T_A < 85°C	TBD		TBD	mA
Quiescent Power	Per Channel, all phase bits = 0		73		mW
	Per Channel max (depends on phase bits)		TBD		mW
Disable Current	All Channels Disabled; SPI stays on		2.6		mA
PSRR	VPOS to Ix/Qx outputs (meas. @ AD8021 output)		TBD		dB
	VNEG to Ix/Qx outputs (meas. @ AD8021 output)		TBD		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Voltages	
Supply Voltage V_S	±6 V
RF Inputs	+6 V, GND
4LO Inputs	+6 V, GND
Outputs (IxOP, QxOP)	+1 V, -6 V
Digital Inputs	+6 V, GND
SDO Output	+6 V, GND
LODC Pin	+6 V (max) VPOS –1.5 V (min)
Thermal Data —4 Layer Jedec Board No Air Flow (Exposed Pad Soldered to PC Board)	
θ_{JA}	TBD°C/W
θ_{JB}	TBD°C/W
θ_{JC}	TBD°C/W
Ψ_{JT}	TBD°C/W
Ψ_{JB}	TBD°C/W
Maximum Junction Temperature	150°C
Maximum Power Dissipation (Exposed Pad Soldered to PC Board)	TBD W
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

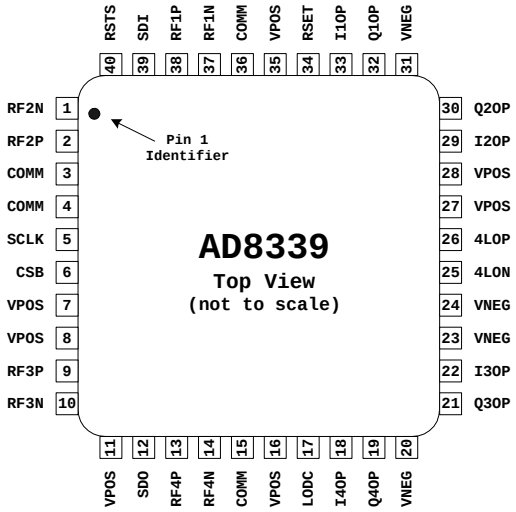

Figure 2. 40-Lead LFCSP

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 9, 10, 13, 14, 37, 38	RF1P-RF4P RF1N-RF4N	RF Inputs. No internal bias. The optimum common mode voltage for maximum symmetrical input differential swing is 2.5 V if ±5 V supplies are used.
3, 4, 15, 36	COMM	Ground
5	SCLK	Serial Interface – Clock
6	CSB	Serial Interface – Chip Select Bar. Active Low.
7, 8, 11, 16, 27, 28, 35	VPOS	Positive Supply. These pins should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 1 nF capacitor between the VPOS pins and ground. Since the VPOS pins are internally connected, one set of supply decoupling components on each side of the chip should be sufficient.
12	SDO	Serial Interface – Data Output. Normally connected to SDI of next chip or left open.
17	LODC	Decoupling Pin for LO. A 0.1 μF capacitor should be connected between this pin and ground. Value of cap does influence chip enable/disable times.
18, 19, 21, 22, 29, 30, 32, 33	I1OP-I4OP, Q1OP-Q4OP	I/Q Outputs. These outputs provide a bidirectional current that can be converted back to a voltage via a transimpedance amplifier. Multiple outputs can be summed together through simply connecting them (Wire-OR). The bias voltage should be set to 0 V or less by the transimpedance amplifier, see Figure 7.
20, 23, 24, 31	VNEG	Negative Supply. These pin should be decoupled with a ferrite bead in series with the supply, plus a 0.1 μF and 1 nF capacitor between the pin and ground. Since the VNEG pins are internally connected, one set of supply decoupling components should be sufficient.
25, 26	4LOP, 4LON	LO Inputs. No internal bias; optimally biased by an LVDS driver. For best performance, these inputs should be driven differentially.
34	RSET	LO Interface - Reset. Logic threshold is at about 1.1 V and therefore can be driven by >1.8 V CMOS logic.
39	SDI	Serial Interface – Data Input. Logic threshold is at about 1.1 V and therefore can be driven by >1.8 V CMOS logic.
40	RSTS	Reset for SPI Interface. Logic threshold is at about 1.1 V and therefore can be driven by >1.8 V CMOS logic. For quick testing without the need to program the SPI, the voltage on the RSTS pin should be pulled to -1.4 V; this enables all four channels in the Phase (I=1,Q=0) state.

EQUIVALENT INPUT CIRCUITS

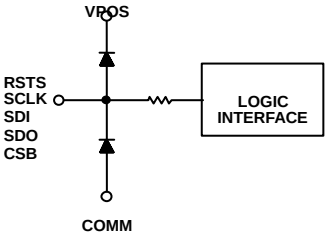

Figure 3. Logic Inputs

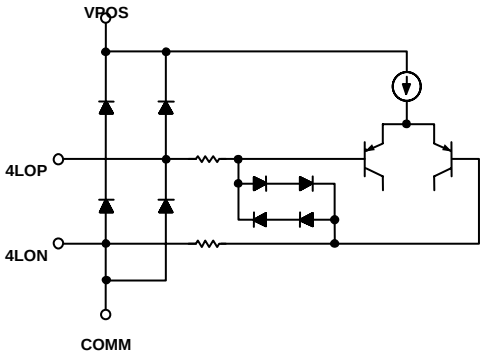

Figure 4. Local Oscillator Inputs

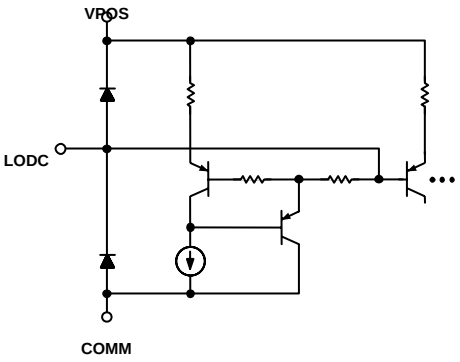

Figure 5. LO Decoupling Pin

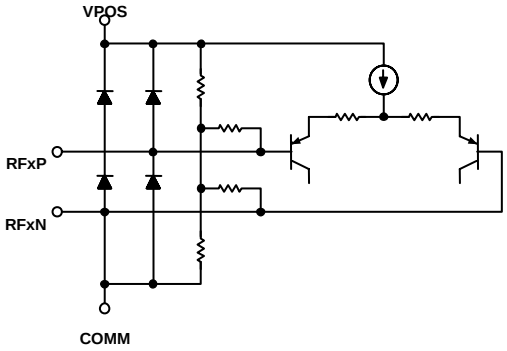

Figure 6. RF Inputs

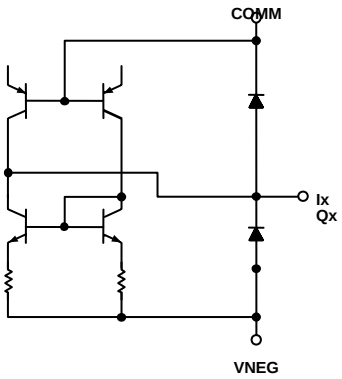

Figure 7. Output Drivers

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T_A = 25°C, $4f_{LO}$ = 20 MHz, f_{LO} = 5 MHz, f_{RF}= 5.01 MHz, f_{BB} = 10 kHz, $P_{LO} \geq 0$ dBm (50Ω); single-ended sine wave; per channel performance, differential voltages, dBm (50Ω), phase select code = 0000, unless otherwise noted (see **Error! Reference source not found.**).

TEST CIRCUITS

THEORY OF OPERATION

The AD8339 is a quad I/Q demodulator with a programmable phase shifter for each channel. The primary application is phased array beamforming in medical ultrasound. Other potential applications might be phased array radar, and smart antennas for mobile communications. The AD8339 can also be used in applications that require multiple well-matched I/Q demodulators. The AD8339 is architecturally very similar to its predecessor – the AD8333. The major differences are:

1. the addition of a serial (SPI) interface that allows daisy-chaining of multiple devices
2. reduced power per channel at the expense of a slight decrease in dynamic range

Figure 1 shows the block diagram and pinout of the AD8339. Four RF inputs accept signals from the RF sources, and a local oscillator (applied to differential input pins marked 4LOP and 4 LON) common to all channels, comprise the analog inputs. Each channel has the option to program 16 delay states/360° (or 22.5°/step) selectable via the SPI port. The part has two reset inputs: RSET is used to synchronize the LO dividers in multiple AD8339s used in arrays; RSTS is used to set the SPI port bits to all zeros. This can be useful in testing or when one quickly wants to turn off the device without first programming the SPI port.

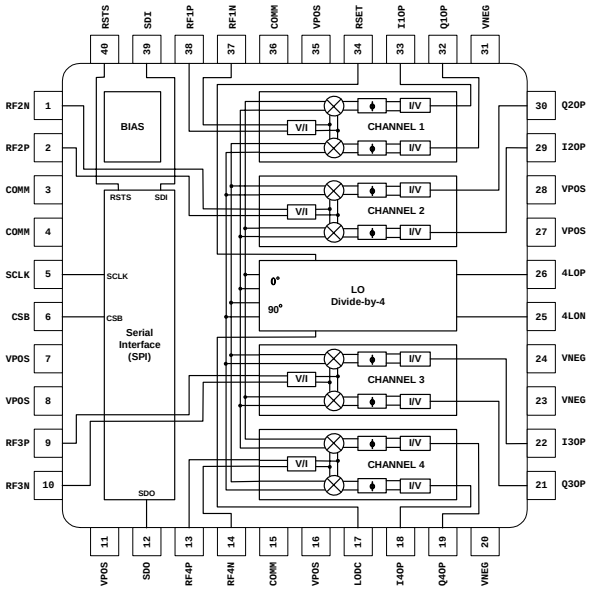

Figure 1. Block Diagram and Pinout

Each of the current formatted I and Q outputs sum together for beamforming applications. Multiple channels are summed and converted to a voltage using a transimpedance amplifier. If desired, channels can also be used individually.

QUADRATURE GENERATION

The internal 0° and 90° LO phases are digitally generated by a divide-by-four logic circuit. The divider is dc-coupled and inherently broadband; the maximum LO frequency is limited only by its switching speed. The duty cycle of the quadrature LO signals is intrinsically 50% and is unaffected by the asymmetry of the externally connected 4xLO input. Furthermore, the divider is implemented such that the 4xLO signal re-clocks the final flip-flops that generate the internal LO signals and thereby minimizes noise introduced by the divide circuitry.

For optimum performance, the 4xLO input is driven differentially, but can also be driven single-ended. A good choice for a drive is an LVDS device. The common-mode range on each pin is approximately 0.2 V to 3.8 V with the nominal ±5 V supplies.

The minimum 4xLO level is frequency dependent. For optimum noise performance it is important to ensure that the LO source has very low phase noise (jitter) and adequate input level to assure stable mixer-core switching. The gain through the divider determines the LO signal level vs. RF frequency. The AD8339 can be operated to very low frequencies at the LO inputs if a square wave is used to drive the LO.

Beamforming applications require a precise channel-to-channel phase relationship for coherence among multiple channels. A reset pin is provided to synchronize the LO divider circuits in different AD8339s when they are used in arrays. The RSET pin resets the dividers to a known state after power is applied to multiple AD8339s. A logic input must be provided to the RSET pin when using more than one AD8339. Note that at least one channel must be enabled for the LO interface to also be enabled and the LO reset to work. See the Reset Input section in the applications section for more detail.

I/Q DEMODULATOR AND PHASE SHIFTER

The I/Q demodulators consist of double-balanced Gilbert cell mixers. The RF input signals are converted into currents by transconductance stages that have a maximum differential input signal capability of 2.7 V p-p. These currents are then presented to the mixers, which convert them to baseband: RF − LO and RF + LO. The signals are phase shifted according to the codes programmed into the SPI latch (see Table 4); the phase bits are labeled PHx0 through PHx3 where '0' indicates LSB and '3' indicates MSB. The phase shift function is an integral part of the overall circuit (patent pending). The phase shift listed in Column 1 of Table 4 is defined as being between the baseband I or Q channel outputs. As an example, for a common signal applied to a pair of RF-inputs to an AD8339, the baseband outputs are in phase for matching phase codes. However, if the phase code for Channel 1 is 0000 and that of Channel 2 is 0001, then Channel 2 leads Channel 1 by 22.5°.

Following the phase shift circuitry, the differential current signal is converted from differential to single-ended via a

current mirror. An external transimpedance amplifier is needed to convert the I and Q outputs to voltages.

Table 4. Phase Select Code for Channel-to-Channel Phase Shift

ϕ-Shift	PHx3 (MSB)	PHx2	PHx1	PHx0 (LSB)
0°	0	0	0	0
22.5°	0	0	0	1
45°	0	0	1	0
67.5°	0	0	1	1
90°	0	1	0	0
112.5°	0	1	0	1
135°	0	1	1	0
157.5°	0	1	1	1
180°	1	0	0	0
202.5°	1	0	0	1
225°	1	0	1	0
247.5°	1	0	1	1
270°	1	1	0	0
292.5°	1	1	0	1
315°	1	1	1	0
337.5°	1	1	1	1

DYNAMIC RANGE AND NOISE

Figure 2 is an interconnection block diagram of two channels (1/2 of the AD8339), more channels are easily added to the summation (up to 16 when using an AD8021 as the summation amplifier) by wire-or connecting the outputs as shown for two channels. For optimum system noise performance, the RF input signal is provided by a very low noise amplifier such as the LNA of the AD8332/AD8334 or the preamplifier of the AD8335. In beamformer applications, the I and Q outputs of a number of receiver channels are summed (for example, the two channels illustrated in Figure 2). The dynamic range of the system increases by the factor $10\log_{10}(N)$, where N is the number of channels (assuming random uncorrelated noise.) The noise in the two channel example of Figure 2 is increased by 3 dB while the signal doubles (+6 dB), yielding an aggregate SNR improvement of (+6 − 3) = +3 dB. For four channels the dynamic range will increase by +6 dB and so on.

Judicious selection of the RF amplifier ensures the least degradation in dynamic range. The input referred spectral voltage noise density (e_n) of the AD8339 is nominally about ***TBD*** nV/√Hz. For the noise of the AD8339 to degrade the system noise figure (NF) by 1 dB, the combined noise of the source and the LNA should be about twice that of the AD8339 or ***TBD*** nV/√Hz. If the noise of the circuitry before the AD8339 is less than ***TBD*** nV/√Hz then the system NF degrades more than 1 dB. For example, if the noise contribution of the LNA and source is equal to the AD8339, or ***TBD*** nV/√Hz, the degradation is 3 dB. If the circuit noise preceding the AD8339 is 1.3× as large as that of the AD8339 (or about ***TBD*** nV/√Hz) the degradation is 2 dB. For a circuit noise 1.45× that of the AD8339 (***TBD*** nV/√Hz) the degradation is 1.5 dB.

To determine the input referred noise it is important to know the active low pass filter (LPF) values R_{FILT} and C_{FILT}, shown in Figure 2. Typical filter values for a single channel are 1.58 kΩ and 1 nF, and implement a 100 kHz single-pole LPF. In the case that two channels are summed as is done on the evaluation board, the values would be the same as for a single channel of the AD8333, namely 787 Ω and 2.2 nF.

If the RF and LO are offset by 10 kHz, the demodulated signal is 10 kHz and is passed by the LPF. The single-channel mixing gain, from the RF input to the AD8021 output (for example, I1′, Q1′) is approximately 1.7 (4.7 dB). This together with the ***TBD*** nV/√Hz of AD8339 noise results in about ***TBD*** nV/√Hz at the AD8021 output. Since the AD8021, including the 1.58 kΩ feedback resistor, contributes another 6.3 nV/√Hz, the total output referred noise is about ***TBD*** nV/√Hz. This value can be adjusted by increasing the filter resistor while maintaining the corner frequency, thereby increasing the gain. The factor limiting the magnitude of the gain is the output swing and drive capability of the op-amp selected for the I-to-V converter, in this instance the AD8021.

Because any amplifier has limited drive capability there will be a finite number of channels that can be summed. This is explained in great detail in the section below called – Channel Summing.

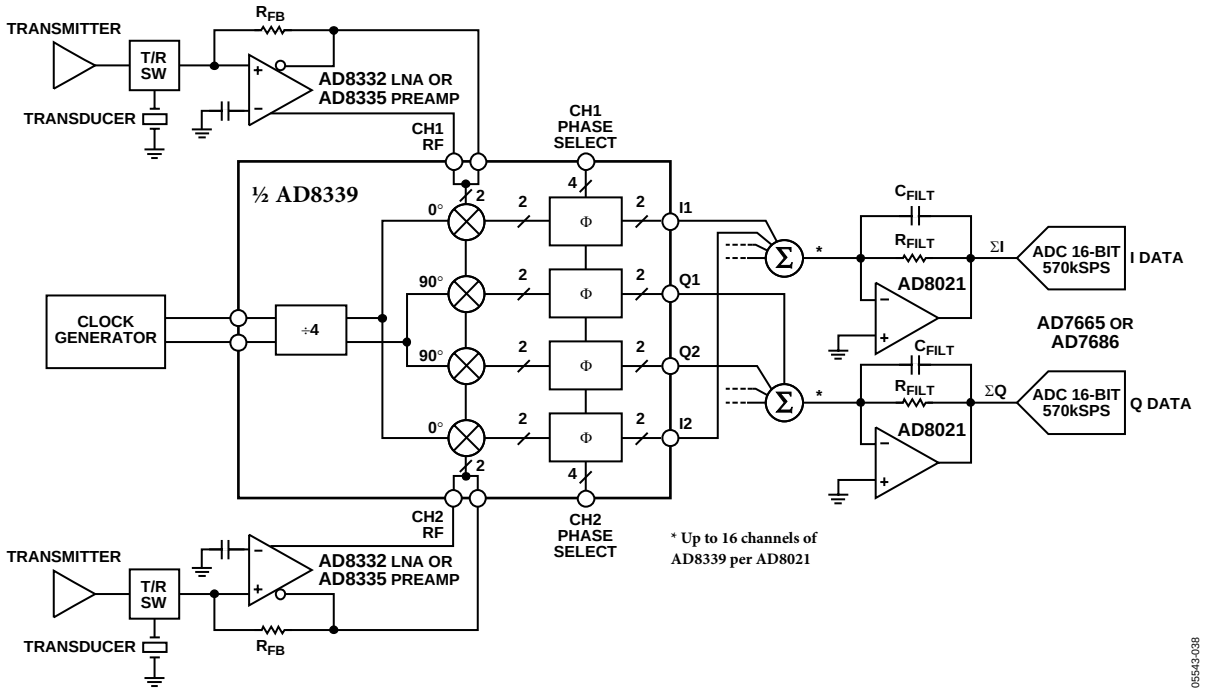

Figure 2. Interconnection Block Diagram for ½ of AD8339

SUMMATION OF MULTIPLE CHANNELS (ANALOG BEAMFORMING)

Beamforming, as applied to medical ultrasound, is defined as the phase alignment and summation of signals generated from a common source, but received at different times by a multi-element ultrasound transducer. Beamforming has two functions: it imparts directivity to the transducer, enhancing its gain and it defines a focal point within the body from which the location of the returning echo is derived. The primary application for the AD8339 is in analog beamforming circuits for ultrasound.

PHASE COMPENSATION AND ANALOG BEAMFORMING

Modern ultrasound machines used for medical applications employ an array of receivers for beamforming, with typical CW Doppler array sizes up to 64 receiver channels phase-shifted and summed together to extract coherent information. When used in multiples, the desired signals from each of the channels can be summed to yield a larger signal (increased by a factor N, where N is the number of channels), while the noise is increased by the square root of the number of channels. This technique enhances the signal to noise performance of the machine. The critical elements in a beamformer design are the means to align the incoming signals in the time domain, and the means to sum the individual signals into a composite whole.

In traditional analog beamformers incorporating Doppler, a V-to-I converter per channel and a cross-point switch precede passive delay lines used as a combined phase shifter and summing circuit. The system operates at the receive frequency (RF) through the delay line which also sums the signals from the various channels, and then the combined signal is down-converted by a very large dynamic range I/Q demodulator.

The resultant I and Q signals are filtered and then sampled by two high resolution AD converters. The sampled signals are processed to extract the relevant Doppler information.

Alternatively, the RF signal can be processed by down-conversion on each channel individually, phase shifting the down-converted signal, and then combining all channels. The AD8333 and the AD8339 provide the means to implement this architecture. The down-conversion is done by an I/Q demodulator on each channel, and the summed current output is the same as in the delay line approach. The subsequent filters after the I-to-V conversion and the AD converters are similar.

The AD8339 integrates the phase shifter, frequency conversion, and I/Q demodulation into a single package, and directly yields the baseband signal.

Figure 3 is a simplified diagram showing the idea for two channels. The ultrasound wave USW is received by two transducer elements, TE1 and TE2, in an ultrasound probe and generates signals E1 and E2. In this example, the phase at TE1 leads the phase at TE2 by 45°.

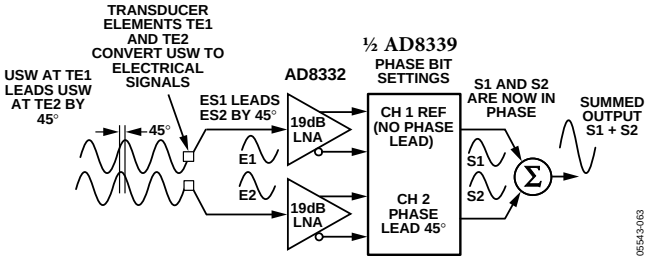

Figure 3. Simplified Example of the AD8339 Phase Shifter

In a real application, the phase difference depends on the element spacing, λ (wavelength), speed of sound, angle of incidence, and other factors. The signals ES1 and ES2 are amplified 19 dB by the low-noise amplifiers in the AD8332; for lower performance portable ultrasound applications, the combination of the AD8335 and the AD8339 result in the lowest power per channel. For optimum signal-to-noise performance, the output of the LNA is applied directly to the input of the AD8339. In order to sum the signals ES1 and ES2, ES2 is shifted 45° relative to ES1 by setting the phase code in Channel 2 to 0010. The phase aligned current signals at the output of the AD8333 are summed in an I-to-V converter to provide the combined output signal with a theoretical improvement in dynamic range of 3 dB for the sum of two channels.

SERIAL INTERFACE

The AD8339 contains a 4-wire SPI compatible digital interface (SDI, SCLK, CSB, and SDO). The interface is comprised of a 20-bit shift register plus a latch. The shift register needs to be loaded MSB first. The data allows control over each channel's phases, plus the last four bits shifted into the register determine the enable state of the individual channels. Figure ***XYZ*** shows a block and timing diagram of the serial interface. The shift direction is to the "right" with MSB first. As soon CSB goes low, the data in the latch is protected and new data can be loaded into the shift register.

If only one AD8339 needs to be programmed, then only 20 bits need to be shifted into the part before CSB goes high. As soon as CSB goes high, the data loaded into the shift register will be transferred to the latch. Depending on the data loaded the corresponding channels will be enabled, and the phases on each channel will be set. Figure ***XYZ*** shows how the timing might look when two AD8339s have their data loaded.

ENBL Bits

If all four ENBL bits are set to '0', then only the SPI port is powered up. This feature allows for very low power consumption (about 13 mW per AD8339 or 3.25 mW per channel) when the CW Doppler function is not needed. Since the SPI port stays alive even when the rest of the chip is powered down, the part can be awakened again by simply programming the port. As soon as the CSB signal goes high, the part turns on again. It should be pointed out that this will take a fair amount of time because of the external capacitor on the LODC pin. It will take about 10-20 µs with the recommended 0.1 µF decoupling cap. The decoupling cap on this pin is intended to reduce bias noise contribution in the LO divider chain. The user can experiment with the value of this decoupling capacitor to see what the smallest value can be without any dynamic range degradation within the frequency band of interest.

The SPI also has an additional pin that can be used in a test mode, or as a quick way to reset the SPI and de-power the chip. All bits in both the shift register and the latch can be reset to '0' when pin RSTS is pulled above about 1.2 V. For quick testing without the need to program the SPI, the voltage on the RSTS pin should be first pulled high and then pulled to -1.4 V; this enables all four channels in the (I=1,Q=0) state (all phase bits are 0000).

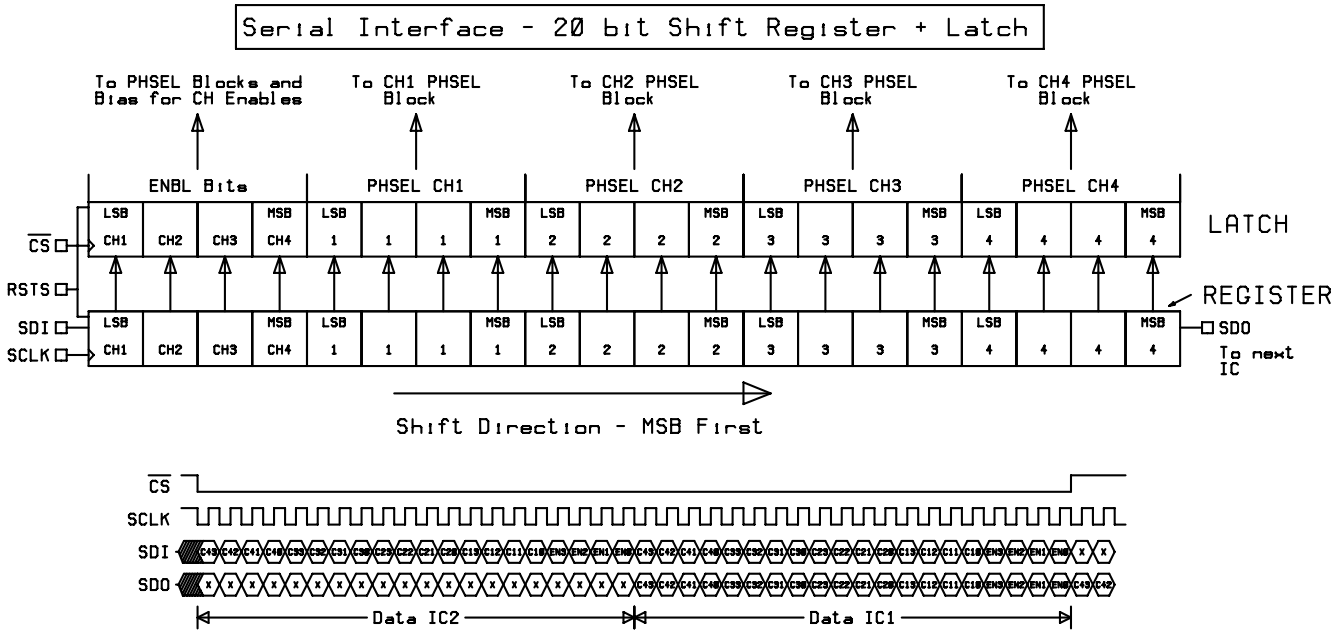

*Figure **XYZ**. SPI - Block and Timing Diagram*

APPLICATIONS

The AD8339 is the key component of a phase-shifter system that aligns time-skewed information contained in RF signals. Combined with a variable gain amplifier (VGA) and low noise amplifier (LNA) as in the AD8334/5 VGA family, the AD8339 forms a complete analog receiver for a high-performance ultrasound system.

LOGIC INPUTS AND INTERFACES

All logic inputs of the AD8339 including the SPI and RSET pins are CMOS compatible down to 1.8 V. Each logic input pin has a Schmitt trigger activated input that contains a threshold that is centered at about 1.1 V with a hysteresis of ±0.1 V around this value.

The LO divider RSET pin has a slightly higher threshold at about 1.3 V and a hysteresis of about ±0.1 V. This input also can still be driven by 1.8 V CMOS logic.

The only logic output, SDO, generates a signal that has a logic low level of about 0.2 V and a logic high level of about 1.9V to allow for easy interfacing to the next AD8339 SDI input.

RESET INPUT

The RSET pin is used to synchronize the LO dividers in AD8339 arrays. Because they are driven by the same internal LO, the four channels in any AD8339 are inherently synchronous. However, when multiple AD8339s are used it is possible that their dividers wake up in different phase states. The function of the RSET pin is to phase align all the LO signals in multiple AD8339s.

The 4 × LO divider of each AD8339 can initiate in one of four possible states - 0°, 90°, 180°, and 270° relative to other AD8339s. The internally generated I/Q signals of each AD8339 LO are always at a 90° angle relative to each other, but a phase shift can occur during power up between the internal LOs of the different AD8339s.

The LO divider reset function has been improved in the AD8339 over the AD8333. The RSET pin still provides an asynchronous reset of the LO dividers by forcing the internal LO to "hang", however, now the LO reset function is fast and does not require a shut-down of the 4 x LO input signal.

The RSET mechanism also allows the measurement of non-mixing gain from the RF input to the output.

The rising edge of the active high RSET pulse can occur at any time; however, the duration should be ≥ 20 ns minimum. When the RSET pulse transitions from high to low, the LO dividers are reactivated on the next rising edge of the 4 x LO clock. To guarantee synchronous operation of an array of AD8339s the RSET pulse needs to go low on all devices before the next rising edge of the 4 x LO clock. Therefore it is best to have the RSET pulse go low on the falling edge of the 4 x LO clock; at the very least the t_{SET-UP} should be ≥ 5 ns. An optimal timing set-up would be for the RSET pulse to go high on a 4 x LO falling edge and go low on a 4 x LO falling edge; this gives 10 ns of set-up time even at a 4 x LO frequency of 50 MHz (12.5 MHz internal LO).

Synchronization of multiple AD8339s can be checked as follows:

1. Activate at least one channel per AD8339 by setting the appropriate channel enable bit in the serial interface.
2. Set the phase code of all AD8339 channels the same, for example, 0000.
3. Apply the same test signal to all devices that generates a sine wave in the baseband output and measure the output of one channel per device.
4. Apply a RSET pulse to all AD8339s.
5. Since all the phase codes of the AD8339s should be the same, the combined signal of multiple devices should be N times bigger than a single channel. If the combined signal is less than N times one channel, then the LO phases of the individual AD8339s are most likely in error.

OUTLINE DIMENSIONS

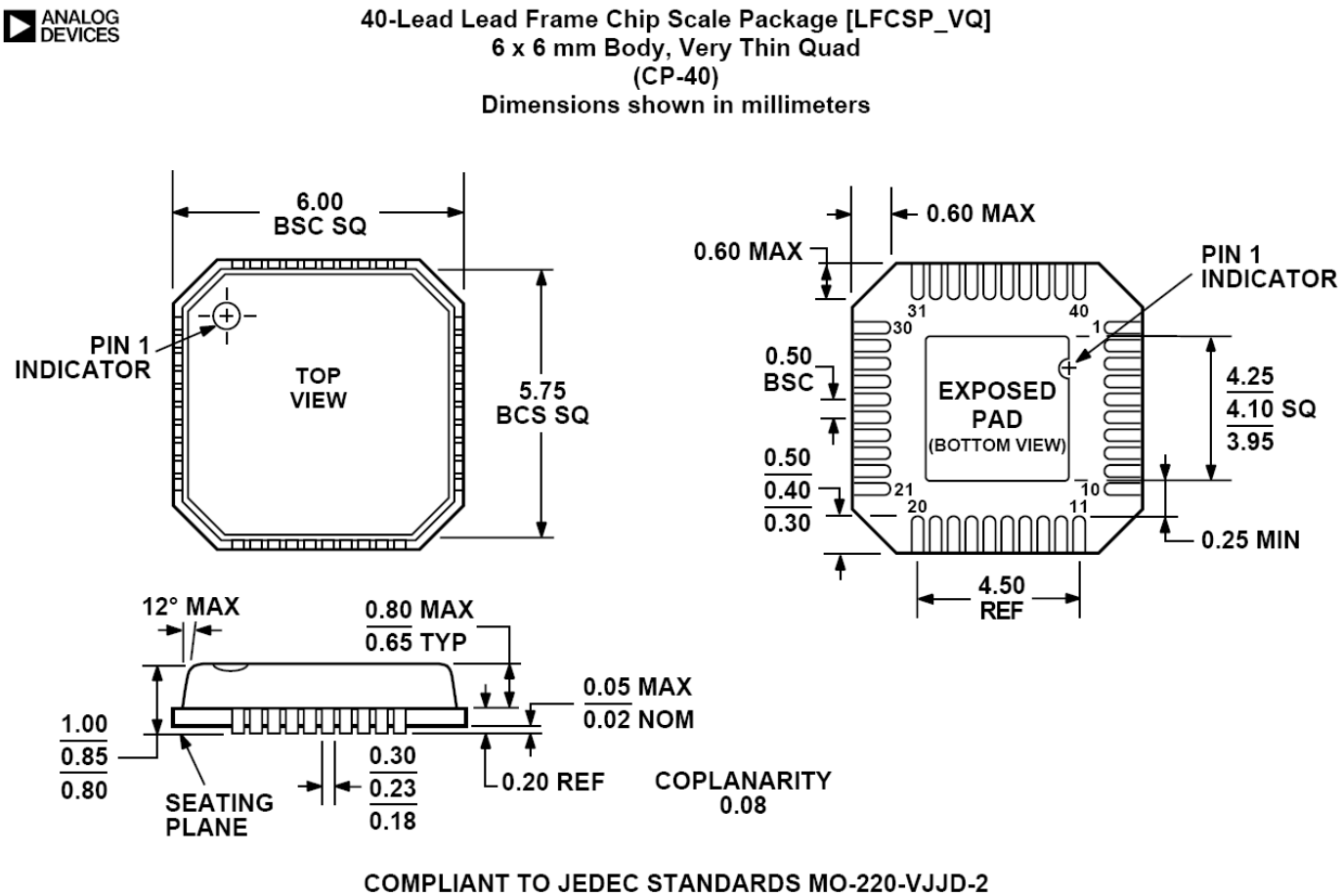

Figure 8. 40-Lead Chip Scale Package