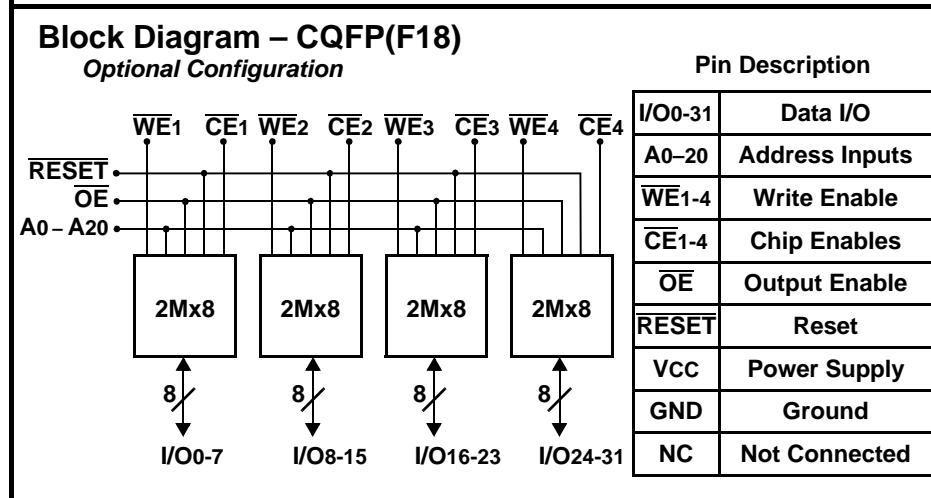
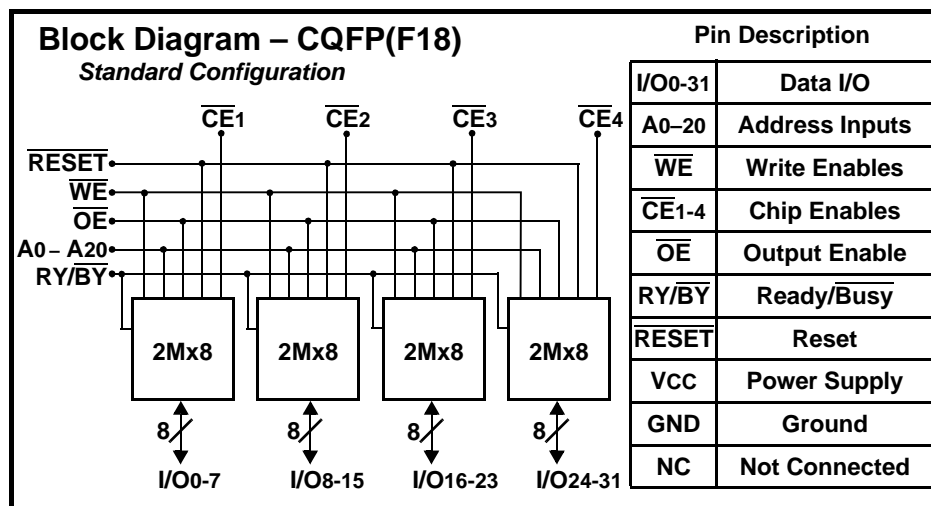


# ACT-F2M32A High Speed 64 Megabit Sector Erase FLASH Multichip Module



## Features

- 4 Low Voltage/Power AMD 2M x 8 FLASH Die in One MCM Package
- Overall Configuration is 2M x 32
- +5V Power Supply / +5V Programming Operation
- Access Times of 90, 120 and 150 ns
- Erase/Program Cycles – 100,000 Minimum
- Sector erase architecture (Each Die)
  - 32 uniform sectors of 64 Kbytes each
  - Any combination of sectors can be erased. Also supports full chip erase
  - Sector group protection is user definable
- Embedded Erase Algorithms – Automatically pre-programs and erases the die or any sector
- Embedded Program Algorithms – Automatically programs and verifies data at specified address
- Ready/Busy output (RY/BY) – Hardware method for detection of program or erase cycle completion
- Hardware RESET pin – Resets internal state machine to the read mode
- Erase Suspend/Resume – Supports reading or programming data to a sector not being erased
- Packaging – Hermetic Ceramic
  - 68 Lead, .94" x .94" x .140" Single-Cavity Small Outline Gull Wing, Aeroflex code# "F18" (Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges
- MIL-PRF-38534 Compliant MCMs Available



## General Description

Utilizing AMD's Sector Erase Flash Memory Die, the ACT-F2M32A is a high speed, 64 megabit CMOS flash multichip module (MCM) designed for full temperature range, military, space, or high reliability applications.

The ACT-F2M32A consists of four high-performance AMD Am29F016 16Mbit (16,777,216 bit) memory die. Each die contains 8 separately write or erase sector groups of 256Kbytes (A sector group consists of 4 adjacent sectors of 64Kbytes each).

The command register is written by bringing WE to a logic low level (V<sub>IL</sub>), while CE is low and OE is high (V<sub>IH</sub>). Reading is accomplished by chip Enable (CE) and Output Enable (OE) being logically active. Access time grades of 90ns, 120ns and 150ns maximum are standard.

## General Description, Cont'd

The ACT-F2M32A is packaged in a hermetically sealed co-fired ceramic 68 lead, .94" SQ Ceramic Gull Wing CQFP package. This allows operation in a military environment temperature range of -55°C to +125°C.

The ACT-F2M32A can be programmed (both read and write functions) in-system using the +5.0V VCC power supply. A 12.0V VPP is not required for programming or erase operations. The end of program or erase is detected by the RY/BY pin, Data Polling of DQ7, or by the Toggle bit (DQ6).

The ACT-F2M32A also has a hardware  $\overline{\text{RESET}}$  pin. When this pin is driven low, execution of any Embedded Program Algorithm or Embedded Erase Algorithm will be terminated.

Each block can be independently erased and programmed 100,000 times at +25°C.

For Detail Information regarding the operation of the Am29F016 Sector Erase Flash Memory, see the AMD datasheet (Publication 18805).

## Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Voltage with Respect to GND (All pins except A9) <sup>(1)</sup>	-2.0 to +7.0	V
Voltage on Pins A9, $\overline{OE}$ , $\overline{RESET}$ <sup>(2)</sup>	-2.0 to +13.5	V
Vcc Supply Voltage with Respect to Ground <sup>(1)</sup>	-2.0 to +7.0	V
Output Short Circuit Current <sup>(3)</sup>	200	mA

Notes:

1. Minimum DC voltage is -0.5V on input/output pins. During Transitions, inputs may undershoot GND to -2.0V for periods up to 20ns. Maximum DC voltage on input/output pins is  $V_{CC} + 0.5V$ , which may overshoot to  $V_{CC} + 2.0V$  for periods up to 20ns.
2. Minimum DC input voltage on A9,  $\overline{OE}$ ,  $\overline{RESET}$  pins is -0.5V. During Voltage transitions, A9,  $\overline{OE}$  &  $\overline{RESET}$  may overshoot GND to -2.0V for periods up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14V for periods up to 20ns.
3. No more than one output shorted to ground for no more than 1 second.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
VCC	5V Power Supply Voltage (10%)	+4.5	+5.5	V
V <sub>IH</sub>	Input High Voltage (CMOS)	0.7 x VCC	$V_{CC} + 0.3$	V
V <sub>IL</sub>	Input Low Voltage	-0.5	+0.8	V
T <sub>C</sub>	Operating Temperature (Military)	-55	+125	°C

## Capacitance

(f = 1MHz, T<sub>C</sub> = 25°C, Standard Configuration)

Symbol	Parameter	Maximum	Units
CAD	A0 – A20 Capacitance	50	pF
COE	$\overline{OE}$ Capacitance	50	pF
CCE	$\overline{CE}$ Capacitance	20	pF
CRESET	$\overline{RESET}$ Capacitance	50	pF
CWE	$\overline{WE}$ Capacitance	60	pF
CRY/ $\overline{BY}$	RY/ $\overline{BY}$ Capacitance	50	pF
CI/O	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

## DC Characteristics – CMOS Compatible

(T<sub>C</sub> = -55°C to +125°C, V<sub>CC</sub> = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Sym	Conditions	Min	Max	Units
Input Load Current	I <sub>IL</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., V <sub>IN</sub> = V <sub>CC</sub> or GND		10	μA
A9 Leakage Current	I <sub>LIT</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., A9 = +12V		50	μA
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Vcc Active Read Current	I <sub>CC1</sub>	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$		160	mA
Vcc Active Program/Erase Current <sup>(1)</sup>	I <sub>CC2</sub>	$\overline{CE} = V_{IL}$ , $\overline{OE} = V_{IH}$		240	mA
Vcc Standby Current	I <sub>CC3</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., $\overline{CE} = \overline{RESET} = V_{CC} \pm 0.3V$		4	mA
Vcc Standby Current (Reset)	I <sub>CC4</sub>	V <sub>CC</sub> = V <sub>CC</sub> Max., $\overline{RESET} = V_{CC} \pm 0.3V$		4	mA
Output Low Voltage	V <sub>OL</sub>	V <sub>CC</sub> = V <sub>CC</sub> Min., I <sub>OL</sub> = 12 mA		0.45	V
Output High Voltage	V <sub>OH1</sub>	V <sub>CC</sub> = V <sub>CC</sub> Min., I <sub>OH</sub> = -2.5 mA	0.85 x V <sub>CC</sub>		V
	V <sub>OH2</sub>	V <sub>CC</sub> = V <sub>CC</sub> Min., I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.4V		V
Low Vcc Lock-Out Voltage	V <sub>LKO</sub>		3.2	4.2	V

Notes:

1. Not 100% tested.

## AC Characteristics – Write/Erase/Program Operations – $\overline{WE}$ Controlled

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>wc</sub>	t <sub>AVAV</sub>	90		120		150		ns
Address Setup to $\overline{WE}$ Going Low	t <sub>AS</sub>	t <sub>AVWL</sub>	0		0		0		ns
Address Hold Time from $\overline{CE}$ High	t <sub>AH</sub>	t <sub>WLAX</sub>	45		50		50		ns
Data Setup to $\overline{WE}$ Going High	t <sub>DS</sub>	t <sub>DVWH</sub>	45		50		50		ns
Data Hold Time from $\overline{WE}$ High	t <sub>DH</sub>	t <sub>WHDX</sub>	0		0		0		ns
Output Enable Hold Time	Read		0		0		0		ns
	Toggle Bit I and Data Polling		10		10		10		ns
Read Recover Time Before Write ( $\overline{OE}$ High to $\overline{WE}$ Low)	t <sub>GHWL</sub>	t <sub>GHWL</sub>	0		0		0		ns
$\overline{CE}$ Setup Time from $\overline{WE}$ Low	t <sub>CS</sub>	t <sub>ELWL</sub>	0		0		0		ns
$\overline{CE}$ Hold Time from $\overline{WE}$ High	t <sub>CH</sub>	t <sub>WHEH</sub>	0		0		0		ns
$\overline{WE}$ Pulse Width	t <sub>WP</sub>	t <sub>WLWH</sub>	45		50		50		ns
$\overline{WE}$ Pulse Width High	t <sub>WPH</sub>	t <sub>WHWL</sub>	20		20		20		ns
Byte Programming Operation	t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	8		8		8		μs
Sector Erase Operation	t <sub>WHWH2</sub>	t <sub>WHWH2</sub>		15		15		15	Sec
Vcc Set-Up Time	t <sub>VCS</sub>		50		50		50		μs
Rise Time to V <sub>ID</sub>	t <sub>VDR</sub>		500		500		500		ns
$\overline{OE}$ Setup Time to $\overline{WE}$ Active	t <sub>OESP</sub>		4		4		4		μs
Reset Pulse Width	t <sub>RP</sub>		500		500		500		ns
Program/Erase Valid to RY/ $\overline{BY}$ Delay	t <sub>BUSY</sub>		40		50		60		ns

Notes:

1. Not 100% tested.

## AC Characteristics – Read Only Operations

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time <sup>(1)</sup>	t <sub>RC</sub>	t <sub>AVAV</sub>	90		120		150		ns
Address to Output Delay	t <sub>ACC</sub>	t <sub>AVQV</sub>		90		120		150	ns
$\overline{CE}$ to Output Delay	t <sub>CE</sub>	t <sub>ELQV</sub>		90		120		150	ns
$\overline{OE}$ to Output Delay	t <sub>OE</sub>	t <sub>GLQV</sub>		40		50		55	ns
$\overline{CE}$ to Output in High Z <sup>(1)</sup>	t <sub>DF</sub>	t <sub>EHQZ</sub>		20		30		35	ns
$\overline{OE}$ to Output in High Z <sup>(1)</sup>	t <sub>DF</sub>	t <sub>GHQZ</sub>		20	0	30	0	35	ns
Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	t <sub>OH</sub>	t <sub>AXQX</sub>	0		0		0		ns
RESET Low to Read Mode <sup>(1)</sup>	t <sub>READY</sub>			20		20		20	μs

Notes:

1. Not 100% tested.

## AC Characteristics – Write/Erase/Program Operations – $\overline{CE}$ Controlled

(Tc = -55°C to +125°C, Vcc = +4.5V to +5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Write Cycle Time <sup>(1)</sup>	tWC	tAVAV	90		120		150		ns
Address Setup to $\overline{CE}$ Going Low	tAS	tAVEL	0		0		0		ns
Address Hold Time from $\overline{CE}$ Low	tAH	tELAX	45		50		50		ns
Data Setup to $\overline{CE}$ Going High	tDS	tDVEH	45		50		50		ns
Data Hold Time from $\overline{CE}$ High	tDH	tEHDX	0		0		0		ns
Output Enable Setup Time <sup>(1)</sup>	toES		0		0		0		ns
Output Enable Hold Time <sup>(1)</sup>	Read	toEH	0		0		0		ns
	Toggle Bit I and Data Polling		10		10		10		ns
Read Recover Time Before Write ( $\overline{OE}$ High to $\overline{WE}$ Low)	tGHEL	tGHEL	0		0		0		ns
$\overline{CE}$ Setup Time from $\overline{WE}$ Low	tWS	tWLEL	0		0		0		ns
$\overline{WE}$ Hold Time from $\overline{CE}$ High	tWH	tEHHW	0		0		0		ns
$\overline{WE}$ Pulse Width	tCP	tELEH	45		50		50		ns
$\overline{WE}$ Pulse Width High	tCPH	tELEL	20		20		20		ns
Byte Programming Operation	tWHWH1	tWHWH1	8		8		8		µs
Sector Erase Operation	tWHWH2	tWHWH2		15		15		15	Sec

Notes:

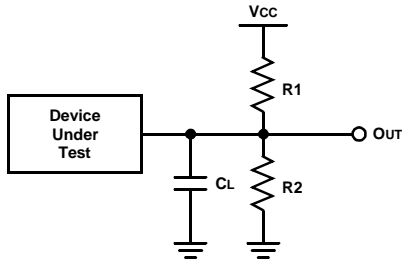
1. Not 100% tested.

## AC Test Circuit

Test Configuration Component Values

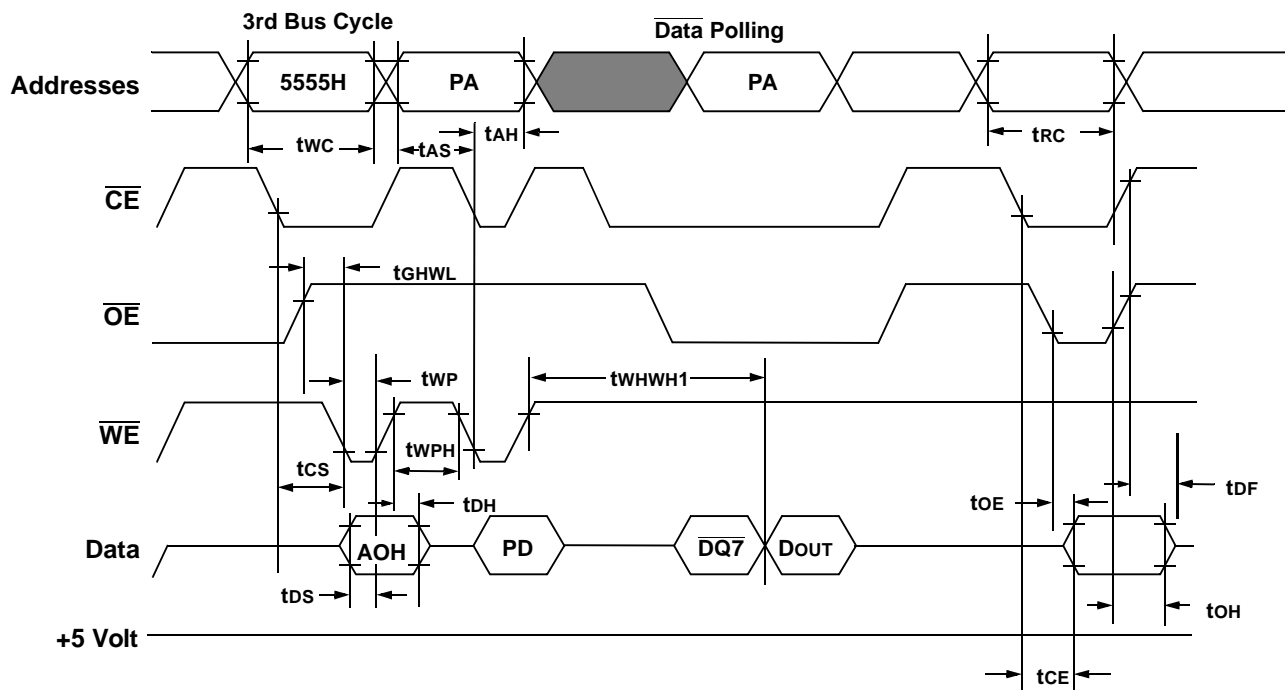
Test Configuration	CL (pF)	R1 ( $\Omega$ )	R2 ( $\Omega$ )
3.3V Standard Test	50	990	770
5V Standard Test	50	580	390

NOTES:  
CL includes jig capacitance.

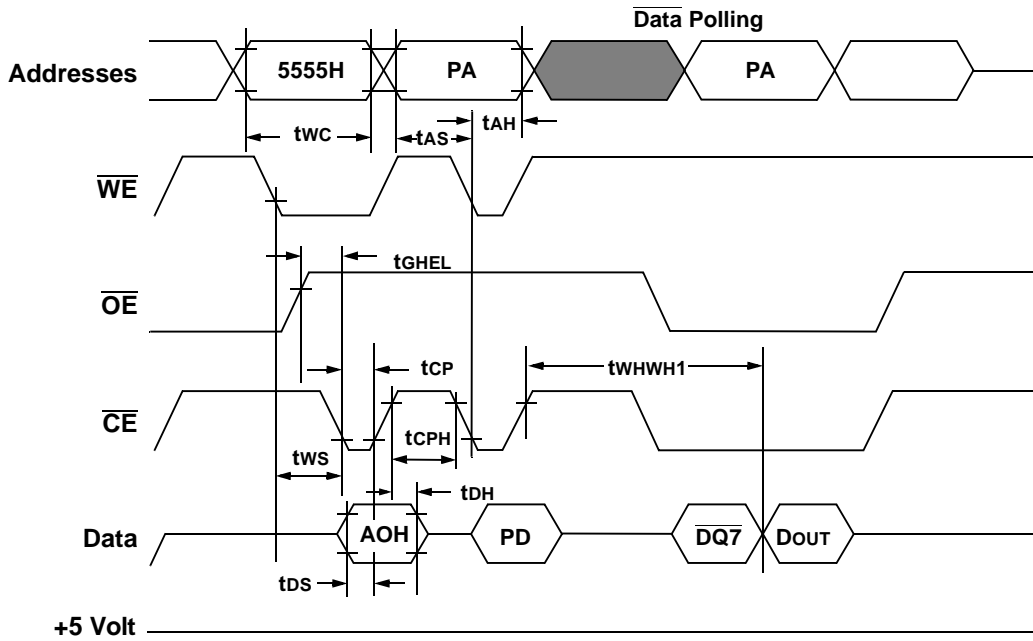


Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

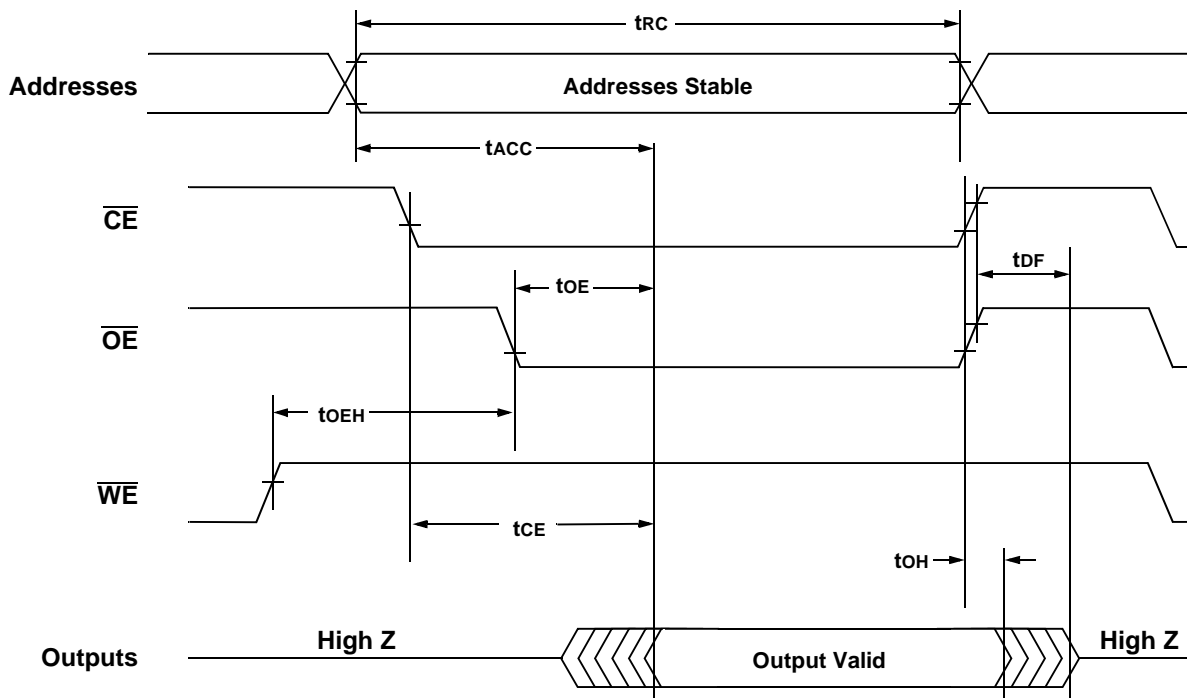
## AC Waveforms for Write and Erase Operations, $\overline{WE}$ Controlled



## AC Waveforms for Write and Erase Operations, $\overline{CE}$ Controlled



## AC Waveform For Read Operations

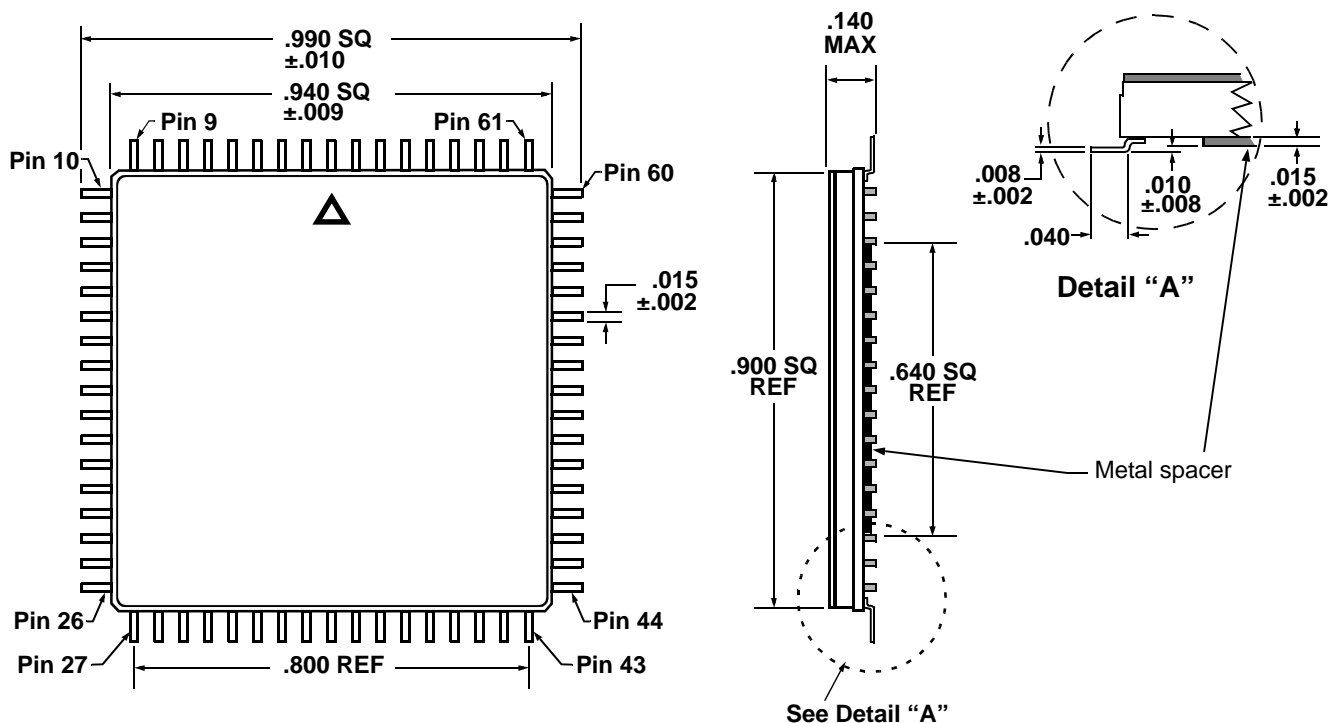


## Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP (Standard Configuration)							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O <sub>8</sub>	36	$\overline{CE}_2$	53	I/O <sub>23</sub>
3	A <sub>5</sub>	20	I/O <sub>9</sub>	37	A <sub>17</sub>	54	I/O <sub>22</sub>
4	A <sub>4</sub>	21	I/O <sub>10</sub>	38	RY/ $\overline{BY}$	55	I/O <sub>21</sub>
5	A <sub>3</sub>	22	I/O <sub>11</sub>	39	NC	56	I/O <sub>20</sub>
6	A <sub>2</sub>	23	I/O <sub>12</sub>	40	NC	57	I/O <sub>19</sub>
7	A <sub>1</sub>	24	I/O <sub>13</sub>	41	A <sub>18</sub>	58	I/O <sub>18</sub>
8	A <sub>0</sub>	25	I/O <sub>14</sub>	42	A <sub>19</sub>	59	I/O <sub>17</sub>
9	$\overline{RESET}$	26	I/O <sub>15</sub>	43	A <sub>20</sub>	60	I/O <sub>16</sub>
10	I/O <sub>0</sub>	27	V <sub>CC</sub>	44	I/O <sub>31</sub>	61	V <sub>CC</sub>
11	I/O <sub>1</sub>	28	A <sub>11</sub>	45	I/O <sub>30</sub>	62	A <sub>10</sub>
12	I/O <sub>2</sub>	29	A <sub>12</sub>	46	I/O <sub>29</sub>	63	A <sub>9</sub>
13	I/O <sub>3</sub>	30	A <sub>13</sub>	47	I/O <sub>28</sub>	64	A <sub>8</sub>
14	I/O <sub>4</sub>	31	A <sub>14</sub>	48	I/O <sub>27</sub>	65	A <sub>7</sub>
15	I/O <sub>5</sub>	32	A <sub>15</sub>	49	I/O <sub>26</sub>	66	A <sub>6</sub>
16	I/O <sub>6</sub>	33	A <sub>16</sub>	50	I/O <sub>25</sub>	67	$\overline{WE}$
17	I/O <sub>7</sub>	34	$\overline{CE}_1$	51	I/O <sub>24</sub>	68	$\overline{CE}_4$

Consult Factory for Special order (Optional Configuration): Pin 38 -  $\overline{WE}_2$ , Pin 39 -  $\overline{WE}_3$ , Pin 40 -  $\overline{WE}_4$  and Pin 67 -  $\overline{WE}_1$

### "F18" — CQFP Package



All dimensions in inches

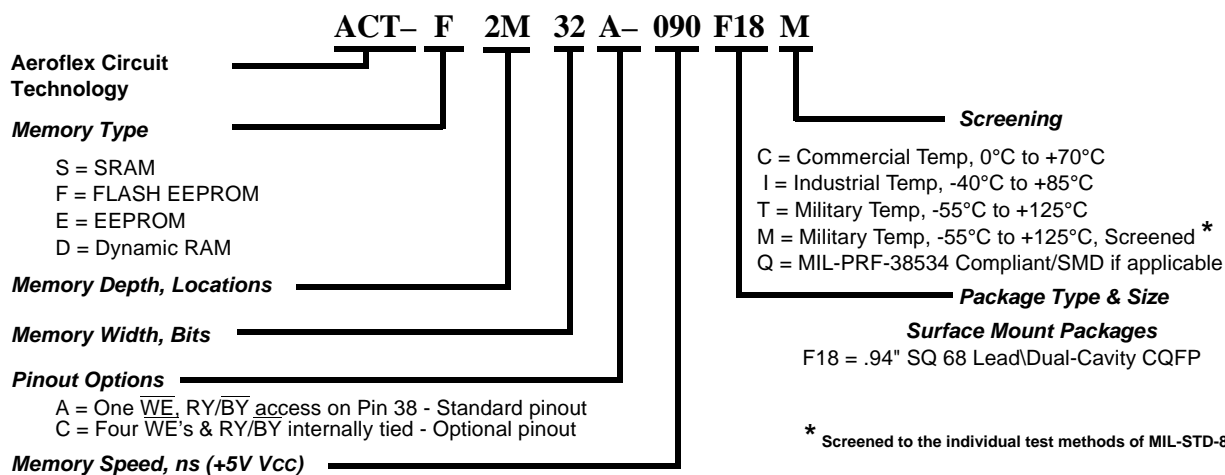




## Ordering Information

Model Number	Screening	Speed	Package
ACT-F2M32A-090F18C	Commercial (0°C to +70°C)	90 ns	CQFP
ACT-F2M32A-120F18C	Commercial (0°C to +70°C)	120 ns	CQFP
ACT-F2M32A-150F18C	Commercial (0°C to +70°C)	150 ns	CQFP
ACT-F2M32A-090F18I	Industrial (-40°C to +85°C)	90 ns	CQFP
ACT-F2M32A-120F18I	Industrial (-40°C to +85°C)	120 ns	CQFP
ACT-F2M32A-150F18I	Industrial (-40°C to +85°C)	150 ns	CQFP
ACT-F2M32A-090F18M	Military (-55°C to +125°C)	90 ns	CQFP
ACT-F2M32A-120F18M	Military (-55°C to +125°C)	120 ns	CQFP
ACT-F2M32A-150F18M	Military (-55°C to +125°C)	150 ns	CQFP
ACT-F2M32A-090F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	90 ns	CQFP
ACT-F2M32A-120F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	120 ns	CQFP
ACT-F2M32A-150F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	150 ns	CQFP

## Part Number Breakdown



Specifications subject to change without notice

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