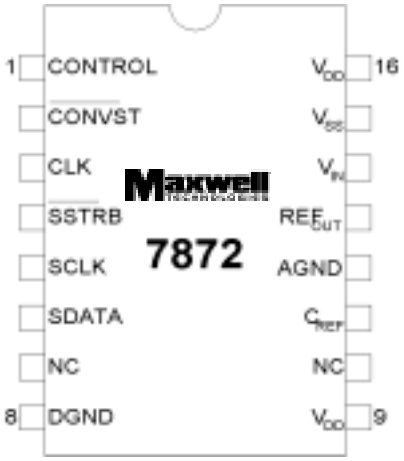
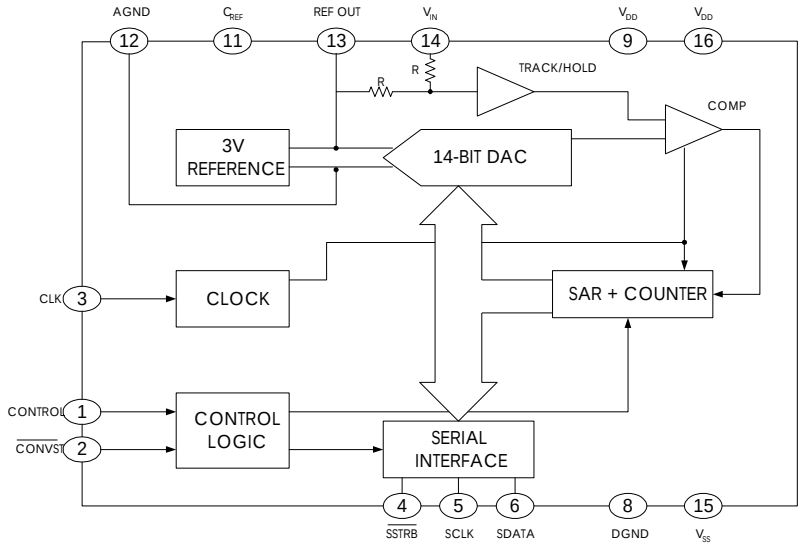
# 7872
## 14-Bit A/D Converter




**Logic Diagram**

## FEATURES:

- 14-bit resolution and accuracy
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Single event effects:
  - SEL > 104 MeV/mg/cm$^2$
  - $SEU_{TH}$ = 1.4 MeV/mg/cm$^2$
  - $SEU_{Sat}$ = 1E-3 cm$^2$/Device
- Package:
  - 16 pin RAD-PAK® flat package
  - 16 pin RAD-PAK® dual-in-line package
- Fast Conversion Times: 10 µs
- Low 50 mW typical power consumption
- High speed LC$^2$MOS technology
  - Analog input range of ±3V
  - 83 KSPS throughput rate
  - Operates with +5V/-5V power supplies
  - 80 dB SNR at 10 kHz input frequency
  - 2 s complement coding
  - Serial output

## DESCRIPTION:

Maxwell Technologies' 7872 high-speed 14-bit ADC microcircuit features a greater than 100 krad (Si) total dose tolerance; depending upon orbit. The 7872 consists of a track/hold amplifier, successive-approximation ADC, 3V buried Zener reference and versatile interface logic. It features a self-contained, laser- trimmed internal clock, so no external clock timing components are required. For minimum noise possible, the on-chip clock may be overridden to synchronize the device operation to the digital system. The 7872 is a serial output device. It is capable of interfacing to all modern microprocessors and digital signal processors. The 7872 operates from ±5V power supplies, accepts bipolar input signals of ±3V and is able to convert full power signals up to 41.5 kHz. It is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.



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TABLE 1. 7872 PIN DESCRIPTION

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | CONTROL | Control Function |
| 2 | $\overline{\text{CONVST}}$ | Convert Start |
| 3 | CLK | Clock Input |
| 4 | $\overline{\text{SSTRB}}$ | Serial Strobe |
| 5 | SCLK | Serial Clock |
| 6 | SDATA | Serial Data |
| 7 | NC | Non Connect |
| 8 | DGND | Digital Ground |
| 9 | $V_{DD}$ | Positive Supply |
| 10 | NC | No Connect |
| 11 | $C_{REF}$ | Reference Capacitor |
| 12 | AGND | Analog Ground |
| 13 | $REF_{OUT}$ | Voltage Reference Output |
| 14 | $V_{IN}$ | Analog Input |
| 15 | $V_{SS}$ | Negative Supply |
| 16 | $V_{DD}$ | Positive Supply |

TABLE 2. 7872 ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Positive Supply Voltage; Relative to GND | $V_{DD}$ | -0.3 | 7.0 | V |
| Negative Supply Voltage; Relative to GND | $V_{SS}$ | 0.3 | 7.0 | V |
| AGND to DGND; Relative to GND | -- | -0.3 | $V_{DD}$ +0.3 | V |
| $REF_{OUT}$, $C_{REF}$ to AGND | -- | 0 | $V_{DD}$ | V |
| $V_{IN}$ to AGND | -- | $V_{SS}$ -0.3 | $V_{DD}$ +0.3 | V |
| Digital Input Voltage | $V_{IN}$ | -0.3 | $V_{DD}$ +0.3 | V |
| Digital Output Voltage | $V_{OUT}$ | -0.3 | $V_{DD}$ +0.3 | V |
| Thermal Impedance | $\Theta_{JC}$ | -- | 2.44 | °C/W |
| Storage Temperature Range | $T_S$ | -65 | 150 | °C |
| Operating Temperature Range | $T_A$ | -55 | 125 | °C |

## TABLE 3. 7872 DC ELECTRICAL CHARACTERISTICS FOR DYNAMIC PERFORMANCE [1]

($V_{DD}$ = 5 V ± 5%, $V_{SS}$ = -5 V ± 5%, AGND = DGND = 0 V,
$f_{CLK}$ = 2 MHz EXTERNAL, $f_{SAMPLE}$ = 83 kHz, -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUBGROUPS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Signal to Noise Ratio $V_{IN}$ = 10kHz Sine Wave, $T_{MIN}$ to $T_{MAX}$;<br>SNR is typically 82dB for $V_{IN}$ < 41.5kHz [2] | SNR | 4, 5, 6 | 79 | -- | -- | dB |
| Total Harmonic Distortion $V_{IN}$ = 10kHz Sine Wave | THD | 4, 5, 6 | -- | -86 | -- | dB |
| Peak Harmonic or Spurious Noise | -- | 4, 5, 6 | -- | -86 | -- | dB |
| Intermodulation Distortion<br>Second Order Terms: $f_a$ = 9 kHz, $f_b$ = 9.5 kHz, $f_{SAMPLE}$ = 50 kHz<br>Third Order Terms: $f_a$ = 9 kHz, $f_b$ = 9.5 kHz, $f_{SAMPLE}$= 50 kHz | IMD | 4, 5, 6 | <br>--<br>-- | <br>-86<br>-86 | <br>--<br>-- | dB |
| Track/Hold Acquisition Time | -- | 4, 5, 6 | -- | -- | 2 | µs |

1. $V_{IN}$ = ± 3 V. Guaranteed by design.
2. SNR calculation includes distortion and noise components.

## TABLE 4. 7872 DC ELECTRICAL CHARACTERISTICS FOR ACCURACY

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUGROUPS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Resolution | -- | 1, 2, 3 | 14 | -- | -- | Bits |
| Resolution for Which No Missing Codes are Guaranteed | -- | 1, 2, 3 | 14 | -- | -- | Bits |
| Integral Nonlinearity @ 25 °C | -- | 1, 2, 3 | -- | ±1 | -- | LSB |
| Integral Nonlinearity $T_{MIN}$ to $T_{MAX}$ | -- | 1, 2, 3 | -- | -- | ±2 | LSB |
| Bipolar Zero Error | -- | 1, 2, 3 | -- | -- | ±12 | LSB |
| Positive Gain Error [1] | -- | 1, 2, 3 | -- | -- | ±12 | LSB |
| Negative Gain Error [1] | -- | 1, 2, 3 | -- | -- | ±12 | LSB |

1. Measured with respect to internal reference.

## TABLE 5. 7872 DC ELECTRICAL CHARACTERISTICS FOR ANALOG INPUT

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUBGROUPS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input Voltage Range | -- | 1, 2, 3 | -3 | 3 | V |
| Input Current | -- | 1, 2, 3 | -500 | 500 | µA |

## TABLE 6. 7872 DC ELECTRICAL CHARACTERISTICS FOR REFERENCE OUTPUT

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUGGROUPS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $REF_{OUT}$ @ +25 ˚C | -- | 1, 2, 3 | 2.99 | 3.01 | V |
| $REF_{OUT}$ $T_{MIN}$ to $T_{MAX}$ | -- | 1, 2, 3 | 2.98 | 3.02 | V |
| $REF_{OUT}$ Tempco: Typically 35ppm | -- | 1, 2, 3 | -- | ±40 | ppm/ºC |
| Reference Load Sensitivity ($DREF_{OUT}$/DI) Reference Load Current Change (0-300 µA); Reference Load Should Not Be Changed During Conversion | -- | 1, 2, 3 | -- | 1.2 | mV |

## TABLE 7. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC INPUTS

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUGGROUPS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Input High Voltage: $V_{DD}$ 5 V ± 5% | $V_{INH}$ | 1, 2, 3 | 2.4 | -- | V |
| Input Low Voltage: $V_{DD}$ 5 V ± 5% | $V_{INL}$ | 1, 2, 3 | -- | 0.8 | V |
| Input Current: $V_{IN}$ = 0 V to $V_{DD}$ | $I_{IN}$ | 1, 2, 3 | -10 | 10 | µA |
| Input Current: (14/8/CLK input only) VIN = VSS to VDD | -- | 1, 2, 3 | -10 | 10 | µA |
| Input Capacitance [1] | $C_{IN}$ | 1, 2, 3 | -- | 10 | pF |

1. Not tested.

## TABLE 8. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC OUTPUTS

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUBGROUPS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Output High Voltage $I_{SOURCE}$ = 40 µA | $V_{OH}$ | 1, 2, 3 | 4.0 | -- | V |
| Output Low Voltage $I_{SINK}$ = 1.6 mA | $V_{OL}$ | 1, 2, 3 | -- | 0.4 | V |
| Floating-State Leakage Current | -- | 1, 2, 3 | -- | 10 | µA |
| Floating-State Output Capacitance [1] | -- | 1, 2, 3 | -- | 15 | pF |

1. Not tested.

## TABLE 9. 7872 DC ELECTRICAL CHARACTERISTICS FOR CONVERSION TIME

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | SUBGROUPS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| External Clock | -- | 1, 2, 3 | -- | 10 | µs |
| Internal Clock: Nominal Value = 2 MHz | -- | 1, 2, 3 | -- | 11 | µs |

## TABLE 10. 7872 DC ELECTRICAL CHARACTERISTICS FOR POWER REQUIREMENTS

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER | SYMBOL | CONDITIONS | REQUIREMENTS | UNITS |
|---|---|---|---|---|
| Positive Supply Voltage | $V_{DD}$ | 5% for Specified Performance | 5 | V |
| Negative Supply Voltage | $V_{SS}$ | 5% for Specified Performance | -5 | V |
| Positive Supply Current | $I_{DD}$ | Typically 6mA | 13 | mA max |
| Negative Supply Current | $I_{SS}$ | Typically 4mA | 6 | mA max |
| Power Dissipation | $P_D$ | Typically 50mW | 95 | mW max |

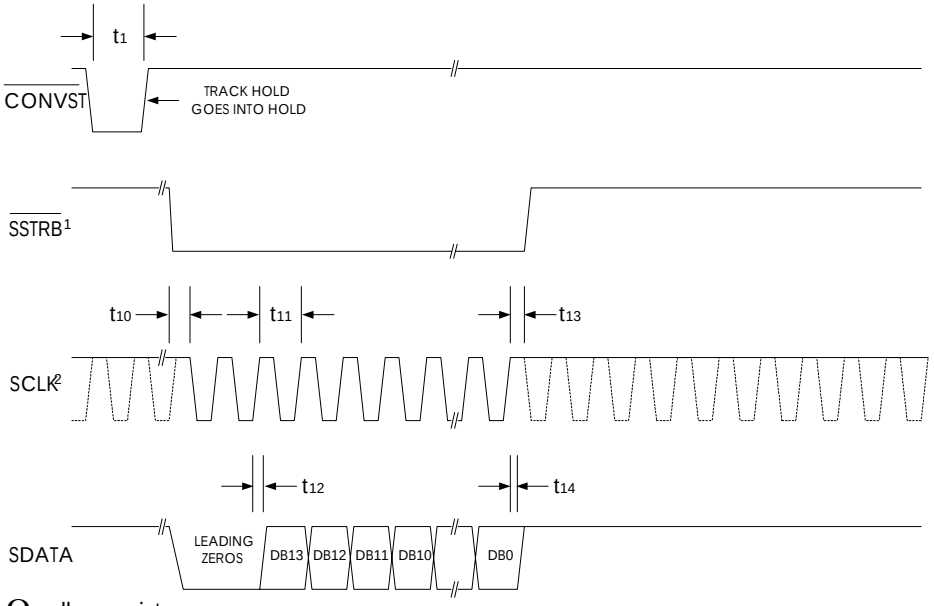
## TABLE 11. 7872 TIMING CHARACTERISTICS [1,2]

($V_{DD}$ = 5V ±5%, $V_{SS}$ = -5 V ± 5%, $T_A$ = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

| PARAMETER/CONDITION | SYMBOL | SUBGROUPS | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $\overline{\text{CONVST}}$ Pulse Width | $t_1$ | 9, 10, 11 | 50 | -- | ns |
| $\overline{\text{SSTRB}}$ to SCLK Falling Edge Setup Time | $t_{10}$ | 9, 10, 11 | 100 | -- | ns |
| SCLK Cycle Time [3] | $t_{11}$ | 9, 10, 11 | 440 | -- | ns |
| SCLK to Valid Data Delay: $C_L$ = 35 pF [4] | $t_{12}$ | 9, 10, 11 | -- | 155 | ns |
| SCLD Rising Edge to $\overline{\text{SSTRB}}$ | $t_{13}$ | 9, 10, 11 | 20 | 150 | ns |
| Bus Relinquish Time After SCLK | $t_{14}$ | 9, 10, 11 | 4 | 100 | ns |

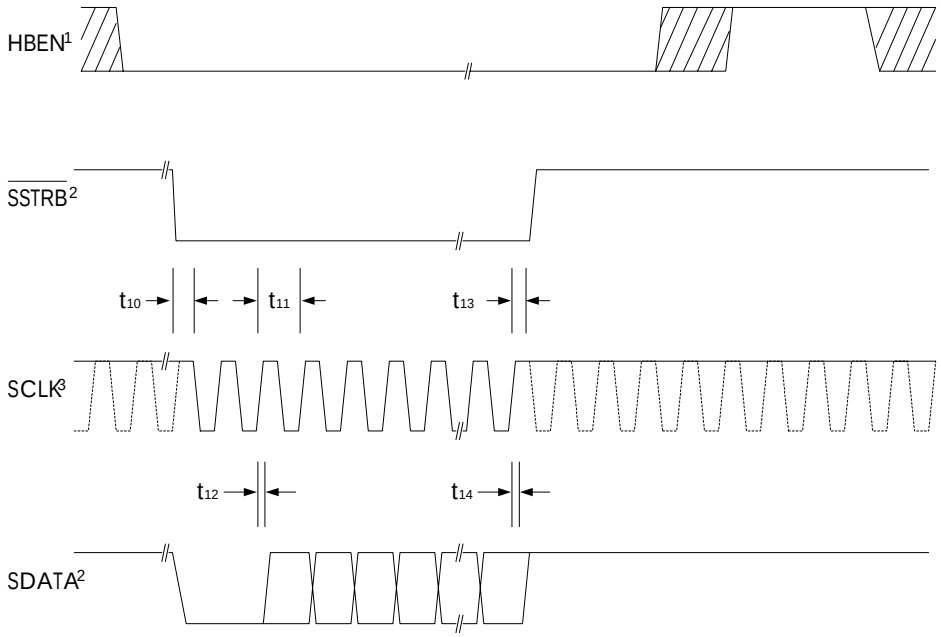
1. All input signals are specified with tr = tr = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
2. Serial timing is measured with a 4.7 kΩ pull-up resistor on SDATA and $\overline{\text{SSTRB}}$ and a 2 kΩ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
3. SCLK mark/space ration (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
4. SDATA will drive higher capacitive loads, but this will add to $t_{12}$ since it increases the external RC time constant (4.7kΩ/$C_L$) and hence, the time to reach 2.4 V.

FIGURE 1. MODE 1 TIMING DIAGRAM SERIAL




1. External 4.7 kΩ pull-up resistor.
2. External 2 kΩ pull-up resistor continuos SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V.

FIGURE 2. MODE 2 TIMING DIAGRAM, SERIAL READ




1. Times t15, t18, t19 and t20 are the same for a high byte read as for a low byte read.
2. External 4.7 kΩ pull-up resistor.
3. Continuos SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V. External 2 kΩ pull-up resistor.

FIGURE 3. LOAD CIRCUIT FOR ACCESS TIME

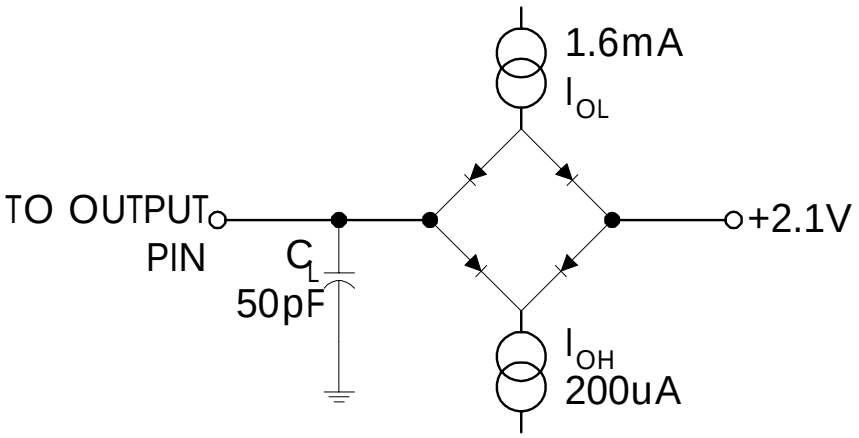
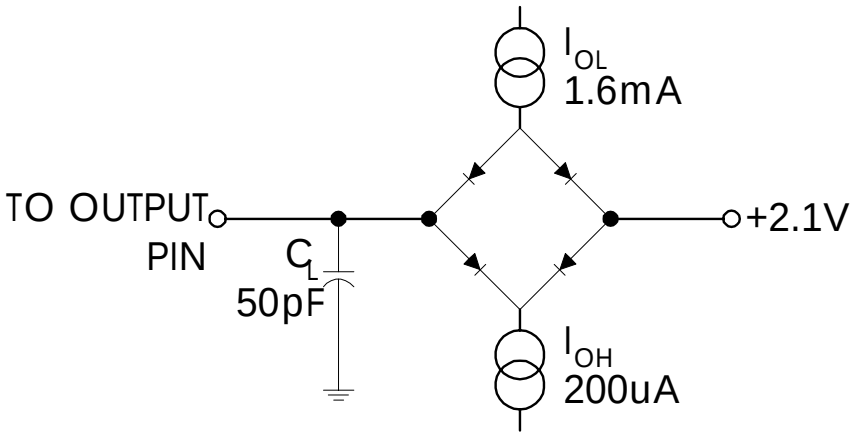
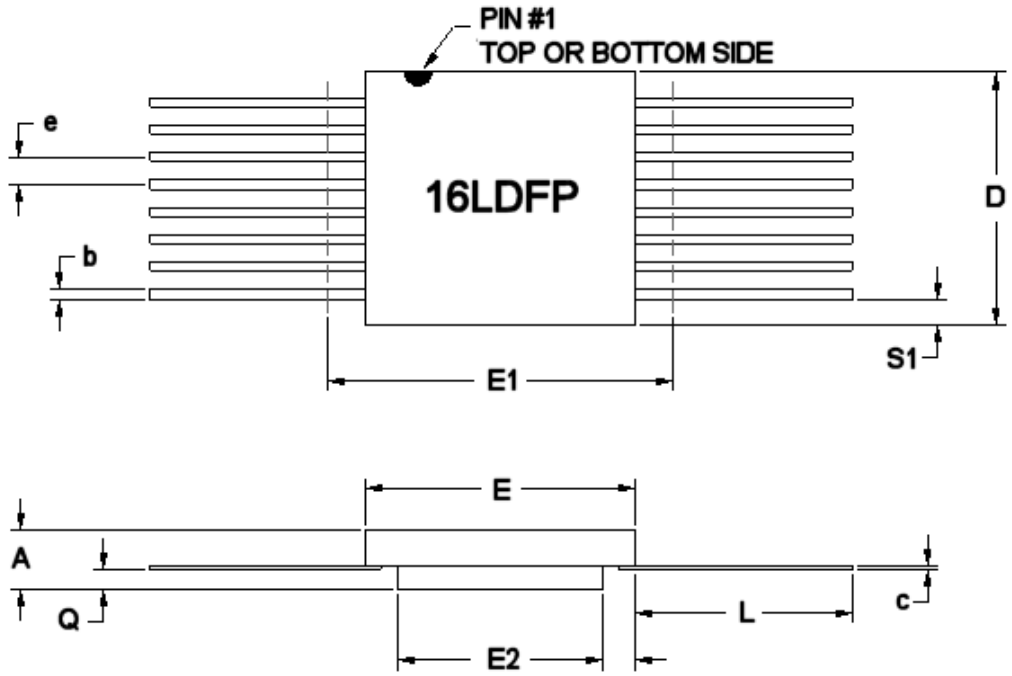



FIGURE 4. LOAD CIRCUIT FOR OUTPUT FLOAT DELAY

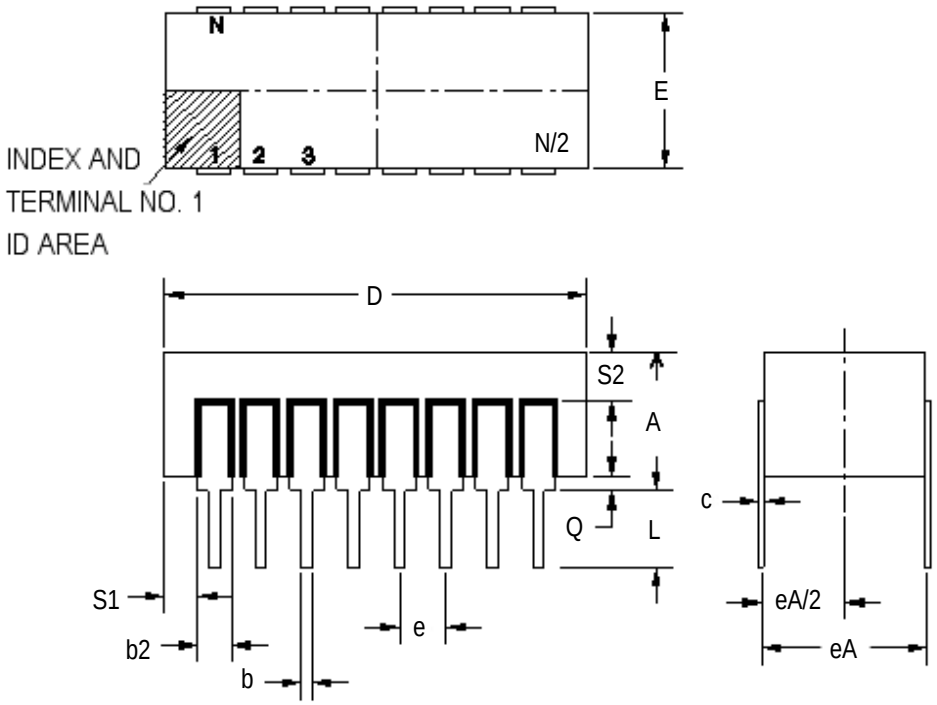





16 PIN RAD-PAK® FLAT PACKAGE

| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.116 | 0.130 | 0.143 |
| b | 0.015 | 0.017 | 0.022 |
| c | 0.004 | 0.005 | 0.009 |
| D | -- | 0.415 | 0.440 |
| E | 0.245 | 0.280 | 0.285 |
| E1 | -- | -- | 0.315 |
| E2 | 0.130 | 0.156 | -- |
| E3 | 0.030 | 0.062 | -- |
| e | 0.050 BSC | | |
| L | 0.325 | 0.335 | 0.345 |
| Q | 0.020 | 0.033 | 0.045 |
| S1 | 0.005 | 0.024 | -- |
| N | 16 | | |

F16-01
Note: All dimensions in inches




16 PIN RAD-PAK® DUAL IN LINE PACKAGE

| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 0.157 | 0.200 |
| b | 0.014 | 0.018 | 0.026 |
| b2 | 0.045 | 0.047 | 0.065 |
| c | 0.008 | 0.010 | 0.018 |
| D | -- | 0.800 | 0.840 |
| E | 0.220 | 0.295 | 0.310 |
| eA | 0.300 BSC | | |
| eA/2 | 0.150 BSC | | |
| e | 0.100 BSC | | |
| L | 0.135 | 0.145 | 0.155 |
| Q | 0.000 | 0.002 | 0.060 |
| S1 | 0.005 | 0.027 | -- |
| S2 | 0.005 | -- | -- |
| N | 16 | | |

D16-01
Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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