

## 74LVTH162374

### Low Voltage 16-Bit D-Type Flip-Flop with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

#### General Description

The LVTH162374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ( $\overline{OE}$ ) are common to each byte and can be shorted together for full 16-bit operation.

The LVTH162374 is designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH162374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

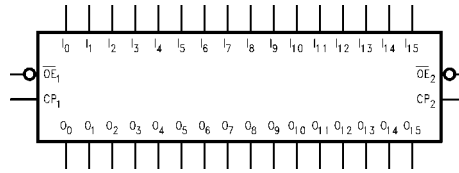
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Power Down high impedance provides glitch-free bus loading
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Functionally compatible with the 74 series 16374
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

#### Ordering Code:

Order Number	Package Number	Package Description
74LVTH162374GX (Note 1)	BGA54A (Preliminary)	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [TAPE and REEL]
74LVTH162374MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TUBES]
74LVTH162374MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVTH162374MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBES]
74LVTH162374MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

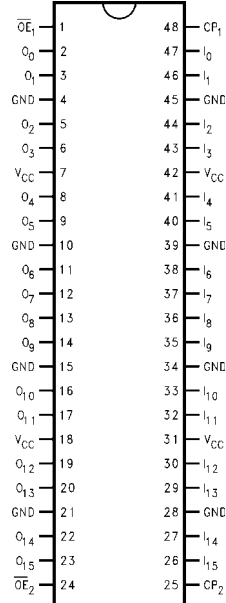
**Note 1:** BGA package available in Tape and Reel only.

### Logic Symbol

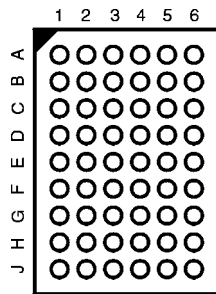


### Connection Diagrams

Pin Assignments for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP <sub>n</sub>	Clock Pulse Input
I <sub>0</sub> -I <sub>15</sub>	Inputs
O <sub>0</sub> -O <sub>15</sub>	3-STATE Outputs
NC	No Connect

### FBGA Pin Assignments

	1	2	3	4	5	6
<b>A</b>	O <sub>0</sub>	NC	$\overline{OE}_1$	CP <sub>1</sub>	NC	I <sub>0</sub>
<b>B</b>	O <sub>2</sub>	O <sub>1</sub>	NC	NC	I <sub>1</sub>	I <sub>2</sub>
<b>C</b>	O <sub>4</sub>	O <sub>3</sub>	V <sub>CC</sub>	V <sub>CC</sub>	I <sub>3</sub>	I <sub>4</sub>
<b>D</b>	O <sub>6</sub>	O <sub>5</sub>	GND	GND	I <sub>5</sub>	I <sub>6</sub>
<b>E</b>	O <sub>8</sub>	O <sub>7</sub>	GND	GND	I <sub>7</sub>	I <sub>8</sub>
<b>F</b>	O <sub>10</sub>	O <sub>9</sub>	GND	GND	I <sub>9</sub>	I <sub>10</sub>
<b>G</b>	O <sub>12</sub>	O <sub>11</sub>	V <sub>CC</sub>	V <sub>CC</sub>	I <sub>11</sub>	I <sub>12</sub>
<b>H</b>	O <sub>14</sub>	O <sub>13</sub>	NC	NC	I <sub>13</sub>	I <sub>14</sub>
<b>J</b>	O <sub>15</sub>	NC	$\overline{OE}_2$	CP <sub>2</sub>	NC	I <sub>15</sub>

### Truth Tables

Inputs			Outputs
CP <sub>1</sub>	$\overline{OE}_1$	I <sub>0</sub> -I <sub>7</sub>	O <sub>0</sub> -O <sub>7</sub>
↗	L	H	H
↗	L	L	L
L	L	X	O <sub>0</sub>
X	H	X	Z

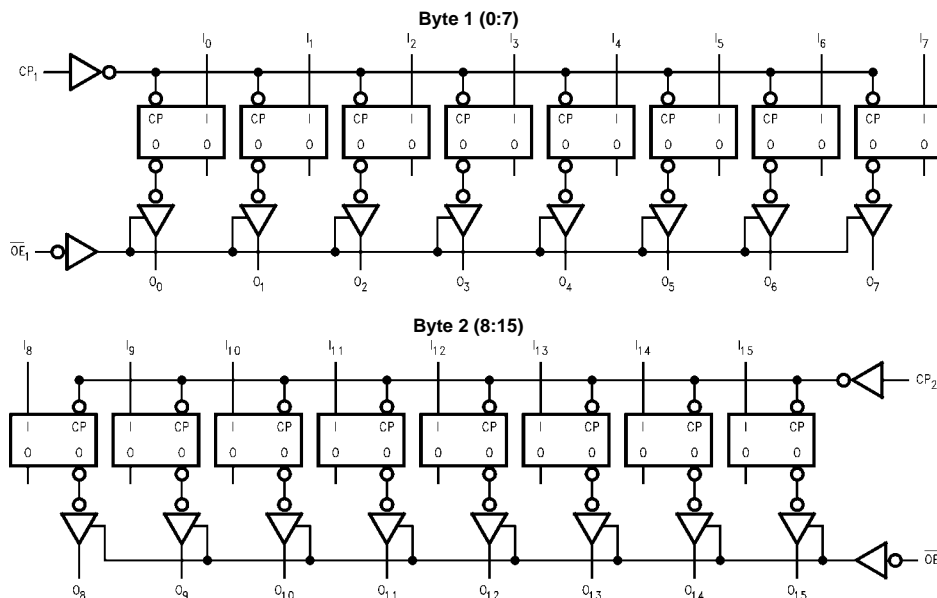
Inputs			Outputs
CP <sub>2</sub>	$\overline{OE}_2$	I <sub>8</sub> -I <sub>15</sub>	O <sub>8</sub> -O <sub>15</sub>
↗	L	H	H
↗	L	L	L
L	L	X	O <sub>0</sub>
X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = HIGH Impedance  
 O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW of CP

## Functional Description

The LVTH162374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock ( $CP_n$ ) transition. With the Output Enable ( $\overline{OE}_n$ ) LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}_n$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}_n$  input does not affect the state of the flip-flops.

## Logic Diagrams



Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)					
Symbol	Parameter	Value	Conditions		Units
V <sub>CC</sub>	Supply Voltage	-0.5 to +4.6			V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0			V
V <sub>O</sub>	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE		V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 3)		
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND		mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND		mA
I <sub>O</sub>	DC Output Current	64	V <sub>O</sub> > V <sub>CC</sub> Output at HIGH State		mA
		128	V <sub>O</sub> > V <sub>CC</sub> Output at LOW State		
I <sub>CC</sub>	DC Supply Current per Supply Pin	±64			mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±128			mA
T <sub>STG</sub>	Storage Temperature	-65 to +150			°C

Recommended Operating Conditions					
Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Supply Voltage	2.7	3.6	V	
V <sub>I</sub>	Input Voltage	0	5.5	V	
I <sub>OH</sub>	HIGH Level Output Current		-12	mA	
I <sub>OL</sub>	LOW Level Output Current		12	mA	
T <sub>A</sub>	Free-Air Operating Temperature	-40	85	°C	
Δt/ΔV	Input Edge Rate, V <sub>IN</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V	0	10	ns/V	

**Note 2:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 3:** I<sub>O</sub> Absolute Maximum Rating must be observed.

### DC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions	
			Min	Max			
V <sub>IK</sub>	Input Clamp Diode Voltage	2.7		-1.2	V	I <sub>I</sub> = -18 mA	
V <sub>IH</sub>	Input HIGH Voltage	2.7–3.6	2.0		V	V <sub>O</sub> ≤ 0.1V or	
V <sub>IL</sub>	Input LOW Voltage	2.7–3.6		0.8	V	V <sub>O</sub> ≥ V <sub>CC</sub> - 0.1V	
V <sub>OH</sub>	Output HIGH Voltage	2.7–3.6	V <sub>CC</sub> - 0.2		V	I <sub>OH</sub> = -100 μA	
		3.0	2.0			I <sub>OH</sub> = -12 mA	
V <sub>OL</sub>	Output LOW Voltage	2.7		0.2	V	I <sub>OL</sub> = 100 μA	
		3.0		0.8		I <sub>OL</sub> = 12 mA	
I <sub>I(HOLD)</sub>	Bushold Input Minimum Drive	3.0	75		μA	V <sub>I</sub> = 0.8V	
			-75			V <sub>I</sub> = 2.0V	
I <sub>I(OD)</sub>	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 4)	
			-500			(Note 5)	
I <sub>I</sub>	Input Current	3.6		10	μA	V <sub>I</sub> = 5.5V	
		Control Pins	3.6			±1	V <sub>I</sub> = 0V or V <sub>CC</sub>
		Data Pins	3.6			-5	V <sub>I</sub> = 0V
				1		V <sub>I</sub> = V <sub>CC</sub>	
I <sub>OFF</sub>	Power Off Leakage Current	0		±100	μA	0V ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V	
I <sub>PU/PD</sub>	Power Up/Down 3-STATE				μA	V <sub>O</sub> = 0.5V to 3.0V	
	Output Current	0–1.5V		±100	μA	V <sub>I</sub> = GND or V <sub>CC</sub>	
I <sub>OZL</sub>	3-STATE Output Leakage Current	3.6		-5	μA	V <sub>O</sub> = 0.5V	
I <sub>OZH</sub>	3-STATE Output Leakage Current	3.6		5	μA	V <sub>O</sub> = 3.0V	
I <sub>OZH+</sub>	3-STATE Output Leakage Current	3.6		10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V	
I <sub>CCH</sub>	Power Supply Current	3.6		0.19	mA	Outputs HIGH	
I <sub>CCL</sub>	Power Supply Current	3.6		5	mA	Outputs LOW	
I <sub>CCZ</sub>	Power Supply Current	3.6		0.19	mA	Outputs Disabled	

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Max		
I <sub>CCZ</sub> <sup>+</sup>	Power Supply Current	3.6		0.19	mA	V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 4:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 5:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 6:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

**Dynamic Switching Characteristics** (Note 7)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 8)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 8)

**Note 7:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 8:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

**AC Electrical Characteristics**

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω				Units
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		
		Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	160		150		MHz
t <sub>PHL</sub>	Propagation Delay	2.0	5.1	2.0	5.3	ns
t <sub>PLH</sub>	CP to O <sub>n</sub>	1.6	5.3	1.6	6.2	
t <sub>PZL</sub>	Output Enable Time	1.8	5.0	1.8	6.0	ns
t <sub>PZH</sub>		1.2	5.6	1.2	6.9	
t <sub>PLZ</sub>	Output Disable Time	1.9	5.0	1.9	5.1	ns
t <sub>PHZ</sub>		2.0	5.4	2.0	5.7	
t <sub>S</sub>	Setup Time	1.8		2.0		ns
t <sub>H</sub>	Hold Time	0.8		0.1		ns
t <sub>W</sub>	Pulse Width	3.0		3.0		ns
t <sub>OSHL</sub>	Output to Output Skew (Note 9)		1.0		1.0	ns
t <sub>OSLH</sub>			1.0		1.0	

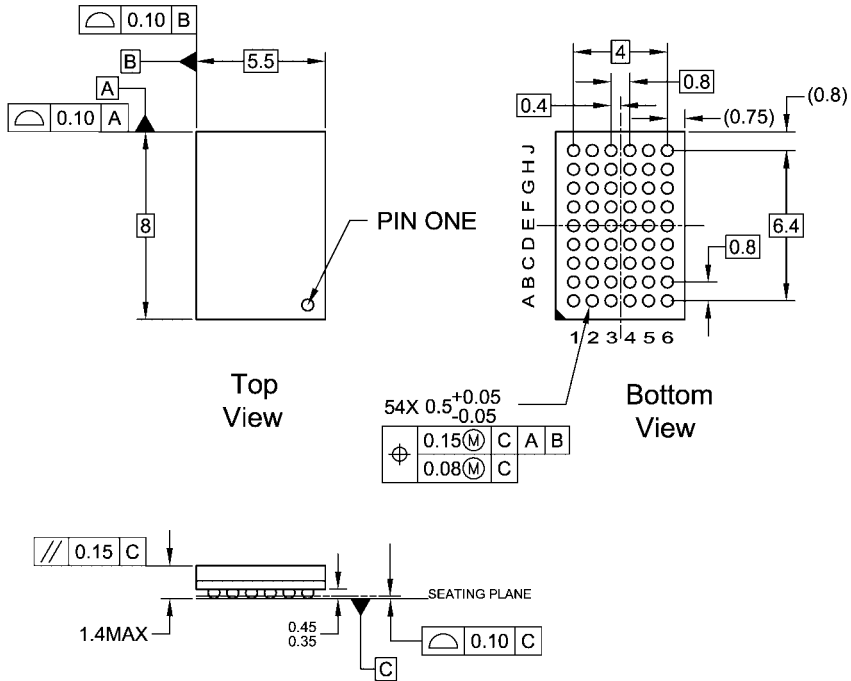
**Note 9:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

**Capacitance** (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = OPEN, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

**Note 10:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



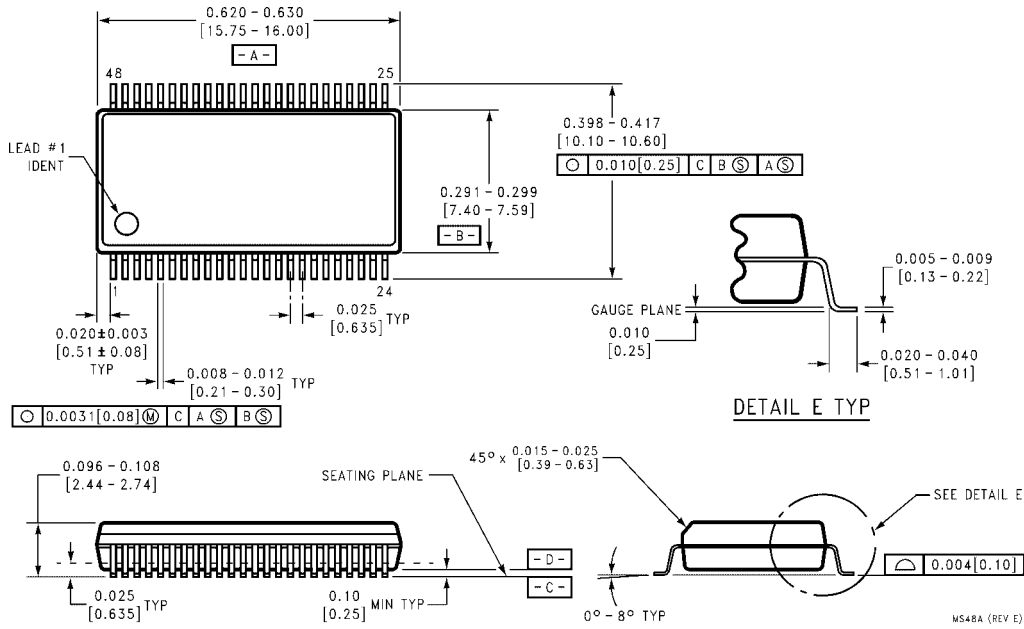
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)  
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

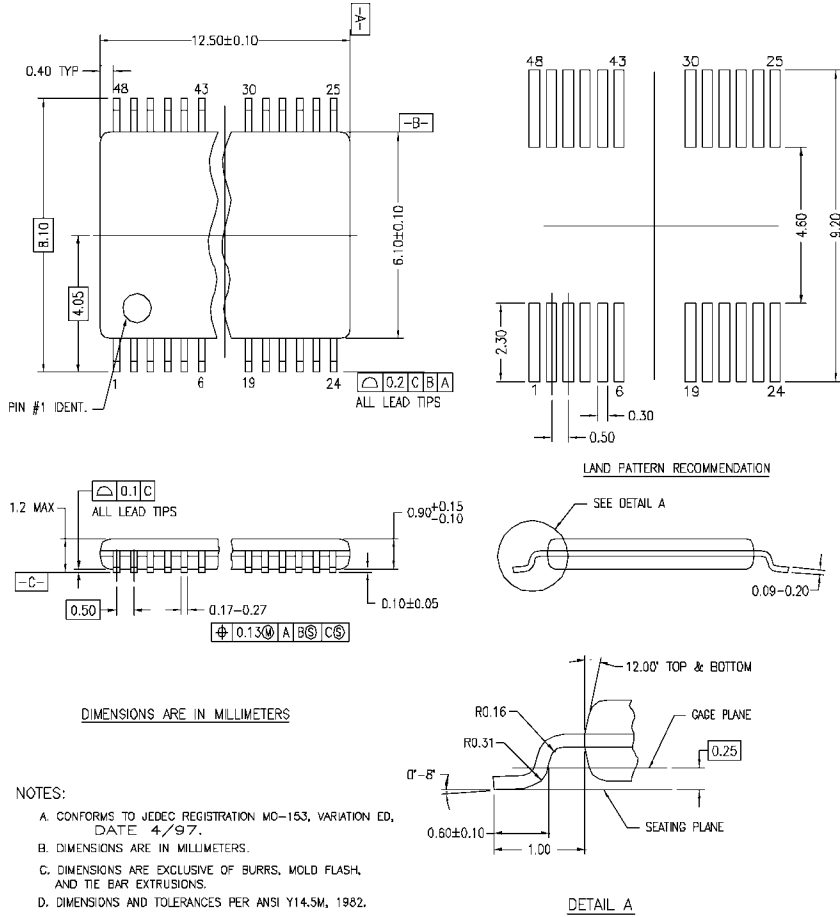
**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide  
Package Number BGA54A  
(Preliminary)**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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