74LVC3G06

Triple inverter with open-drain output

Rev. 03 — 01 February 2005 Product data sheet

1. General description

The 74LVC3G06 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC3G06 provides three inverting buffers.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- –24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PLZ}, t_{PZL}	propagation delay input nA to output nY	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ		-	2.6	-	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω		-	1.6	-	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω		-	2.2	-	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω		-	2.0	-	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω		-	1.4	-	ns
C_I	input capacitance			-	2.5	-	pF
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[1] [2]	-	5.9	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G06DP	–40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G06DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74LVC3G06GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

5. Marking

Table 3: Marking

Type number	Marking code
74LVC3G06DP	V06
74LVC3G06DC	V06
74LVC3G06GT	V06

6. Functional diagram

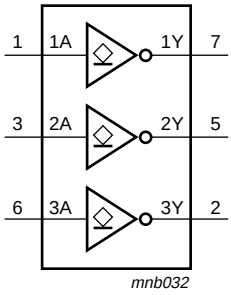


Fig 1. Logic symbol.

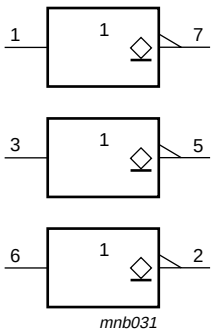


Fig 2. IEC logic symbol.

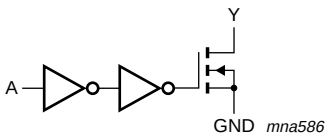


Fig 3. Logic diagram (one driver).

7. Pinning information

7.1 Pinning

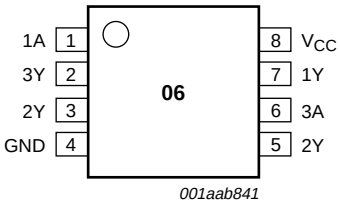
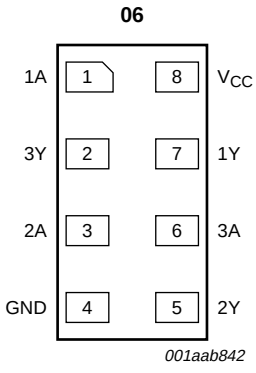


Fig 4. Pin configuration TSSOP8 and VSSOP8.



Transparent top view

Fig 5. Pin configuration XSON8.

7.2 Pin description

Table 4: Pin description

Symbol	Pin	Description
1A	1	data input
3Y	2	data output
2A	3	data input
GND	4	ground (0 V)
2Y	5	data output
3A	6	data input
1Y	7	data output
V_{CC}	8	supply voltage

8. Functional description

8.1 Function table

Table 5: Function table [1]

Input nA	Output nY
L	Z
H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
Z = high-impedance OFF-state.

9. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	active mode	[1]	–0.5	+6.5	V
		Power-down mode	[1] [2]	–0.5	+6.5	V
I_O	output sink current	V_O = 0 V to 6.5 V		-	50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C		-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

10. Recommended operating conditions

Table 7: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	-	10	ns/V

11. Static characteristics

Table 8: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V		0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V		-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V		-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V		-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V		-	-	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V		-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V
		I_O = 32 mA; V_{CC} = 4.5 V		-	-	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V	[2]	-	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V		-	±0.1	±10	µA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	±0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V		-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} – 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	[2]	-	5	500	µA

Table 8: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	input capacitance		-	2.5	-	pF
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V_{CC}	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.80	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V	-	-	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±10	μA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V	-	-	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	40	μA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 2.3 V to 5.5 V	-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.

[2] These typical values are measured at V_{CC} = 3.3 V.

12. Dynamic characteristics

Table 9: Dynamic characteristics

GND = 0 V; see Figure 7 for test circuit.

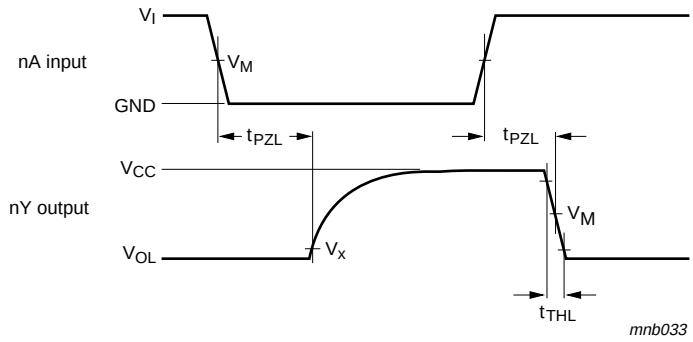
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PLZ}, t_{PZL}	propagation delay input nA to output nY	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		1.0	2.6	6.5	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	1.6	3.9	ns
		V_{CC} = 2.7 V		1.0	2.2	4.2	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	2.0	3.4	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	1.4	2.9	ns
C_{PD}	power dissipation capacitance per gate	V_{CC} = 3.3 V	[2] [3]	-	5.9	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PLZ}, t_{PZL}	propagation delay input nA to output nY	see Figure 6					
		V_{CC} = 1.65 V to 1.95 V		1.0	-	8.2	ns
		V_{CC} = 2.3 V to 2.7 V		0.5	-	4.9	ns
		V_{CC} = 2.7 V		1.0	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	-	4.3	ns
		V_{CC} = 4.5 V to 5.5 V		0.5	-	3.7	ns

[1] All typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[3] The condition is V_I = GND to V_{CC}.

13. Waveforms



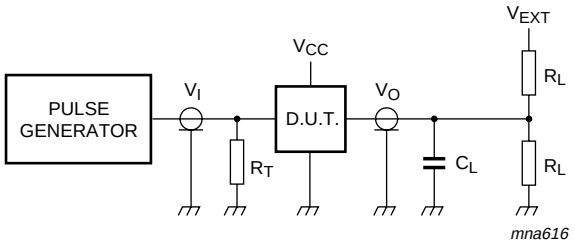
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 6. The input (nA) to output (nY) propagation delays.

Table 10: Measurement points

Supply voltage	Input			Output	
V_{CC}	V_M	V_I	$t_r = t_f$	V_M	V_X
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5 \times V_{CC}$	V_{OL} + 0.15 V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns	$0.5 \times V_{CC}$	V_{OL} + 0.15 V
2.7 V	1.5 V	2.7 V	≤ 2.5 ns	1.5 V	V_{OL} + 0.3 V
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns	1.5 V	V_{OL} + 0.3 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns	$0.5 \times V_{CC}$	V_{OL} + 0.3 V



Test data is given in Table 11.

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

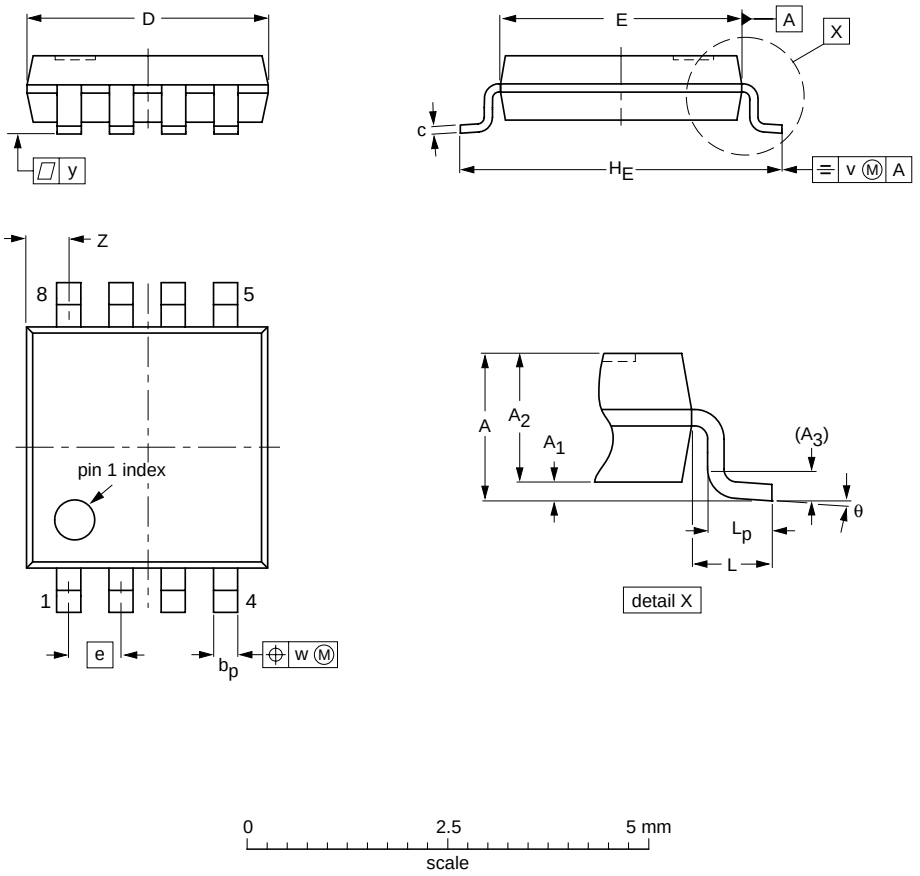
Fig 7. Load circuitry for switching times.

Table 11: Test data

Supply voltage	Input	Load		V_{EXT}
V_{CC}	V_I	C_L	R_L	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	$2 \times V_{CC}$

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

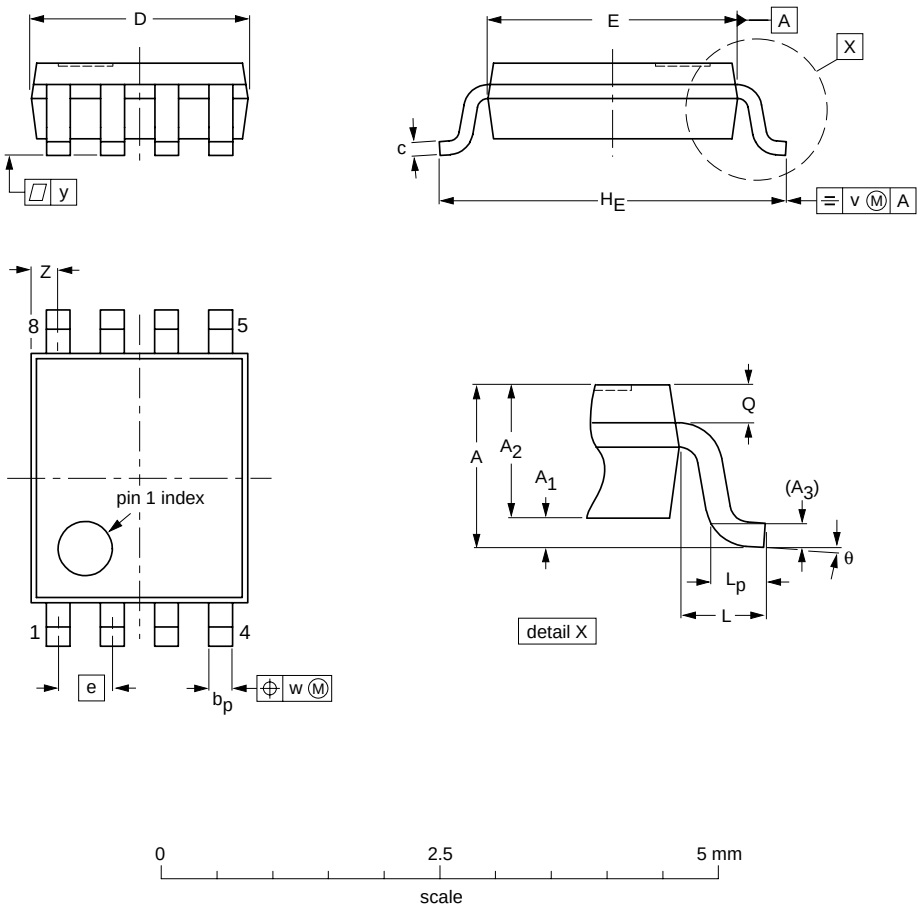
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig 8. Package outline SOT505-2 (TSSOP8).

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

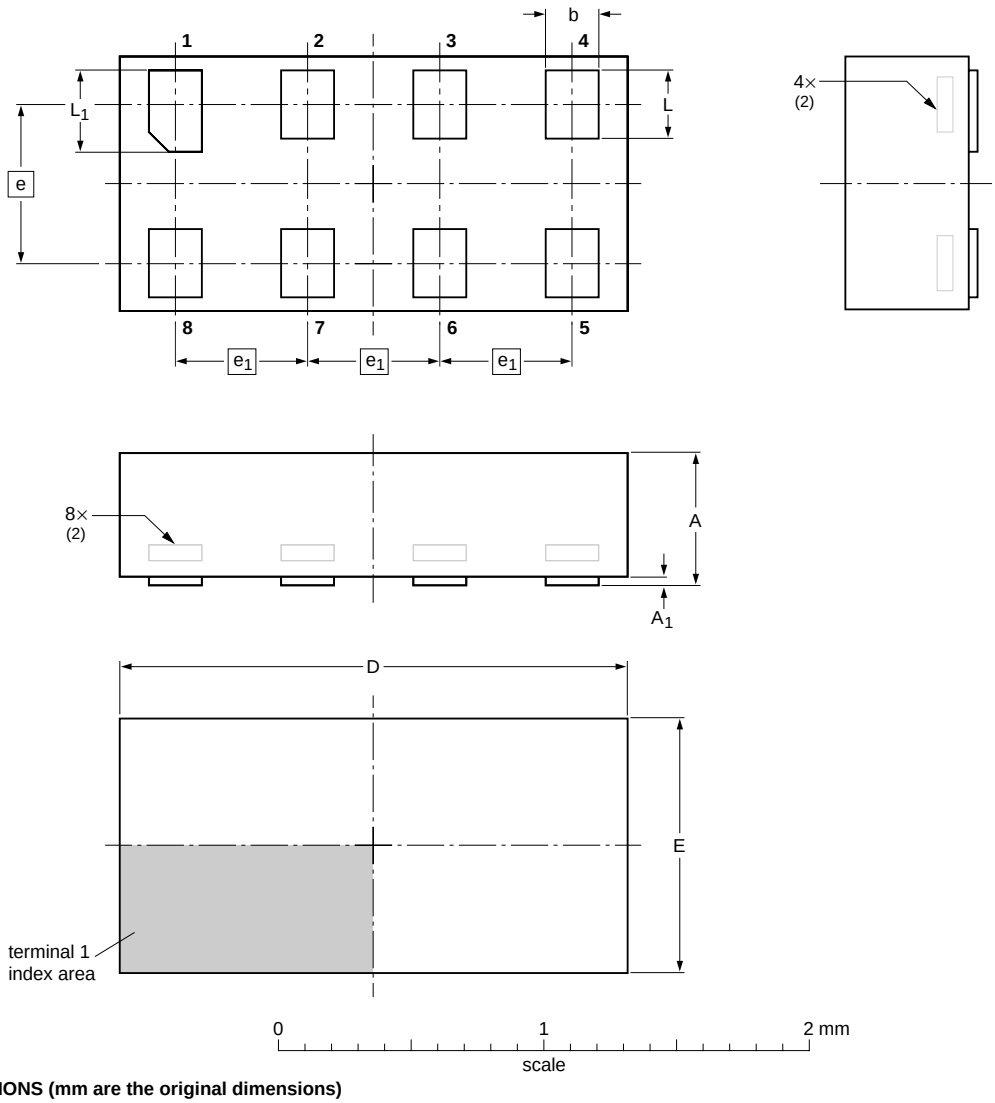
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 9. Package outline SOT765-1 (VSSOP8).

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~04-07-22~~ 04-11-09

Fig 10. Package outline SOT833-1 (XSON8).

15. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC3G06_3	20050201	Product data sheet	-	9397 750 14541	74LVC3G06_2
Modifications:	• Changed: type number 74LVC3G06GT (SOT833-1).				
74LVC3G06_2	20041021	Product data sheet	-	9397 750 13789	74LVC3G06_1
74LVC3G06_1	20040607	Product data sheet	-	9397 750 13266	-

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

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