DATA SHEET

74LV165A
8-bit parallel-in/serial-out shift register

Product specification

2003 Jul 23

Philips
Semiconductors

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8-bit parallel-in/serial-out shift register 74LV165A

FEATURES

- Wide supply voltage range from 2.0 to 5.5 V
- Complies with JEDEC standard:
  JESD8-5 (2.3 to 2.7 V)
  JESD8B/JESD36 (2.7 to 3.6 V)
  JESD8-1A (4.5 to 5.5 V).
- 5.5 V tolerant inputs/outputs
- CMOS LOW power consumption
- Direct interface with TTL levels (2.7 to 3.6 V)
- Power-down mode
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Latch-up performance exceeds 250 mA
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.

DESCRIPTION

The 74LV165A is a high-performance, low-power, low-voltage, Is-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging current back flow through the device when it is powered down.

The 74LV165A is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q7 and $\overline{Q}7$) available from the last stage. When the parallel-load input ($\overline{PL}$) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input $\overline{PL}$ is HIGH, data enters the register serially at the input DS and shifts one place to the right (Q0→Q1→Q2, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output Q7 to the input DS of the succeeding stage.

The clock input is a gate-OR structure which allows one input to be used as an active LOW clock enable input ($\overline{CE}$) input. The pin assignment for the inputs CP and $\overline{CE}$ is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input $\overline{CE}$ should only take place while CP HIGH for predictable operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay	V_{CC} = 3.3 V; C_L = 15 pF		
	$\overline{CE}$, CP to Q7, $\overline{Q}7$		7.5	ns
	$\overline{PL}$ to Q7, $\overline{Q}7$		8.0	ns
	D7 to Q7, $\overline{Q}7$		8.5	ns
f_{max}	maximum clock frequency	V_{CC} = 3.3 V; C_L = 15 pF	115	MHz
C_I	input capacitance		3.0	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2	24	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_i = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	PACKAGES			
	PINS	PACKAGE	MATERIAL	CODE
74LV165AD	16	SO16	plastic	SOT109-1
74LV165APW	16	TSSOP16	plastic	SOT403-1

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT					ON REGISTER		OUTPUT	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	$\overline{Q}$7
Parallel load	L	X	X	X	L	L	L–L	L	H
	L	X	X	X	H	H	H–H	H	L
Serial shift	H	L	↑	l	X	L	q0–q5	q6	$\overline{q}$6
	H	L	↑	h	X	H	q0–q5	q6	$\overline{q}$6
Serial shift	H	↑	L	l	X	L	q0–q5	q6	$\overline{q}$6
	H	↑	L	h	X	H	q0–q5	q6	$\overline{q}$6
Hold “do nothing”	H	H	X	X	X	q0	q1–q6	q7	$\overline{q}$7
Hold “do nothing”	H	X	H	X	X	q0	q1–q6	q7	$\overline{q}$7

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
   q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;
   X = don’t care;
   ↑ = LOW-to-HIGH clock transition.

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{PL}$	asynchronous parallel load input (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3	D4	parallel data input
4	D5	parallel data input
5	D6	parallel data input
6	D7	parallel data input
7	$\overline{Q}7$	complementary serial output from the last stage
8	GND	ground (0 V)
9	Q7	serial output from the last stage
10	DS	serial data input
11	D0	parallel data input
12	D1	parallel data input
13	D2	parallel data input
14	D3	parallel data input
15	$\overline{CE}$	clock enable input (active LOW)
16	V_{CC}	supply voltage

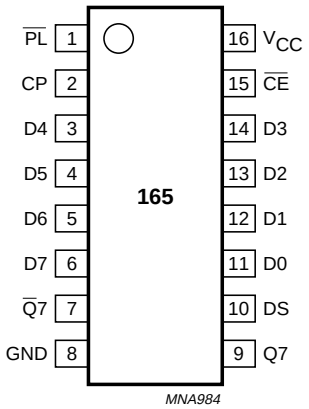


Fig.1 Pin configuration.

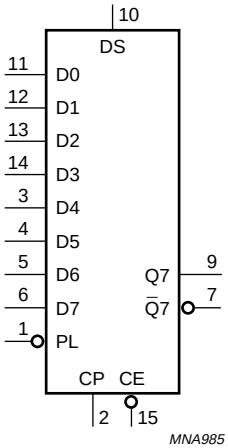


Fig.2 Logic symbol.

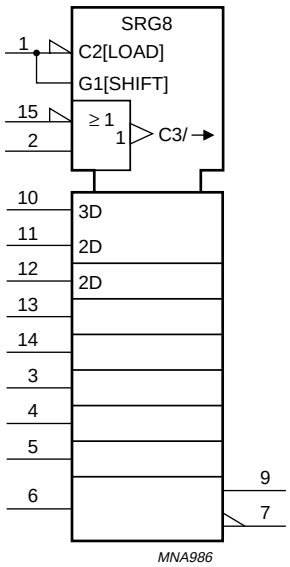


Fig.3 Logic symbol (IEEE/IEC).

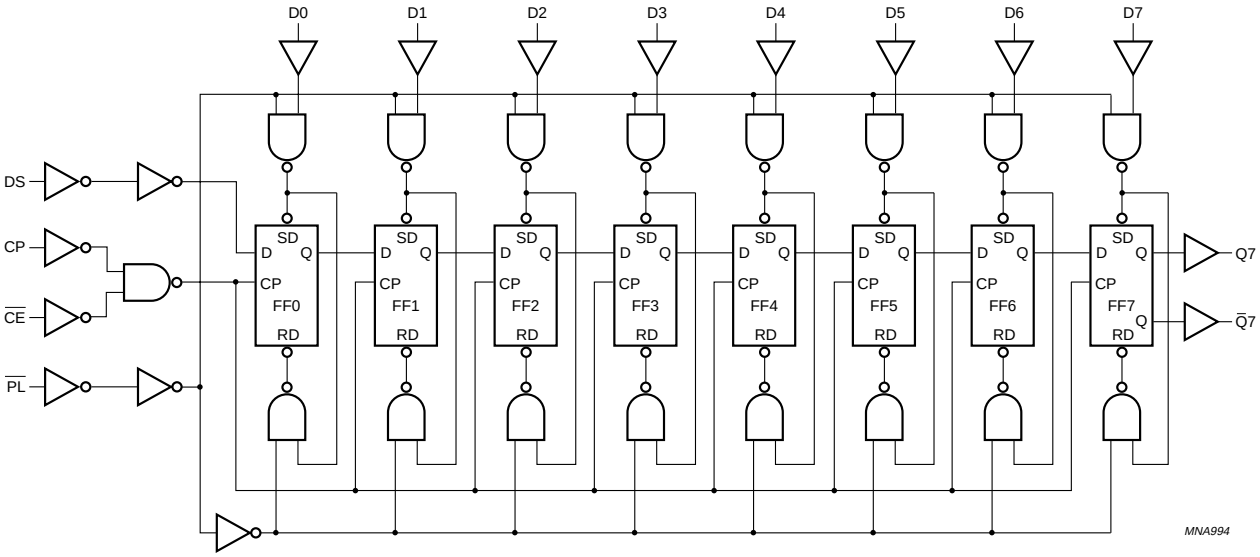


Fig.4 Logic diagram.

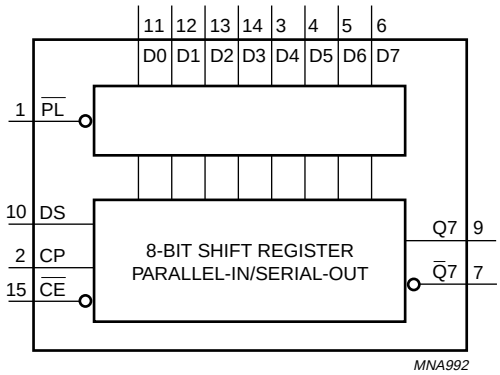


Fig.5 IEC logic symbol.

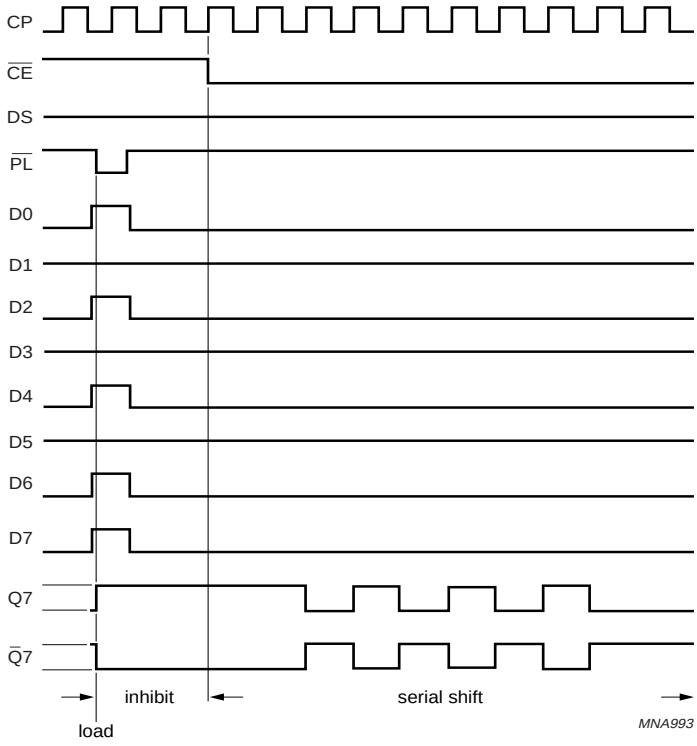


Fig.6 Timing diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		2.0	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+85	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.3 to 2.7 V	0	200	ns/V
		V_{CC} = 3.0 to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 to 5.5 V	0	20	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	V_I < 0	–	–20	mA
V_I	input voltage		–0.5	+7.0	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0	–	±50	mA
V_O	output voltage	note 1	–0.5	V_{CC} + 0.5	V
		Power-down mode	–0.5	+7.0	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 to +85 °C; note 2	–	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO16 packages: above 70 °C derate linearly with 8 mW/K.
   For TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 to +85 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			2.3 to 2.7	$0.7 \times V_{CC}$	–	–	V
			3.0 to 3.6	$0.7 \times V_{CC}$	–	–	V
			4.5 to 5.5	$0.7 \times V_{CC}$	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			2.3 to 2.7	–	–	$0.3 \times V_{CC}$	V
			3.0 to 3.6	–	–	$0.3 \times V_{CC}$	V
			4.5 to 5.5	–	–	$0.3 \times V_{CC}$	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 50 μA	2.0 to 5.5	–	–	0.1	V
		I_O = 2 mA	2.3	–	–	0.4	V
		I_O = 6 mA	3.0	–	–	0.44	V
		I_O = 12 mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −50 μA	2.0 to 5.5	$V_{CC} - 0.1$	–	–	V
		I_O = −2 mA	2.3	2.0	–	–	V
		I_O = −6 mA	3.0	2.48	–	–	V
		I_O = −12 mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.01	±1	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0.0	–	±0.05	±5	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0	5.5	–	0.2	20	μA

Note

1. All typical values are measured at V_{CC} = 5.5 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 3.0$ ns.

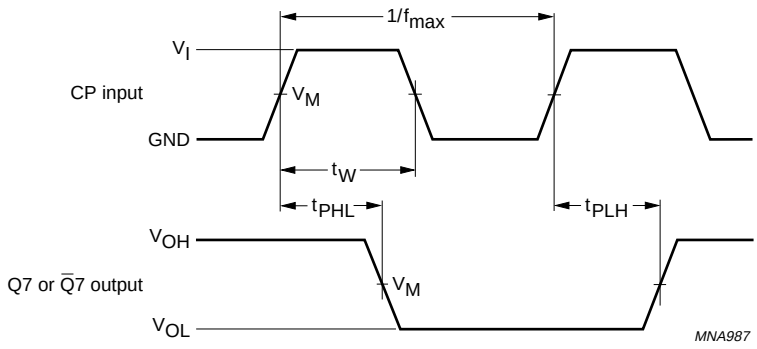
SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.(1)	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)	C_L (pF)				
T_{amb} = −40 to +85 °C								
t_{PLH}/t_{PHL}	propagation delay $\overline{CE}$, CP to Q7, $\overline{Q}$7	see Figs 7, 8 and 12	2.3 to 2.7	15	1.0	11.0	22.0	ns
			3.0 to 3.6	15	1.0	7.5	18.0	ns
			4.5 to 5.5	15	1.0	5.5	11.5	ns
t_{PLH}/t_{PHL}	propagation delay $\overline{PL}$ to Q7, $\overline{Q}$7	see Figs 7, 8 and 12	2.3 to 2.7	15	1.0	11.5	23.5	ns
			3.0 to 3.6	15	1.0	8.0	18.5	ns
			4.5 to 5.5	15	1.0	5.5	11.5	ns
t_{PLH}/t_{PHL}	propagation delay D7 to Q7, $\overline{Q}$7	see Figs 9 and 12	2.3 to 2.7	15	1.0	12.0	24.0	ns
			3.0 to 3.6	15	1.0	8.5	16.5	ns
			4.5 to 5.5	15	1.0	6.0	10.5	ns
t_{PLH}/t_{PHL}	propagation delay $\overline{CE}$, CP to Q7, $\overline{Q}$7	see Figs 7, 8 and 12	2.3 to 2.7	50	1.0	13.0	26.0	ns
			3.0 to 3.6	50	1.0	9.0	21.5	ns
			4.5 to 5.5	50	1.0	6.1	13.5	ns
t_{PLH}/t_{PHL}	propagation delay $\overline{PL}$ to Q7, $\overline{Q}$7	see Figs 7, 8 and 12	2.3 to 2.7	50	1.0	14.0	28.0	ns
			3.0 to 3.6	50	1.0	10.0	22.0	ns
			4.5 to 5.5	50	1.0	6.5	13.5	ns
t_{PLH}/t_{PHL}	propagation delay D7 to Q7, $\overline{Q}$7	see Figs 9 and 12	2.3 to 2.7	50	1.0	14.0	28.0	ns
			3.0 to 3.6	50	1.0	10.0	20.0	ns
			4.5 to 5.5	50	1.0	6.5	12.5	ns
t_W	clock pulse with HIGH to LOW	see Figs 7, 8 and 12	2.3 to 2.7	–	9.0	–	–	ns
			3.0 to 3.6	–	7.0	–	–	ns
			4.5 to 5.5	–	4.0	–	–	ns
t_W	parallel load pulse with LOW	see Figs 7, 8 and 12	2.3 to 2.7	–	13.0	–	–	ns
			3.0 to 3.6	–	9.0	–	–	ns
			4.5 to 5.5	–	6.0	–	–	ns
t_{rem}	removal time $\overline{PL}$ to CP, $\overline{CE}$	see Figs 8 and 12	2.3 to 2.7	–	8.5	–	–	ns
			3.0 to 3.6	–	6.0	–	–	ns
			4.5 to 5.5	–	4.0	–	–	ns
t_{su}	set-up time DS to CP, $\overline{CE}$	see Figs 10, 11 and 12	2.3 to 2.7	–	9.5	–	–	ns
			3.0 to 3.6	–	6.0	–	–	ns
			4.5 to 5.5	–	4.0	–	–	ns
t_{su}	set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	see Figs 10, 11 and 12	2.3 to 2.7	–	7.0	–	–	ns
			3.0 to 3.6	–	5.0	–	–	ns
			4.5 to 5.5	–	3.5	–	–	ns

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.(1)	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)	C_L (pF)				
t_{su}	set-up time Don to $\overline{PL}$	see Figs 10, 11 and 12	2.3 to 2.7	–	12.0	–	–	ns
			3.0 to 3.6	–	8.5	–	–	ns
			4.5 to 5.5	–	5.0	–	–	ns
t_h	hold time DS to CP; $\overline{CE}$ $\overline{PL}$ to CP; $\overline{CE}$	see Figs 10, 11 and 12	2.3 to 2.7	–	0	–	–	ns
			3.0 to 3.6	–	0	–	–	ns
			4.5 to 5.5	–	0.5	–	–	ns
t_h	hold time Don to $\overline{PL}$	see Figs 10, 11 and 12	2.3 to 2.7	–	0.5	–	–	ns
			3.0 to 3.6	–	0.5	–	–	ns
			4.5 to 5.5	–	1.0	–	–	ns
f_{max}	maximum clock pulse frequency	see Figs 7 and 12	2.3 to 2.7	15	45	80	–	MHz
			3.0 to 3.6	15	55	115	–	MHz
			4.5 to 5.5	15	90	165	–	MHz
			2.3 to 2.7	50	35	65	–	MHz
			3.0 to 3.6	50	50	90	–	MHz
			4.5 to 5.5	50	85	125	–	MHz

Note

1. All typical values are measured at T_{amb} = 25 °C.

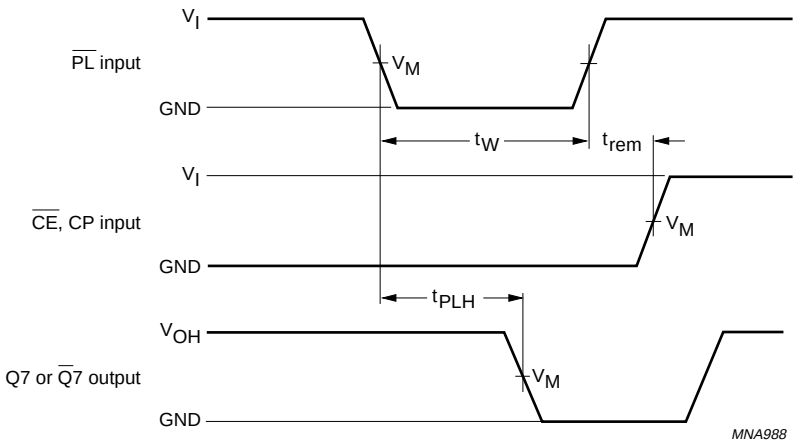
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns
3.0 to 3.6 V	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns

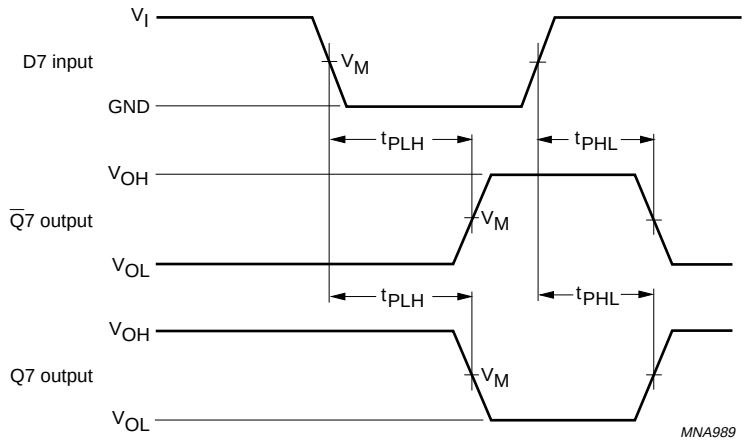
The changing to output assumes internal Q6 opposite state from Q7.

Fig.7 Clock pulse (CP) to output (Q7 or $\overline{Q}$7) propagation delays, the clock pulse width and the maximum clock frequency.



The changing to output assumes internal Q6 opposite state from Q7.

Fig.8 Parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q7 or $\overline{Q}$7) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.



The changing to output assumes internal Q6 opposite state from Q7.

Fig.9 Data input (Don) to output (Q7 or $\overline{Q}$7) propagation delays when $\overline{PL}$ is LOW.

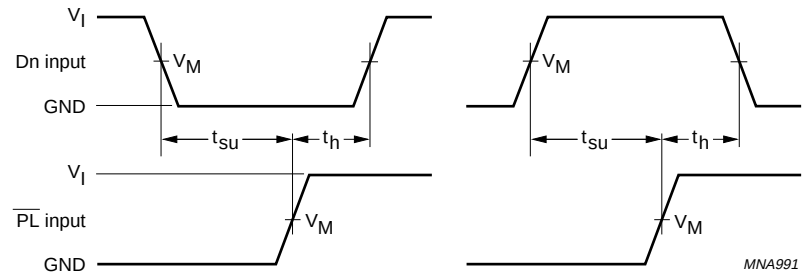
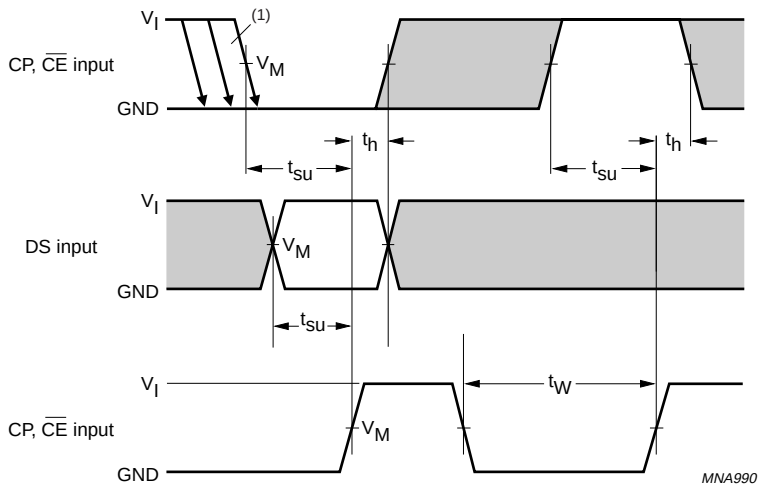
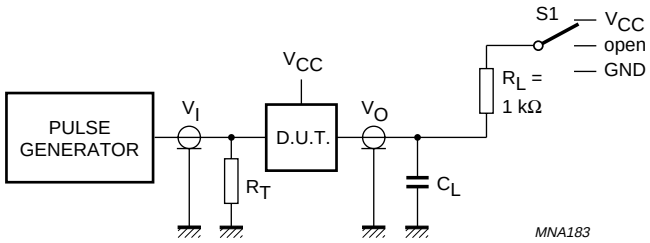


Fig.10 Set-up and hold times from the data inputs (Don) to the parallel load input ($\overline{PL}$).



(1) $\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.11 Set-up and hold times from the serial data input (DS) to the clock (CP) and the clock enable inputs ($\overline{CE}$), from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).



TEST	S1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

R_L = Load resistor.

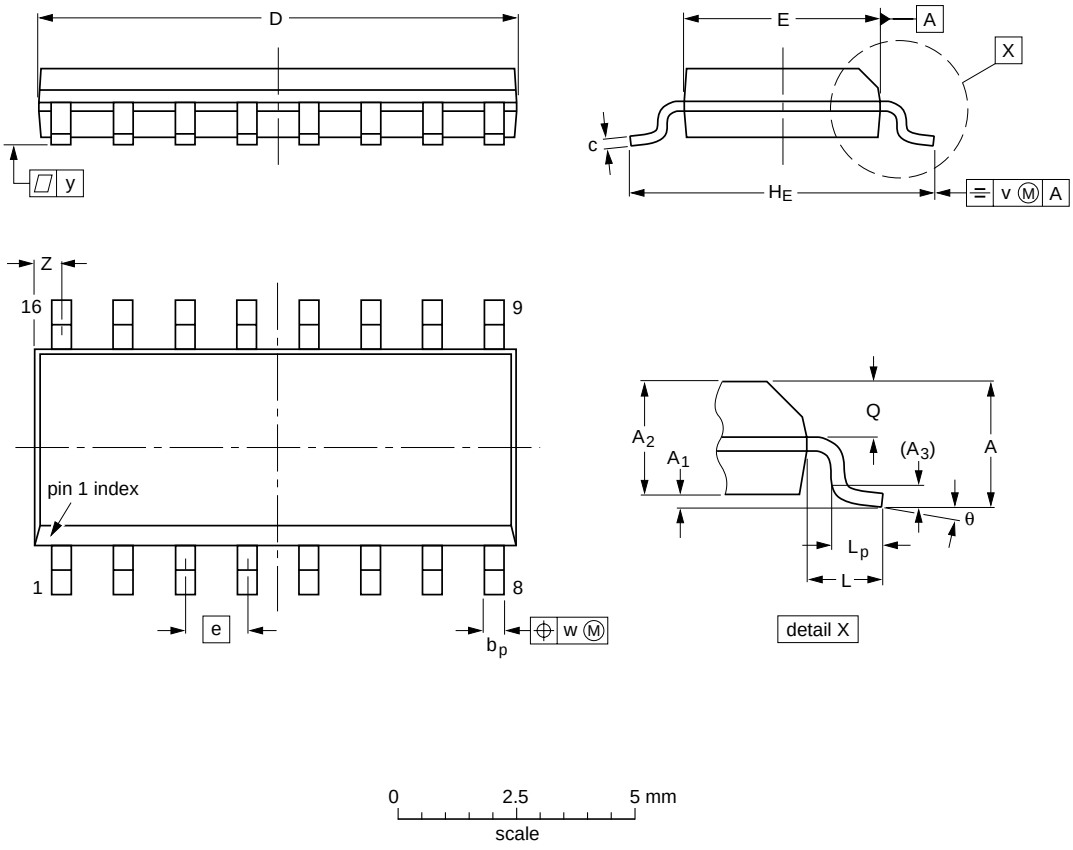
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.12 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

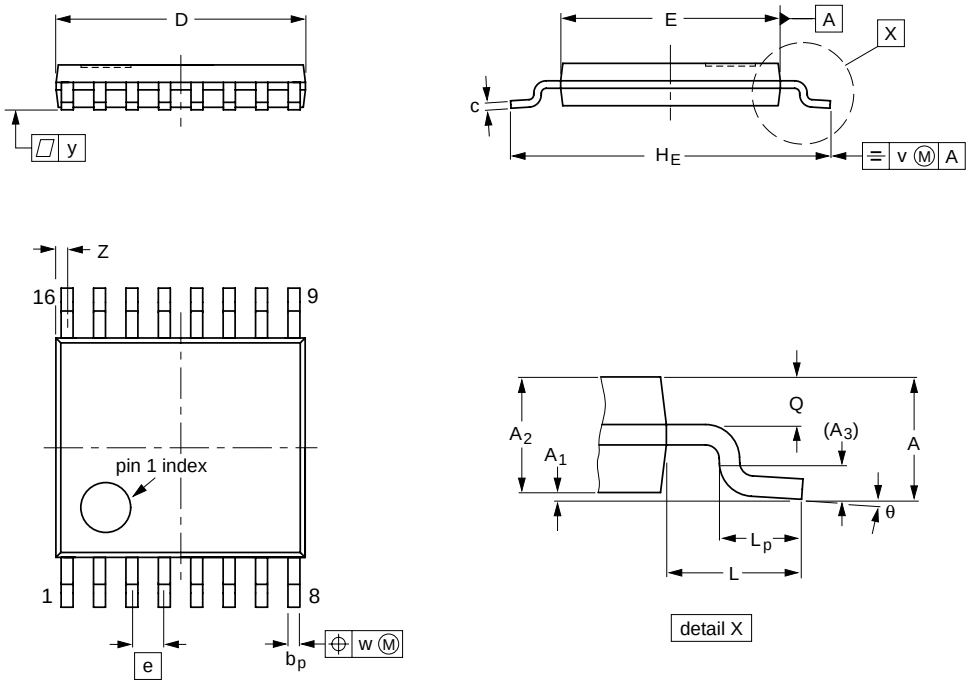
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

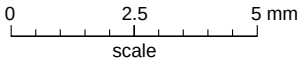
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Interned at URL tap://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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