

74F574 Octal D-Type Flip-Flop with 3-STATE Outputs

General Description

The 74F574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (\overline{OE}). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

This device is functionally identical to the 74F374 except for the pinouts.

Features

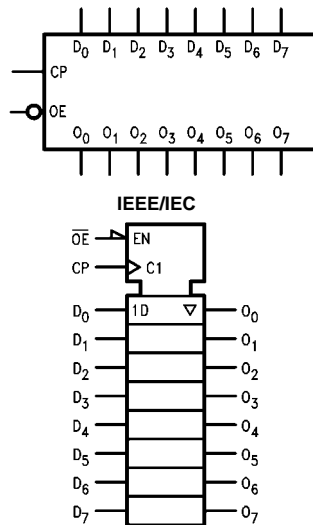
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 74F374
- 3-STATE outputs for bus-oriented applications

Ordering Code:

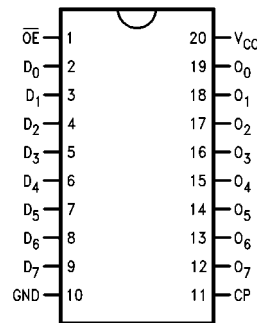
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F574SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74F574SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F574PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
|--------------------------------|--|------------------|---|
| D ₀ -D ₇ | Data Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| CP | Clock Pulse Input (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| \overline{OE} | 3-STATE Output Enable Input (Active LOW) | 1.0/1.0 | 20 μ A/-0.6 mA |
| O ₀ -O ₇ | 3-STATE Outputs | 150/40 (33.3) | -3 mA/24 mA (20 mA) |

Functional Description

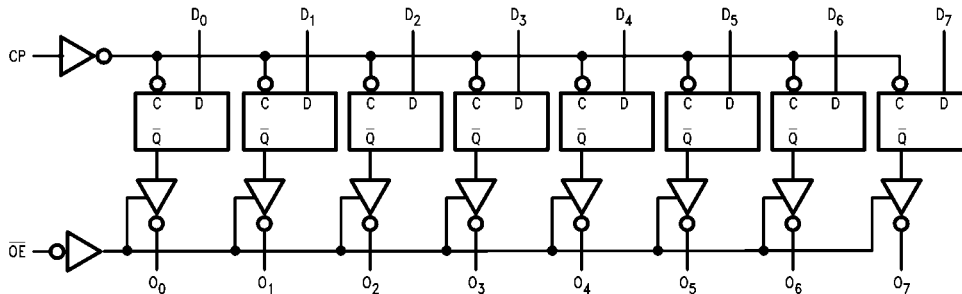
The 74F574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (\overline{OE}) LOW, the contents of the eight flip-flops are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Function Table

| Inputs | | | Internal | Outputs | Function |
|-----------------|------------|---|----------|---------|-------------------|
| \overline{OE} | CP | D | Q | O | |
| H | H | L | NC | Z | Hold |
| H | H | H | NC | Z | Hold |
| H | \nearrow | L | L | Z | Load |
| H | \nearrow | H | H | Z | Load |
| L | \nearrow | L | L | L | Data Available |
| L | \nearrow | H | H | H | Data Available |
| L | H | L | NC | NC | No Change in Data |
| L | H | H | NC | NC | No Change in Data |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 \nearrow = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|---|-------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |

Voltage Applied to Output

in HIGH State (with V_{CC} = 0V)Standard Output -0.5V to V_{CC}

3-STATE Output -0.5V to +5.5V

Current Applied to Output

in LOW State (Max) twice the rated I_{OL} (mA)**Recommended Operating Conditions**

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|-----|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} 2.5 10% V _{CC} 2.4 5% V _{CC} 2.7 5% V _{CC} 2.7 | | | V | Min | I _{OH} = -1 mA I _{OH} = -3 mA I _{OH} = -1 mA I _{OH} = -3 mA |
| V _{OL} | Output LOW Voltage | 10% V _{CC} | | 0.5 | V | Min | I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V |
| I _{OZH} | Output Leakage Current | | | 50 | μA | Max | V _{OUT} = 2.7V |
| I _{OZL} | Output Leakage Current | | | -50 | μA | Max | V _{OUT} = 0.5V |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{ZZ} | Bus Drainage Test | | | 500 | μA | 0.0V | V _{OUT} = 5.25V |
| I _{CCZ} | Power Supply Current | | 55 | 86 | mA | Max | V _O = HIGH Z |

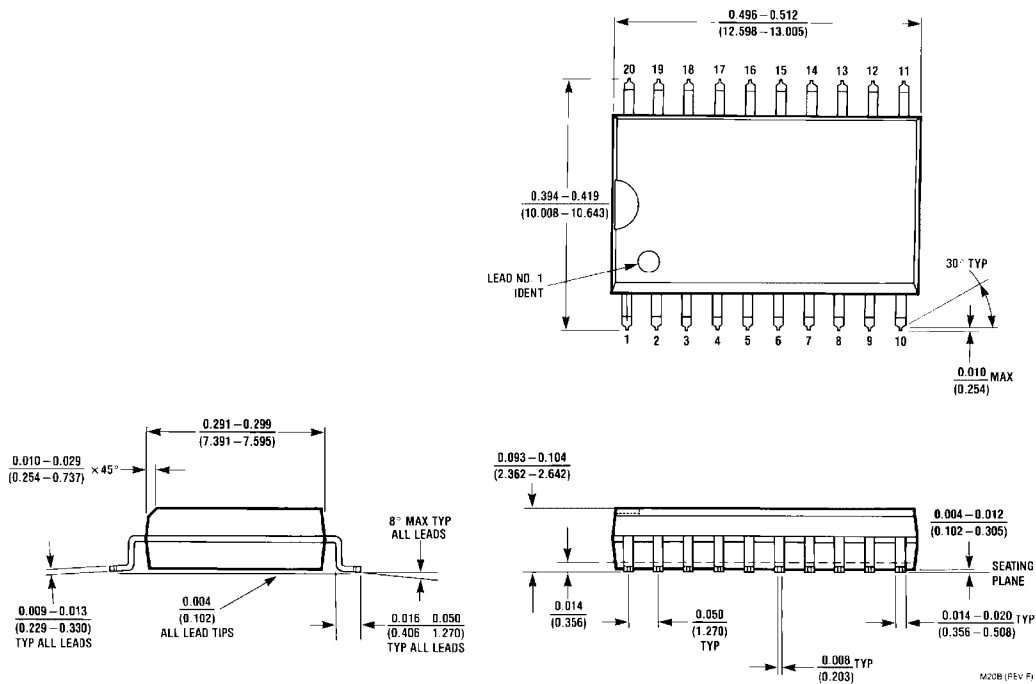
AC Electrical Characteristics

| Symbol | Parameter | $T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ | | Units |
|-----------|-------------------------|--|-----|-----|---|------|--|------|-------|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| f_{MAX} | Maximum Clock Frequency | 100 | | | 60 | | 70 | | MHz |
| t_{PLH} | Propagation Delay | 2.5 | 5.3 | 8.5 | 2.5 | 9.5 | 2.5 | 8.5 | ns |
| t_{PHL} | CP to O_n | 2.5 | 5.3 | 8.5 | 2.5 | 9.5 | 2.5 | 8.5 | |
| t_{PZH} | Output Enable Time | 3.0 | 5.5 | 9.0 | 2.5 | 10.5 | 2.5 | 10.0 | ns |
| t_{PZL} | | 3.0 | 6.0 | 9.0 | 2.5 | 10.5 | 2.5 | 10.0 | |
| t_{PHZ} | Output Disable Time | 1.5 | 3.3 | 5.5 | 1.5 | 7.0 | 1.5 | 6.5 | ns |
| t_{PLZ} | | 1.5 | 2.8 | 5.5 | 1.5 | 7.0 | 1.5 | 6.5 | |

AC Operating Requirements

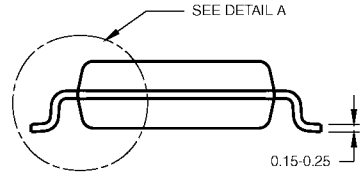
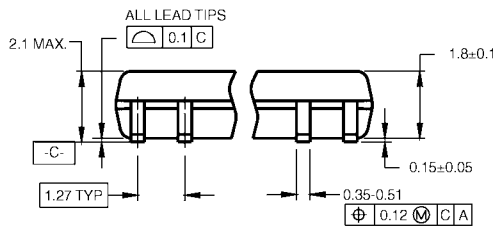
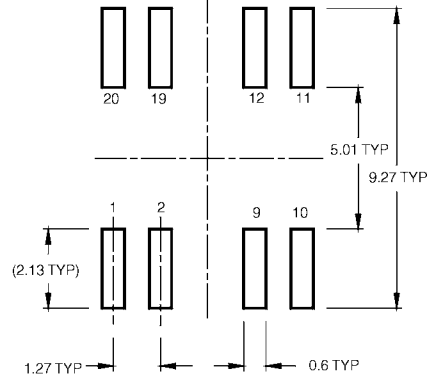
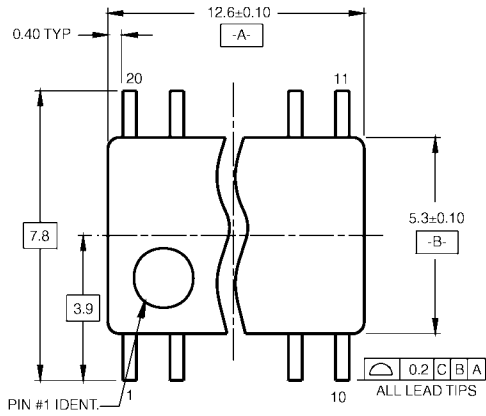
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|----------|--------------------------|--|-----|---|-----|--|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| $t_S(H)$ | Set-up Time, HIGH or LOW | 2.5 | | 3.0 | | 2.5 | | ns |
| $t_S(L)$ | D_n to CP | 2.0 | | 2.5 | | 2.0 | | |
| $t_H(H)$ | Hold Time, HIGH or LOW | 2.0 | | 2.0 | | 2.0 | | ns |
| $t_H(L)$ | D_n to CP | 2.0 | | 2.0 | | 2.0 | | |
| $t_W(H)$ | CP Pulse Width | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_W(L)$ | HIGH or LOW | 5.0 | | 5.0 | | 5.0 | | |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

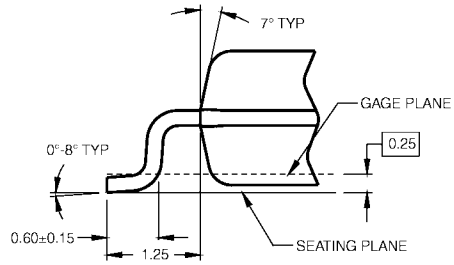
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

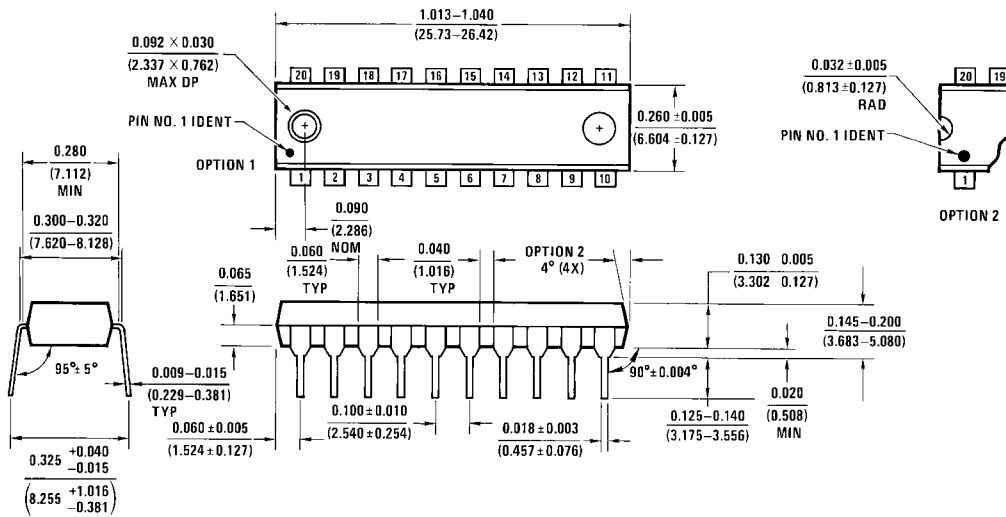
M20DRevB1



DETAIL A

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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