56F8023

Preliminary Chip Errata

56F8023 Digital Signal Controller

This document reports errata information on chip revision A. Errata numbers are in the form n.m, where n is the number of the errata item and m identifies the document revision number. This document is a pre-publication draft.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8023 devices.

Errata Number	Description	Impact and Work Around
1.0	In the DAC, the up/down counter which implements waveform generation in automatic mode in the DAC gasket does not handle negative numbers.	Impact: Down counting to a negative number will wrap the counter and continue down counting. Work Around: Adjust MAXVAL, MINVAL, and/or STEP size so the terminal value while down counting is positive or zero.
2.0	I^2C fails to detect arbitration loss when the loss occurs while the ACK bit of data bytes is received in master RX mode.	Impact: No impact on bus behavior. Arbitration loss software counters will not be accurate in this situation. Work Around: None available.
3.0	Some I^2C slave TX FIFO flushes don't interrupt the CPU.	Impact: If the number of bytes written to the TX FIFO exceeds the number of data bytes retrieved by the remote master, there is no CPU indication that the excess data bytes were flushed from the TX FIFO. Software must accommodate this behavior Work Around: None available
4.0	I^2C ACKs its own address and data during general calls when both master and slave are enabled and the module initiates the general call. This means the transmission will always be completed and it's impossible to determine if another device is ACKing the call.	Impact: Since the module always ACKs the general call address and data in the scenario, the module will never know if any of the other nodes NACKed the general call. Use work around until fixed. Work Around: Disable slave mode prior to initiating a general call.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8023 devices.

Errata Number	Description	Impact and Work Around
5.0	Although required by the Philips spec, the I^2C does not reset its bus logic, and thereby prepare to receive address following an unexpected START or repeated START. An unexpected START or repeated START is one that is not positioned according to the proper format.	Impact: Avoid all unexpected START conditions. Typically, this is not an issue in a single master system. In a multi-master system, avoid an unexpected START by powering up all master I^2Cs while the bus remains idle or by initiating master activity in a newly powered up master only when the bus is idle. Work Around: Use work around until fixed.
6.0	The I^2C bus locks up when disabled in slave TX mode.	Impact: Same as description. Work Around: The user's software must ensure that *slv_activity* and *mst_activity* are deasserted when disabling the module. To prevent this problem, follow the full module disabling procedure outlined in documentation.
7.0	If you power up the I^2C in master mode and write to the TX FIFO for the first time while the bus is not idle, the I^2C may transmit onto the non-idle bus.	Impact: Same as description. Work Around: If it's possible to power up the module while the bus is busy, the user should monitor for I^2C bus STOP detection or idle conditions before writing to the TX FIFO for the first time.
8.0	I^2C may deassert interrupts during module disabling.	Impact: Same as description; reported to inform user of related module functionality. Work Around: Once enabled, if I^2C is disabled, the user's software must be able to manage the possible deassertion of asserted interrupt outputs.
9.0	I^2C prematurely releases SCL in slave TX abort, causing all-ones data to be clocked out.	Impact: Same as description. Work Around: While operating in slave transmitter mode, do not write a read command to the TX FIFO .
10.0	I^2C provides only one IPBus clock period of noise suppression.	Impact: Same as description. Work Around: Ensure that noise spikes do not exceed one IPBus clock period.

Chip Revision A Errata Information:

The following errata items apply only to Revision A 56F8023 devices.

Errata Number	Description	Impact and Work Around
11.0	If the I^2C is generating a STOP condition on the bus, the CPU cannot write to the TX FIFO following a transmit abort.	Impact: Same as description. Work Around: If a transmit abort interrupt service routing needs to write data to the TX FIFO, poll the STAT register's ACT bit (bit 0) until the bit is zero, before writing to the TX FIFO. This work around is needed only if the TX abort source generates a STOP condition on the bus. The following TX abort sources generate STOP conditions: RNORST, SACKDET, GCREAD, GCNACK, TDNACK, AD2NACK, AD1NACK, and AD7NACK.
12.0	In the ADC, V_{REFL} and V_{REFH} functions are attached to the wrong ADC channels and thus are pinned out on the wrong external GPIO pads.	**This errata will be corrected in Revision B of the device (production version).**
13.0	ROSC exceeds its -3% frequency variation spec when operating below -20°C.	Impact: The SCI interface can malfinction if the part is operating on the ROSC and the frequency variation spec is violated. Work Around: Avoid using the SCI or other frequency critical functionality when operating below -20°C.

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MC56F8023E
Rev. 0
09/2006