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# 4AM13

Silicon N-Channel/P-Channel Power MOS FET Array

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## Application

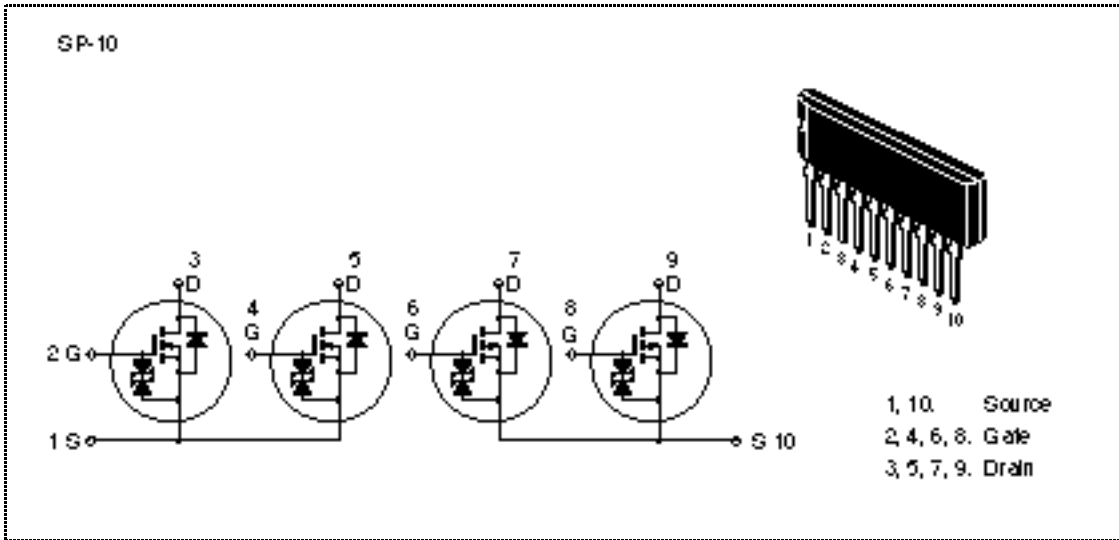
High speed power switching

## Features

- Low on-resistance  
N-channel:  $R_{DS(on)} = 0.4 \Omega$ ,  $V_{GS} = 10 \text{ V}$ ,  $I_D = 1.5 \text{ A}$   
P-channel:  $R_{DS(on)} = 0.45 \Omega$ ,  $V_{GS} = -10 \text{ V}$ ,  $I_D = -1.5 \text{ A}$
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for H-bridged motor driver

# 4AM13

## Outline



### Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

Item	Symbol	Rating		Unit
		Nch	Pch	
Drain to source voltage	$V_{DSS}$	60	-60	V
Gate to source voltage	$V_{GSS}$	±20	±20	V
Drain current	$I_D$	3	-3	A
Drain peak current	$I_{D(pulse)}^{*1}$	12	-12	A
Body to drain diode reverse drain current	$I_{DR}$	3	-3	A
Channel dissipation	$P_{ch} (T_c = 25^\circ C)^{*2}$	28		W
Channel dissipation	$P_{ch}^{*2}$	4		W
Channel temperature	$T_{ch}$	150		°C
Storage temperature	$T_{stg}$	-55 to +150		°C

Notes: 1. PW 10 μs, duty cycle 1%

2. 4 Devices operation

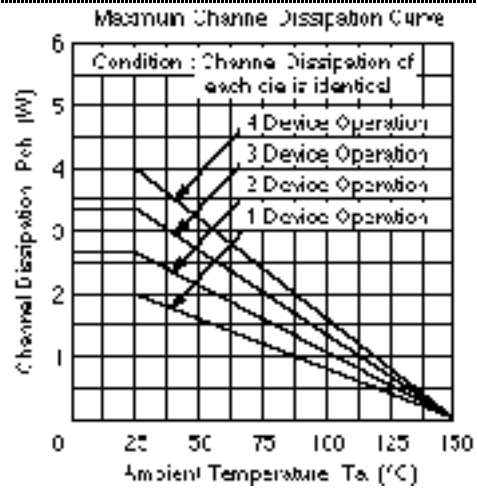
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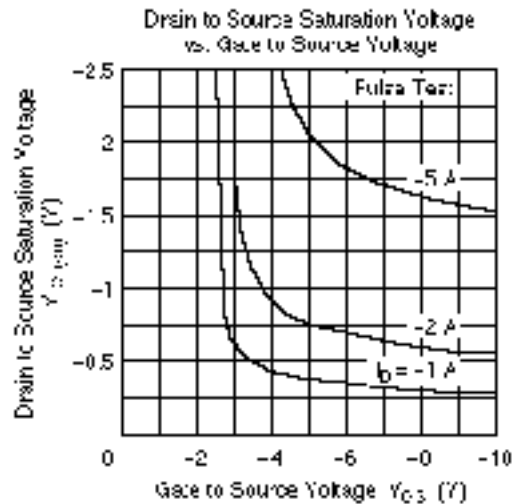
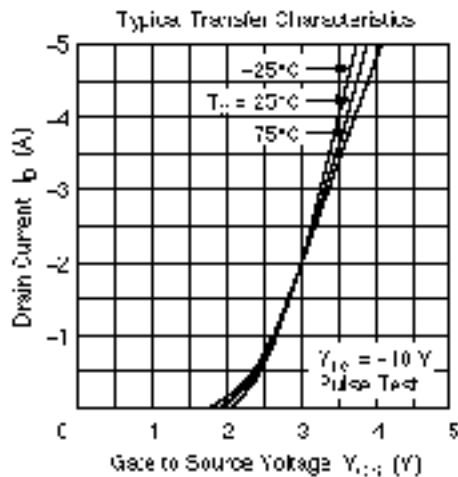
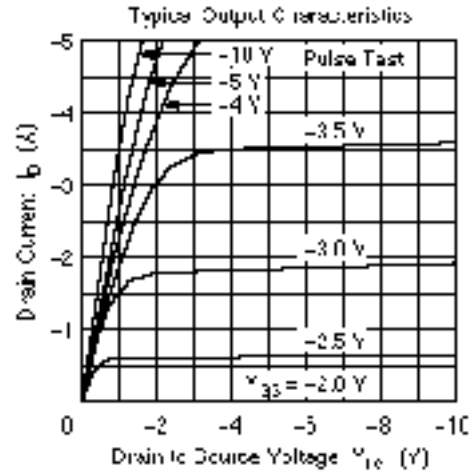
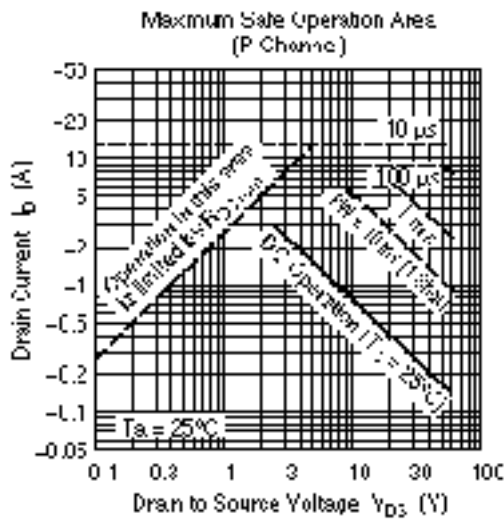
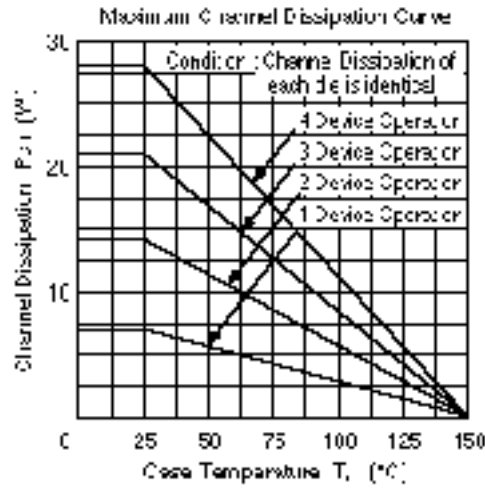
## Electrical Characteristics (Ta = 25°C) (1 Unit)

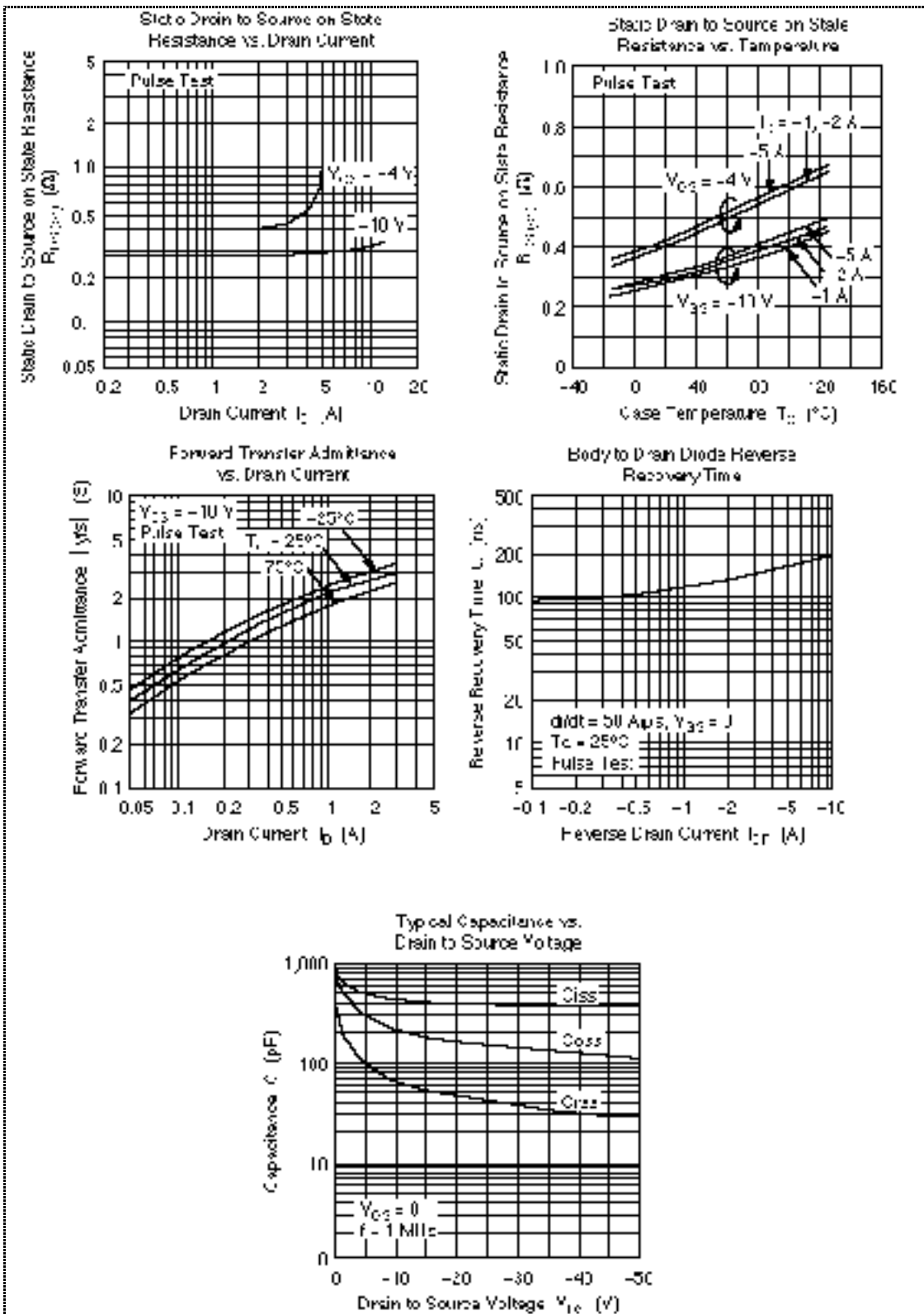
Item	Symbol	N channel			P channel			Unit	Test conditions
		Min	Typ	Max	Min	Typ	Max		
Drain to source breakdown voltage	$V_{(BR)DS}$	60	—	—	-60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GS}$	$\pm 20$	—	—	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	250	—	—	-250	$\mu\text{A}$	$V_{DS} = 50 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	-1.0	—	-2.0	V	$I_D = 1 \text{ mA}, V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.25	0.35	—	0.28	0.4		$I_D = 1.5 \text{ A}, V_{GS} = 10 \text{ V}^{*1}$
		—	0.35	0.5	—	0.4	0.55		$I_D = 1.5 \text{ A}, V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	1.5	2.5	—	1.5	2.5	—	S	$I_D = 1.5 \text{ A}, V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	240	—	—	400	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$
Output capacitance	$C_{oss}$	—	115	—	—	240	—	pF	$f = 1 \text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	—	35	—	—	70	—	pF	
Turn-on delay time	$t_{d(on)}$	—	4	—	—	5	—	ns	$I_D = 1.5 \text{ A}, V_{GS} = 10 \text{ V},$
Rise time	$t_r$	—	20	—	—	25	—	ns	$R_L = 20$
Turn-off delay time	$t_{d(off)}$	—	80	—	—	180	—	ns	
Fall time	$t_f$	—	40	—	—	80	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	1.2	—	—	-1.1	—	V	$I_F = 3 \text{ A}, V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	75	—	—	140	—	ns	$I_F = 3 \text{ A}, V_{GS} = 0,$ $dI_F/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse Test

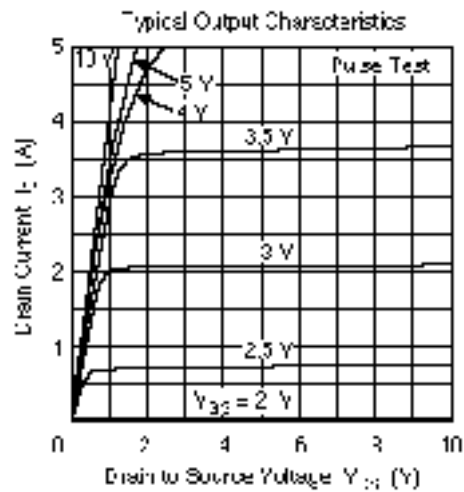
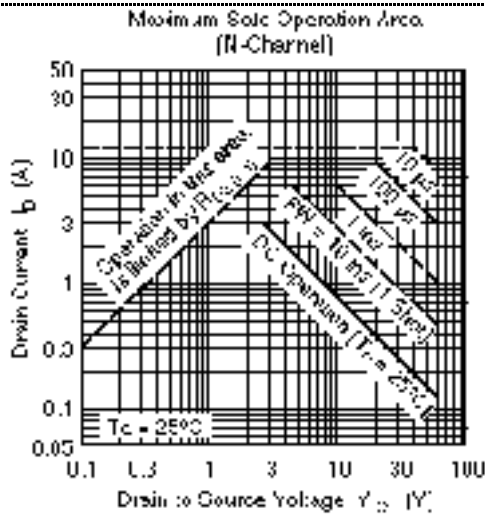
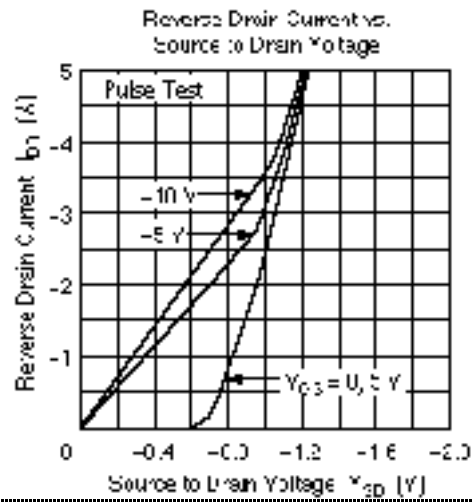
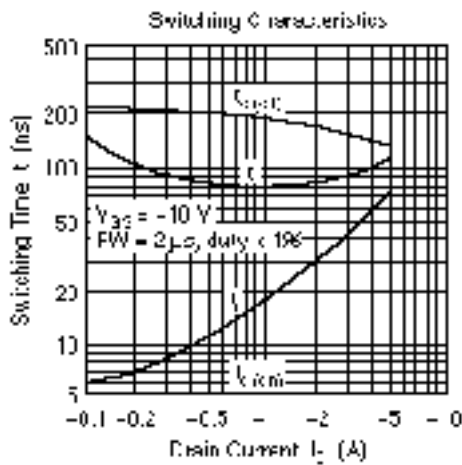
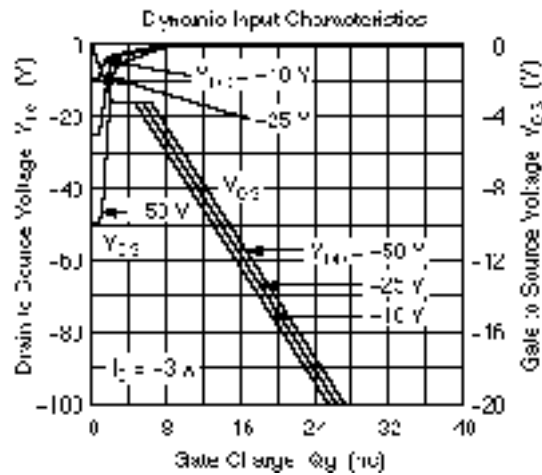
Polarity of test conditions for P channel device is reversed.

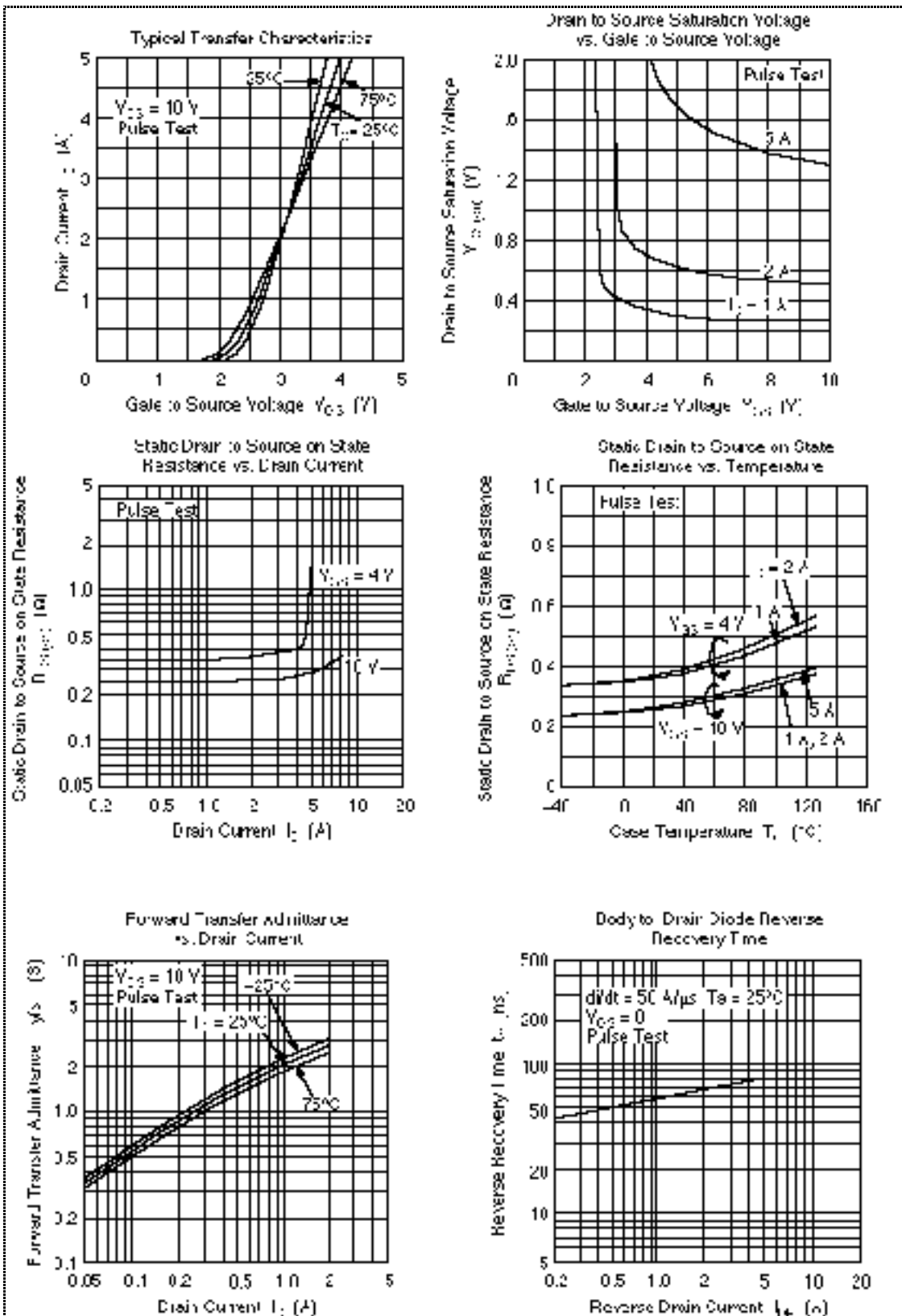






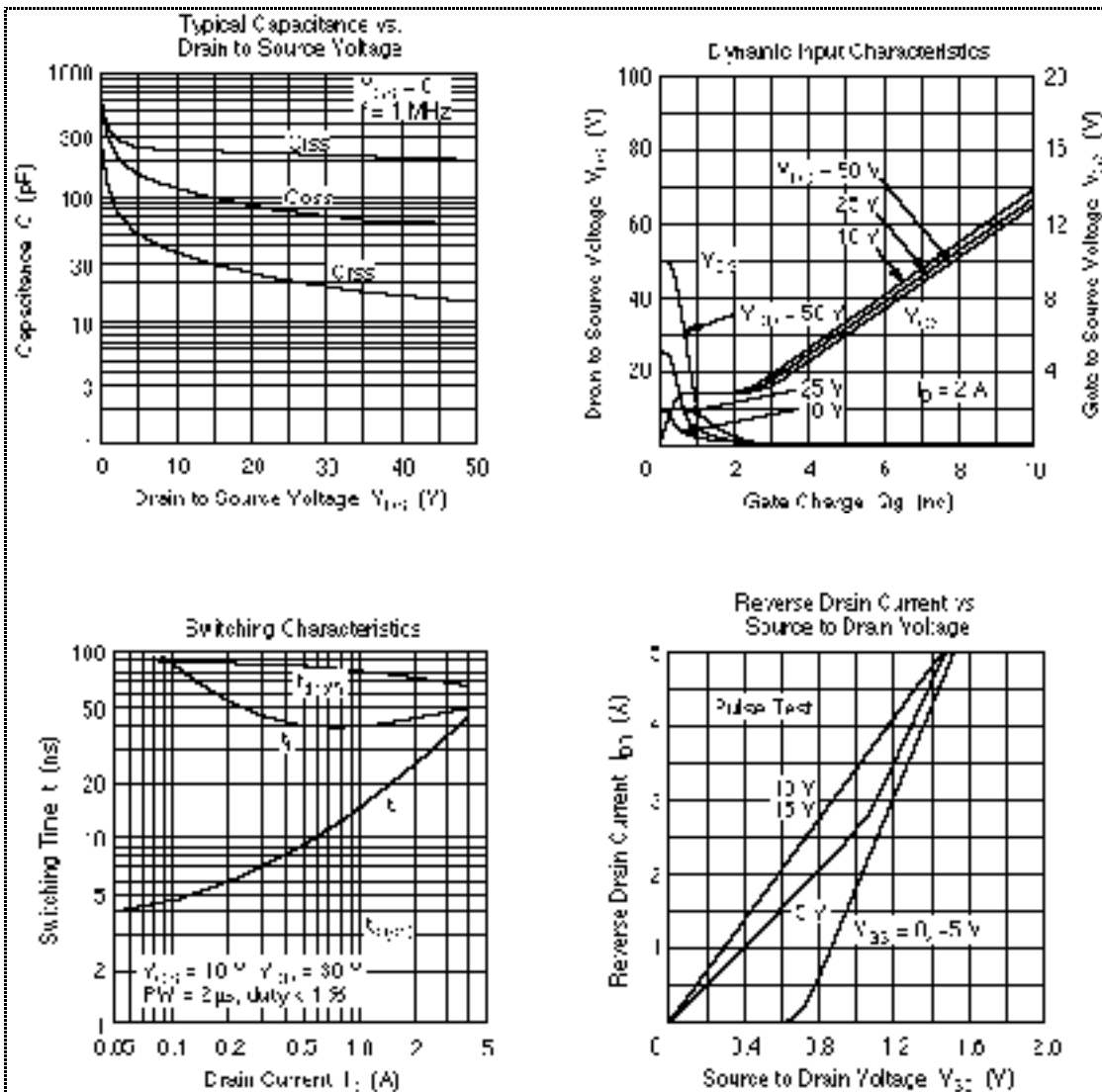
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