

# 4518B

## DUAL 4-BIT DECADE COUNTER

**DESCRIPTION** — The 4518B is a Dual 4-Bit Internally Synchronous BCD Counter. Each counter has both an active HIGH Clock Input (CP<sub>0</sub>) and an active LOW Clock Input ( $\overline{\text{CP}}_1$ ), buffered Outputs from all four bit positions (Q<sub>0</sub>-Q<sub>3</sub>) and an active HIGH overriding asynchronous Master Reset Input (MR).

The counter advances on either the LOW-to-HIGH transition of the CP<sub>0</sub> Input if  $\overline{\text{CP}}_1$  is HIGH or the HIGH-to-LOW transition of the CP<sub>1</sub> Input if CP<sub>0</sub> is LOW (see the Truth Table). Either Clock Input (CP<sub>0</sub>,  $\overline{\text{CP}}_1$ ) may be used as the Clock Input to the counter and the other Clock Input may be used as a Clock Inhibit Input.

A HIGH on the Master Reset Input (MR) resets the counter (Q<sub>0</sub>-Q<sub>3</sub> = LOW) independent of the Clock Inputs (CP<sub>0</sub>,  $\overline{\text{CP}}_1$ ).

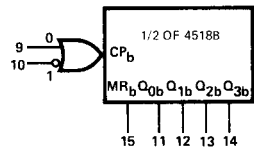
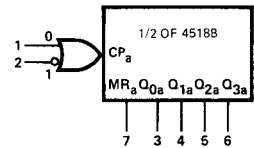
- TYPICAL COUNT FREQUENCY OF 10 MHz AT V<sub>DD</sub> = 10 V
- TRIGGERED ON EITHER A LOW-TO-HIGH OR A HIGH-TO-LOW TRANSITION
- ASYNCHRONOUS ACTIVE HIGH MASTER RESET
- BUFFERED OUTPUTS FROM ALL FOUR BIT POSITIONS
- FULLY SYNCHRONOUS COUNTING

TRUTH TABLE

CP <sub>0</sub>	$\overline{\text{CP}}_1$	MR	MODE
	H	L	Counter Advances
	L	L	Counter Advances
	X	L	No Change
	X	L	No Change
	L	L	No Change
	L	L	No Change
X	X	H	Reset (Asynchronous)

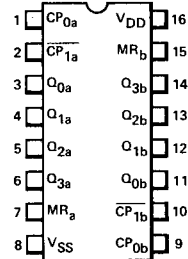
X = Don't Care  
 L = LOW Level  
 H = HIGH Level  
 = Positive-Going Transition  
 = Negative-Going Transition

### LOGIC SYMBOLS



V<sub>DD</sub> = Pin 16  
 V<sub>SS</sub> = Pin 8

### CONNECTION DIAGRAM DIP (TOP VIEW)

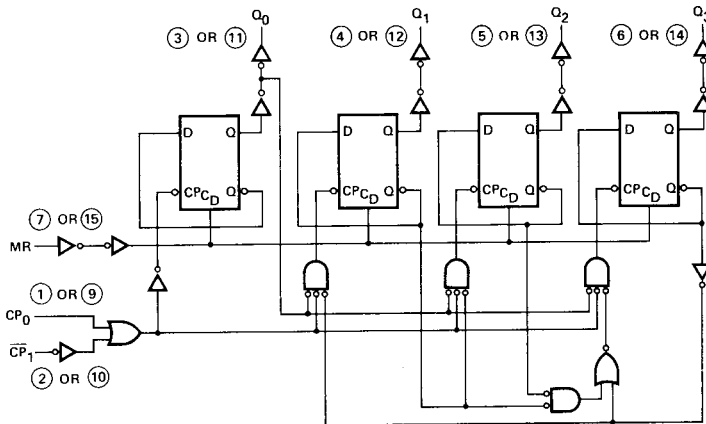


**NOTE:**  
 The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

### PIN NAMES

- CP<sub>0a</sub>, CP<sub>0b</sub> Clock Input (L → H (Triggered))
- $\overline{\text{CP}}_1a$ ,  $\overline{\text{CP}}_1b$  Clock Input (H → L (Triggered))
- MR<sub>a</sub>, MR<sub>b</sub> Master Reset Inputs
- Q<sub>0a</sub>-Q<sub>3a</sub> Outputs
- Q<sub>0b</sub>-Q<sub>3b</sub> Outputs

### 1/2 OF A 4518B LOGIC DIAGRAM



V<sub>DD</sub> = Pin 16  
 V<sub>SS</sub> = Pin 8  
 ○ = Pin Number

DC CHARACTERISTICS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS		
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V							
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX					
$I_{DD}$	Quiescent Power	XC			20			40			80	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$	
					150			300			600		MAX		
	Supply Current	XM			5			10			20		$\mu$ A		MIN, 25°C
					150			300			600				MAX

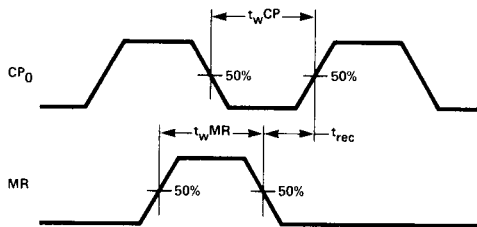
AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $F_{SS} = 0$  V,  $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, $CP_0$ or $\overline{CP_1}$ to $Q_n$		220	480		95	210		60	168	ns	CL = 50 pF, R <sub>L</sub> = 200 kΩ Input Transition Times ≤ 20 ns
$t_{PLH}$			220	480		95	210		60	168		
$t_{PHL}$	Propagation Delay, MR to $Q_n$		220	480		90	210		60	168	ns	
$t_{TLH}$	Output Transition Time		65	135		35	70		25	45	ns	
$t_{THL}$			65	135		35	70		25	45		
$t_{WMR}$	MR Minimum Pulse Width	180	70		70	30		56	20		ns	
$t_{WCP}$	$CP_0$ or $\overline{CP_1}$ Minimum Pulse Width	275	120		120	50		96	35		ns	
$t_{rec}$	MR Recovery Time	40	15		25	5		20	0		ns	
$t_s$	Set-Up Time, $CP_0$ to $\overline{CP_1}$	275	130		125	57		100	40		ns	
$t_s$	Set-Up Time, $\overline{CP_1}$ to $CP_0$	275	130		125	57		100	40		ns	
$f_{MAX}$	Input Count Frequency (Note 3)	2	4		4	10		5	12		MHz	

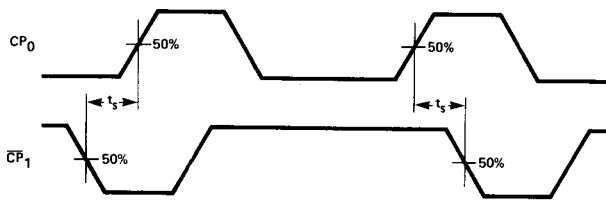
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For  $f_{MAX}$ , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 10$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.

SWITCHING WAVEFORMS



MINIMUM PULSE WIDTHS FOR  $CP_0$ ,  $\overline{CP_1}$  AND MR AND MR RECOVERY TIME



SET-UP TIMES,  $CP_0$  TO  $\overline{CP_1}$  AND  $\overline{CP_1}$  TO  $CP_0$

CONDITIONS:  $\overline{CP_1}$  = HIGH and the device triggers on a LOW-to-HIGH transition at  $CP_0$ . The timing also applies when  $CP_0$  = LOW and the device triggers on a HIGH-to-LOW transition at  $\overline{CP_1}$ .

NOTE:

Set-up and Hold Times are shown as positive values but may be specified as negative values.

TYPICAL ELECTRICAL CHARACTERISTICS

