CMOS 8-BIT UNIVERSAL BUS REGISTER

FEATURES

- Bidirectional Parallel Data Inputs
- Parallel or Serial Inputs/Parallel Outputs
- Asynchronous or Synchronous Parallel Data Loading
- Data Recirculation for Register Storage
- Parallel Enable on Data Lines for Bus Connection
- Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The 4034B is a Static Eight-Stage Parallel- or Serial-Input/Parallel-Output Register. It can be used to:

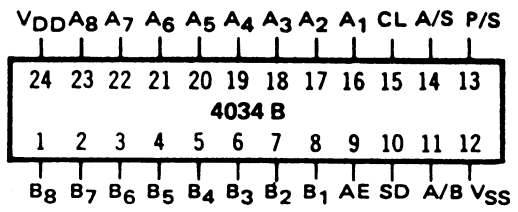
1. bidirectionally transfer parallel information between two buses,
2. convert serial data to parallel form and direct the parallel data to either of two buses,
3. store (recirculate) parallel data, or
4. accept parallel data from either of two buses and convert that data to serial form.

Inputs that control the operations include a single phase Clock (CL), "A" Data Enable (AE), Asynchronous/Synchronous (A/S), "A" bus to "B" bus/"B" bus to "A" bus (A/B), and Parallel/Serial (P/S). Data inputs include 16 bidirectional Parallel Data lines of which the eight "A" Data lines are inputs (outputs) and the "B" Data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for Serial data is also provided.

All register stages are D-type master/slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

Useful applications for this device include pseudo-random code generation, sample-and-hold register frequency and phase comparators, address or buffer register, and serial/parallel input/output conversion.

CONNECTION DIAGRAM
(all packages)



Add suffix for package:

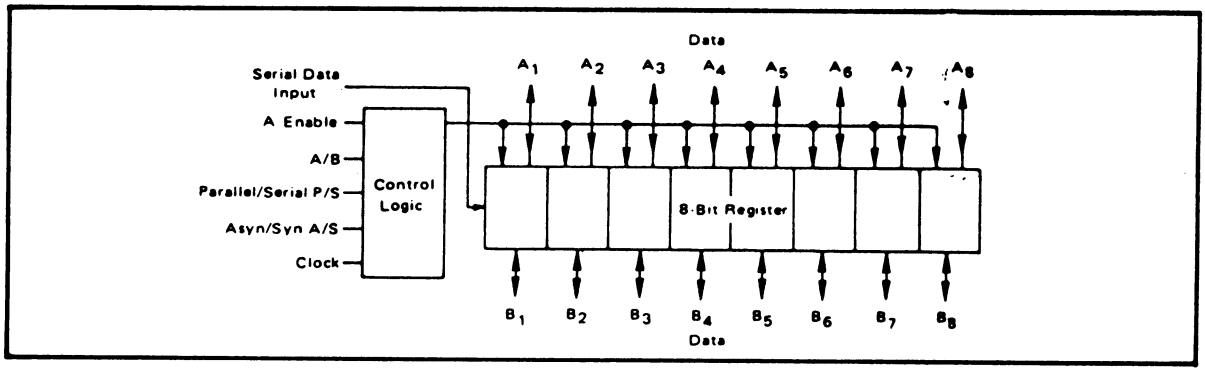
C 24-pin Ceramic
E 24-pin Epoxy

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN}=V_{SS}$ or V_{DD}	–	5	–	0.05	5	–	150	μAdc
		10	All valid inputs	–	10	–	0.1	10	–	300	
		15	combinations	–	20	–	0.2	20	–	600	
3-STATE OUTPUT LEAKAGE CURRENT	I_{ZL}	15		–	±0.1	–	$\pm 10^{-4}$	±0.1	–	±1.0	μAdc

NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME	t_{PLH}, t_{PHL}	5	–	350	700	ns
		10	–	120	240	
		15	–	100	200	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	180	360	ns
		10	–	90	180	
		15	–	70	140	
MINIMUM CLOCK PULSE WIDTH	PW_{CL}	5	–	125	250	ns
		10	–	50	100	
		15	–	40	80	
MAXIMUM CLOCK FREQUENCY	f_{CL}	5	2	4	–	MHz
		10	4	8	–	
		15	6	12	–	
MAXIMUM CLOCK RISE AND FALL TIME [1]	t_{rCL}, t_{fCL}	5	15	–	–	μs
		10	15	–	–	
		15	15	–	–	
MINIMUM HIGH-LEVEL PULSE WIDTH AE, P/S, A/S Inputs	PW_{AE}, $PW_{P/S}$, $PW_{A/S}$	5	–	180	360	ns
		10	–	90	180	
		15	–	70	140	
MINIMUM SETUP TIME A, B; Serial Inputs	t_{setup}	5	–	140	280	ns
		10	–	70	140	
		15	–	50	100	

[1] When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.

OPERATING INFORMATION

The 4034 B is composed of eight register cells connected in cascade with additional control logic. Each register cell is composed of one "D' master-slave flip-flop with separate internal clocks, and two data transfer gates allowing the data to be transferred bidirectionally from bus A to bus B and from bus B to bus A, and to be memorized. Besides the single phase clock and the serial data inputs, the control logic provides four other features:

A Enable Input – When high, this input enables the bus A data lines.

A/B Input (Data A or B) – This input controls the direction of data flow: when high, the data flows from bus A to bus B; when low, the data flows from bus B to bus A.

P/S Input (Parallel/Serial) – This input controls the data input mode (Parallel or Serial). When high, the data is transferred to the register in a parallel asynchronous mode or a parallel synchronous mode (positive clock transition). When low, the data is entered into the register in a serial synchronous mode (positive clock transition).

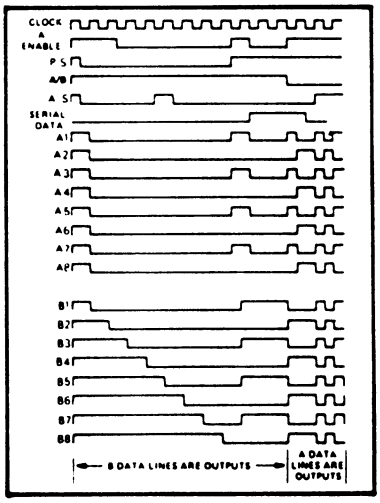
A/S Input (Asynchronous/Synchronous to the Clock) – When this input is high, the data is transferred independently from the clock rate; when low, the clock is enabled and the data is transferred synchronously.

Truth Table for Register Input-Levels and the Resulting Operation (L = Low Level, H = High, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

TIMING DIAGRAM



LOGIC DIAGRAM